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MICROCOMPUTER MN101C

MN101C57C/57D/F57D
LSI User's Manual

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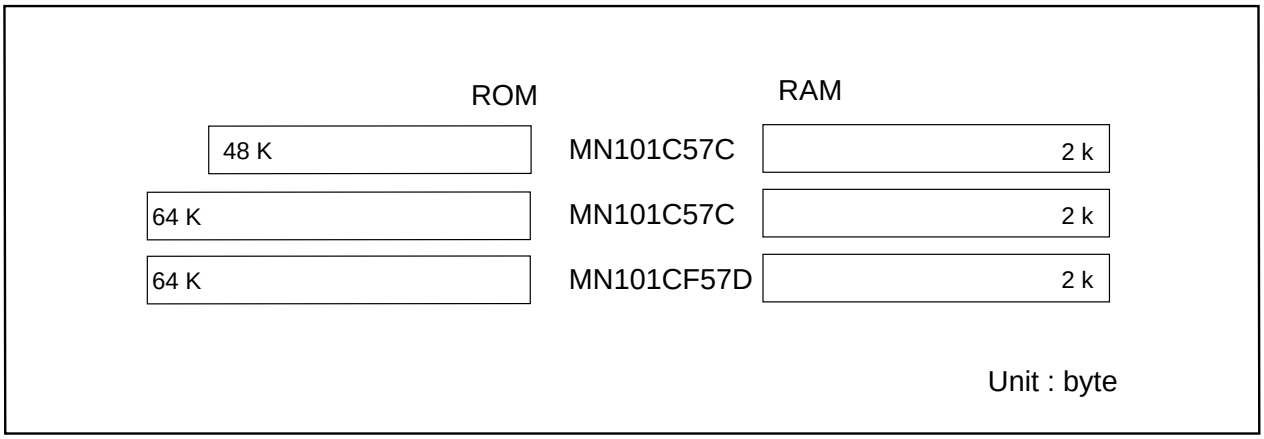
About This Manual

MN101C57 series offers a choice of masked ROM version. We're now developing user-programmable flash EEPROM version.



■Organization

In this LSI manual, this LSI functions are presented in the following order : overview, basic CPU functions, interrupt functions, port functions, timer functions, serial functions, and other peripheral hardware functions.

Each section contains overview of function, block diagram, control register, operation, and setting example.

■Organization

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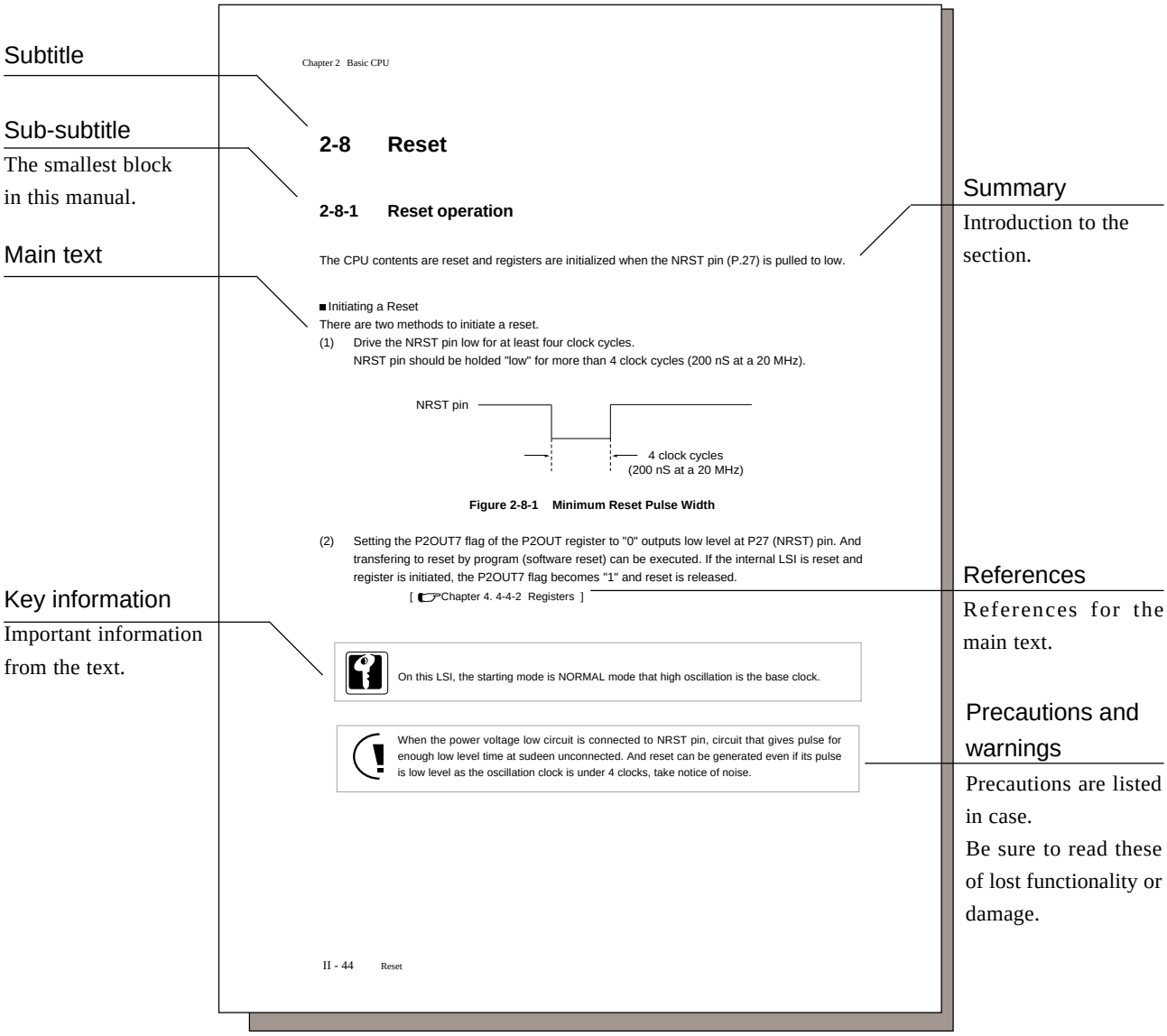
Each section contains overview of function, block diagram, control register, operation, and setting example.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.

The layout and definition of each section are shown below.


Subtitle
Sub-subtitle
The smallest block in this manual.
Main text
Key information
Important information from the text.
Summary
Introduction to the section.
References
References for the main text.
Precautions and warnings
Precautions are listed in case.
Be sure to read these of lost functionality or damage.
Chapter 2 Basic CPU
2-8 Reset
2-8-1 Reset operation
The CPU contents are reset and registers are initialized when the NRST pin (P.27) is pulled to low.
■ Initiating a Reset
There are two methods to initiate a reset.
(1) Drive the NRST pin low for at least four clock cycles.
NRST pin should be holded "low" for more than 4 clock cycles (200 nS at a 20 MHz).
NRST pin
4 clock cycles
(200 nS at a 20 MHz)
Figure 2-8-1 Minimum Reset Pulse Width
(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transfering to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.
[Chapter 4. 4-4-2 Registers]
On this LSI, the starting mode is NORMAL mode that high oscillation is the base clock.
When the power voltage low circuit is connected to NRST pin, circuit that gives pulse for enough low level time at sudeen unconnected. And reset can be generated even if its pulse is low level as the oscillation clock is under 4 clocks, take notice of noise.
II - 44 Reset

■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

(1) Consult the index at the front of the manual to locate the beginning of each section.
(2) Consult the table of contents at the front of the manual to locate desired titles.
(3) Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

■Related Manuals

Note that the following related documents are available.

"MN101C Series LSI User's Manual"
<Describes the device hardware.>
"MN101C Series Instruction Manual"
<Describes the instruction set.>
"MN101C Series Cross-assembler User's Manual"
<Describes the assembler syntax and notation.>
"MN101C Series C Compiler User's Manual: Usage Guide"
<Describes the installation, the commands, and options of the C Compiler.>
"MN101C Series C Compiler User's Manual: Language Description"
<Describes the syntax of the C Compiler.>
"MN101C Series C Compiler User's Manual: Library Reference"
<Describes the standard library of the C Compiler.>
"MN101C Series C Source Code Debugger User's Manual"
<Describes the use of C source code debugger.>
"MN101C Series PanaX Series Installation Manual"
<Describes the installation of C compiler, cross-assembler and C source code debugger and the procedure for bringing up the in-circuit emulator.>

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Chapter 1 Overview

1-1 Overview

1-1-1 Overview

The MN101C series of 8-bit single-chip microcomputers incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, remote control, fax machine, musical instrument, health care and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. This LSI has an internal 48 / 64 KB of ROM and 2 KB of RAM. Peripheral functions include 5 external interrupts, 24 internal interrupts including NMI, 8 timer counters, 2 sets of serial interfaces, A/D converter, watchdog timer, synchronous output function, buzzer output, and remote control output. The configuration of this microcomputer is well suited for application as a system controller in a camera, a sphygmomanometer, CD player, or MD.

With two oscillation system (max.20 MHz/32 kHz) contained on the chip, the system clock can be switched to **high frequency input** (high speed mode), or to **low frequency input** (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software.

A **machine cycle** (min. instructions execution) is 250 ns when fosc is 8 MHz, and when fosc is 20 MHz, a **machine cycle** is 100 ns. On the 2x-speed mode, CPU is operated with the same cycle to the external clock, when fosc is 8 MHz, a machine cycle is 125 ns. Two types of packages are available, 100-pin LQFP and 100-pin QFP.

1-1-2 Product Summary

This manual describes the following models of the MN101C57 series. These products have identical functions.

Table 1-1-1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101C57C	48 KB	2 KB	Mask ROM version
MN101C57D	64 KB	2 KB	Mask ROM version
MN101CF57D	64 KB	2 KB	Flash version

1-2 Hardware Functions

CPU Core **MN101C Core**

- LOAD-STORE architecture (3-stage pipeline)
- Half-byte instruction set / Handy addressing
- Machine cycle (at 2-devide of crystal oscillation)

High speed mode	0.10 µs / 20 MHz	(4.5 V to 5.5 V)
	0.25 µs/ 8 MHz	(2.7 V to 5.5 V)
	0.5 µs / 4 MHz	(2.2 V to 5.5 V)*1
	1.00 µs/ 2 MHz	(2.0 V to 5.5 V)*1
Low speed mode	62.5 µs / 32 kHz	(2.0 V to 5.5 V)*1

*1 Minimum rating for flash EEPROM vers. is 2.5 V to 5.5 V.

- Clock gear

  The operation speed of system clock can be changed by switching devide ratio of the oscillation with software.

- Operation modes

  NORMAL mode (High speed mode)
  SLOW mode (Low speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)

Internal memory < Single-chip Mode >

-Internal ROM*2	64 KB
-Internal RAM	2 KB

< Memory Expansion Mode >

-Internal ROM*2	64 KB
-Internal RAM	2 KB
-External ROM	128 KB
-External RAM	4 KB

*2 Differs depending upon the model. [☞ Chapter 1. 1-1-1 Product Summary]

Interrupts **24 Internal interrupts**

< Non maskable interrupt (NMI) >

- Incorrect code execution interrupt

< Timer interrupts >

- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt
- Timer 6 interrupt
- Time base interrupt
- Timer 7 interrupt
- Match interrupt for Timer 7 compare register 2
- Timer 8 interrupt
- Match interrupt for Timer 8 compare register 2

< Serial interrupts >
- Serial 0 interrupt 1
- Serial 0 interrupt 2
- Serial 2 interrupt

< A/D interrupt >
- A/D conversion interrupt

< Remote control interrupt >
- Remote control interrupt

8 External interrupts

- IRQ0 : Edge selectable. With/Without noise filter.
- IRQ1 : Edge selectable. With/Without noise filter. AC zero cross detector.
- IRQ2 : Edge selectable. Both edges interrupt. (STOP/HALT : can be recovered at the both edges)
- IRQ3 : Edge selectable. Both edges interrupt. (STOP/HALT : can be recovered at the both edges)
- IRQ4 : Key scan interrupt (At the falling edge. Also serves as an external interrupt)
- IRQ5 : Key scan interrupt (Either falling edge or rising edge is selectable.)
- IRQ6 : Edge selectable. Both edges interrupt. (STOP/HALT : can be recovered at the both edges)
- IRQ7 : Edge selectable. Both edges interrupt. (STOP/HALT : can be recovered at the both edges)

Timers / Counters 8 timers (7 can operate independently)

- 8-bit timer for general use 3 sets
- 8-bit timer (also serves as UART baud rate timer) 1 set
- 8-bit free-running timer 1 set
  Time base timer 1 set
- 16-bit timer for general use 2 sets

Timer 0 (8-bit timer for general use)

- Square wave output (Timer pulse output), PWM output, Event count, Remote control carrier output, Simple pulse width measurement
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock
- Square wave output and PWM output can be output to large current driver port P50 (TM00).

Timer 1 (8-bit timer for general use)

- Square wave output (Timer pulse output), Event count, 16-bit cascade connection function (connected to timer 0), Timer synchronous output
- Clock source
  fosc, fosc/4, fosc/16, fosc/2^{13}, fosc/2^{15}, fs/2, fs/8, fx, external clock

Timer 2 (8-bit timer for general use)

- Square wave output (Timer pulse output), Added pulse (2-bit)type PWM output,
  Event count, Timer synchronous output, Simple pulse width measurement
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

- Square wave output and PWM output can be output to large current driver port P52 (TM20).

Timer 3 (8-bit timer for general use)

- Square wave output (Timer pulse output), Event counter, Serial transfer clock, 16-bit cascade connection function (connect to timer 2), Remote control carrier output
- Clock source

  fosc, fosc/4, fosc/16, fosc/64, fosc/128, fs/2, fs/8, fx, external clock
- Can be used as UART baud rate timer

Timer 6 (8-bit free-running timer, Time base timer)

❑ **8-bit free-running timer**

- Clock source

  fosc, fosc/2^{12}, fosc/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}

❑ **Time base timer**

- Interrupt generation cycle

  fosc/2^{7}, fosc/2^{8}, fosc/2^{9}, fosc/2^{10}, fosc/2^{13}, fosc/2^{15},
  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)

- Clock source

  fosc, fosc/2, fosc/4, fosc/16, fs, fs/2, fs/4, fs/16,
  1/1, 1/2, 1/4, 1/16 of the external clock
- Hardware organization

Compare register with double buffer	2 sets
Input capture register	1 set
Timer interrupt	2 vectors

- Timer functions

  Square wave output (Timer pulse output), Event count,
  High precision PWM output (Cycle/Duty can be changed constantly),
  Timer synchronous output, Input capture function (Both edges can be operated)
- Square wave output and PWM output can be output to large current driver port P51 (TM70).

Timer 8 (16-bit timer for general use)

- Clock source

  fosc, fosc/2, fosc/4, fosc/16, fosc/128, fs, fs/2, fs/4, fs/16, fs/128,
  1/1, 1/2, 1/4, 1/16 of the external clock
- Hardware organization

Compare register with double buffer	2 sets
Input capture register	1 set
Timer interrupt	2 vectors

- Timer functions

  Square wave output (Timer pulse output), Event count,
  High precision PWM output (Cycle / Duty continuous changeable),
  Input capture function (Both edges can be operated)
- Square wave output and PWM output can be output to large current driver port P53 (TM80).

Watchdog timer

- Time-out period can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$.
- On detection of errors, hardware reset is done by force in LSI.

Synchronous output function

Timer synchronous output, Interrupt synchronous output

- Port 4 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 2, or 7, or of the external interrupt 2 (IRQ2).

Buzzer output Output frequency can be selected from $fosc/2^9$, $fosc/2^{10}$, $fosc/2^{11}$, $fosc/2^{12}$, $fosc/2^{13}$, $fosc/2^{14}$, $fx/2^3$, $fx/2^4$.

Remote Control output

Based on the timer 0 and timer 3 outpout, a remote control carrier with duty cycle of 1/2 or 1/3 can be output.

Remote Control reception

-Compatible with the Kaseikyo format (Setup can be adjusted to optional format)

-Queued reception by low speed clock

A/D converter **10 bits X 16 channels**

Serial interface **2 types**

Serial 0 (Duplex UART / Synchronous serial interface)

❑ **Synchronous serial interface**

- Transfer clock source
  fosc/2, fosc/4, fosc/16, fosc/64, fs/2, fs/4, timers 3 output, External clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrary transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

❑ **Duplex UART (Baud rate timer : Timers 3)**

- Parity check, Overrun error / framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 2 (Synchronous serial interface)

- Transfer clock source
  fosc/2, fosc/4, fosc/16, fosc/32, fs/2, fs/4, timer 3 output, External clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrary transfer size 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

LED driver **5 pins (push-pull configuration)**

LCD driver **LCD driver pins**

- Segment output : 47 pins max. (SEG0 to 46)
  SEG0 to 7 are switchable to I/O ports in unit of 8 pins.
  SEG8 to 33, 35 to 38 are switchable to I/O ports in unit of 2 pins.
  SEG34, 39 to 46 are switchable to I/O ports in 1 pin unit.
  [Note : At reset, SEG0 to 46 are input ports.]
- Common output pins : 4 pins
  COM0 to 3 are switchable to I/O ports in 1 pin unit.

Display mode selection

static
1/2 duty, 1/2 bias
1/3 duty, 1/3 bias
1/4 duty, 1/3 bias

LCD driver clock

The source clock is the main clock (fosc) :
$1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$
The source clock is the sub-clock (fx) :
$1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$

LCD power supply

LCD power supply is separated from V_{DD} (usable at $V_{LC1} \leq V_{DD}$).
(External supply voltage is input from V_{LC1} and V_{LC2} and V_{LC3} pins. Or voltage applied to V_{LC1} is divided by internal resistance, and supplied to V_{LC2} and V_{LC3} pins.)

Port **I/O ports** **77 ports**

- LED (large current) driver ports 5 ports (push-pull configuration)

Input ports **6 ports**

- also used for External interrupt 6 ports

Special pins

- Analog reference voltage input pins : 2 pins
- Operation mode input pin : 1 pin
- Reset input pins : 1 pin
- Power pins : 4 pins
- Oscillation pins : 4 pins
- NC pin : 2 pins
- LCD power supply pin : 3 pins

Package **100-pin LQFP (14 mm square / 0.5 mm pitch)**
100-pin QFP (18 mm square / 0.65 mm pitch)

Package code name **LQFP0100 - P - 1414**
QFP100 - P - 1818B

1-3 Pin Description

1-3-1 Pin Configuration

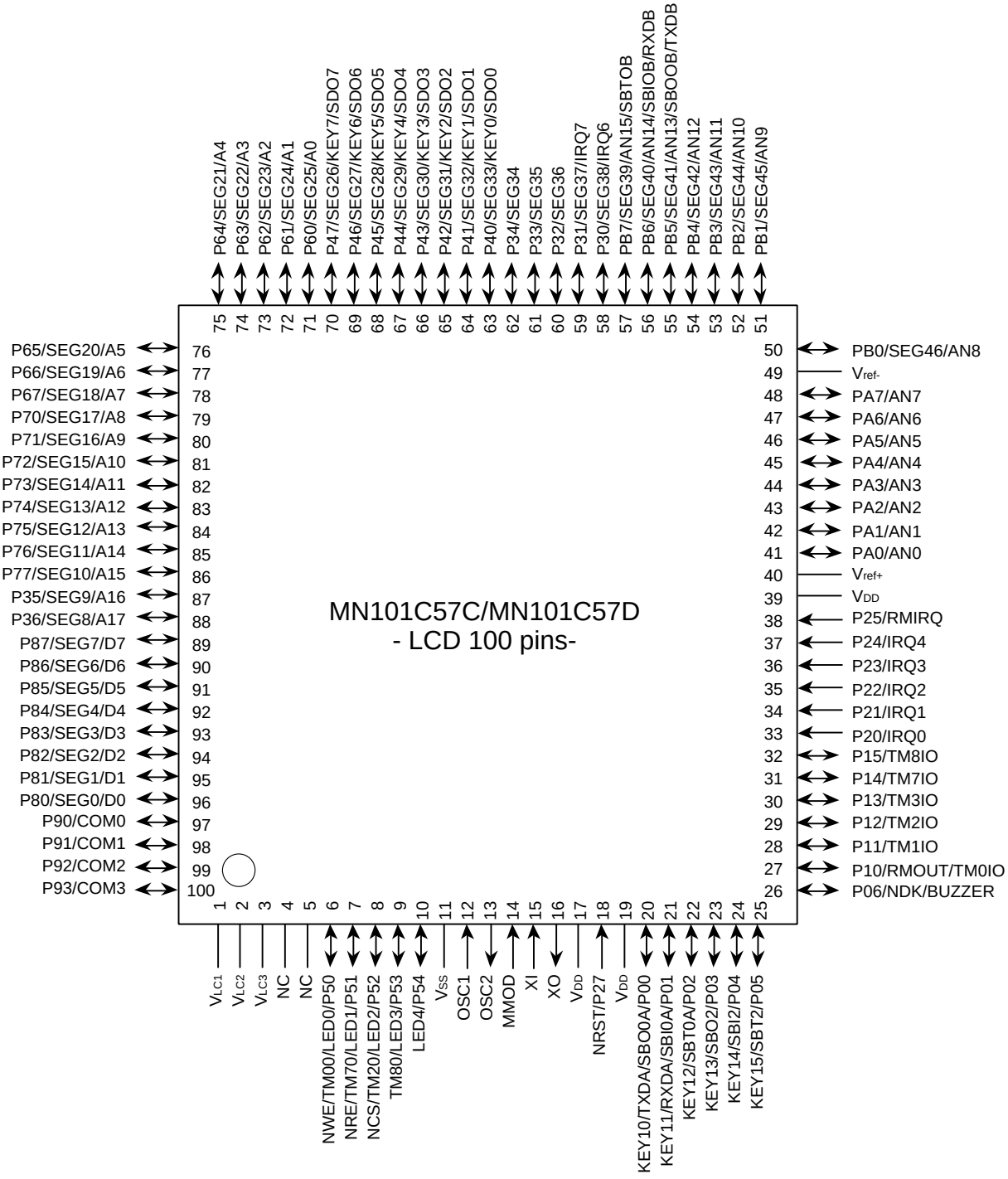

Figure 1-3-1 Pin Configuration (100LQFP : Top view)

1-3-2 Pin Specification

Table 1-3-1 Pin Specification (1/2)

Pins	Special Functions	I/O	Direction Control	Pin Control	Functions Description
P00	SBO0 TXDA KEY10	in/out	P0DIR0	P0PLUD0	SBO0 : Serial 0 transmission data output TXD : UART transmission data output KEY10:KEY interrupt imput 10
P01	SBI0 RXDA KEY11	in/out	P0DIR1	P0PLUD1	SBI0 : Serial 0 reception data input RXD : UART reception data input KEY11:KEY interrupt imput 11
P02	SBT0 KEY12	in/out	P0DIR2	P0PLUD2	SBT0 : Serial 0 clock input / output RXD : UART reception data input KEY12:KEY interrupt imput 12
P03	SBO2 KEY13	in/out	P0DIR3	P0PLUD3	SBO2 : Serial 2 transmission data output RXD : UART reception data input KEY13:KEY interrupt imput 13
P04	SBI2 KEY14	in/out	P0DIR4	P0PLUD4	SBI2 : Serial 2 reception data input RXD : UART reception data input KEY14:KEY interrupt imput 14
P05	SBT2 KEY15	in/out	P0DIR5	P0PLUD5	SBT2 : Serial 2 clock input / output RXD : UART reception data input KEY15:KEY interrupt imput 15
P06	BUZZER	in/out	P0DIR6	P0PLUD6	BUZZER : Buzzer output
P10	TM0IO RMOUT	in/out	P1DIR0	P1PLUD0	TM0IO : Timer 0 input / output RMOUT : Remote control carrier output
P11	TM1IO	in/out	P1DIR1	P1PLUD1	TM1IO : Timer 1 input / output
P12	TM2IO	in/out	P1DIR2	P1PLUD2	TM2IO : Timer 2 input / output
P13	TM3IO	in/out	P1DIR3	P1PLUD3	TM3IO : Timer 3 input / output
P14	TM4IO	in/out	P1DIR4	P1PLUD4	TM7IO : Timer 7 input / output
P15	TM5IO	in/out	P1DIR5	P1PLUD5	TM8IO : Timer 8 input / output
P20	IRQ0	in	-	P2PLU0	IRQ0 : External interrupt 0
P21	IRQ1 ACZ	in	-	P2PLU1	IRQ1 : External interrupt 1 ACZ : Zero-cross input
P22	IRQ2	in	-	P2PLU2	IRQ2 : External interrupt 2
P23	IRQ3	in	-	P2PLU3	IRQ3 : External interrupt 3
P24	IRQ4	in	-	-	IRQ4 : External interrupt 4
P25	RMIRQ	in	-	-	RMIRQ: Remote Control interrupt
P27	NRST	in	-	-	NRST : Reset
P30	IRQ6 SEG38	in/out	P3DIR0	P3PLU0	IRQ6 : External interrupt 6 SEG38: LCD segment output
P31	IRQ7 SEG37	in/out	P3DIR1	P3PLU1	IRQ7 : External interrupt 7 SEG37: LCD segment output
P32	SEG36	in/out	P2DIR1	P3PLU2	SEG36: LCD segment output
P33	SEG35	in/out	P3DIR3	P3PLU3	SEG35: LCD segment output
P34	SEG34	in/out	P3DIR4	P3PLU4	SEG34: LCD segment output
P35	SEG9 A16	in/out	P3DIR5	P3PLU5	A16: External expansion address SEG9: LCD segment output
P36	SEG8 A17	in/out	P3DIR6	P3PLU6	A17: External expansion address SEG8: LCD segment output
P40	KEY0 SDO0 SEG33	in/out	P4DIR0	P4PLU0	KEY0: KEY interrupt input 0 SDO0 : Timer synchronous output 0 SEG33 : LCD segment output
P41	KEY1 SDO1 SEG32	in/out	P4DIR1	P4PLU1	KEY1: KEY interrupt input 1 SDO1 : Timer synchronous output 1 SEG32 : LCD segment output
P42	KEY2 SDO2 SEG31	in/out	P4DIR2	P4PLU2	KEY2: KEY interrupt input 2 SDO2 : Timer synchronous output 2 SEG31 : LCD segment output
P43	KEY3 SDO3 SEG30	in/out	P4DIR3	P4PLU3	KEY3: KEY interrupt input 3 SDO3 : Timer synchronous output 3 SEG30 : LCD segment output
P44	KEY4 SDO4 SEG29	in/out	P4DIR4	P4PLU4	KEY4: KEY interrupt input 4 SDO4 : Timer synchronous output 4 SEG29 : LCD segment output
P45	KEY5 SDO5 SEG28	in/out	P4DIR5	P4PLU5	KEY5: KEY interrupt input 5 SDO5 : Timer synchronous output 5 SEG28 : LCD segment output
P46	KEY6 SDO6 SEG27	in/out	P4DIR6	P4PLU6	KEY6: KEY interrupt input 6 SDO6 : Timer synchronous output 6 SEG27 : LCD segment output
P47	KEY7 SDO7 SEG26	in/out	P4DIR7	P4PLU7	KEY7: KEY interrupt input 7 SDO7 : Timer synchronous output 7 SEG26 : LCD segment output
P50	TM0O LED0	in/out	P5DIR0	P5PLU0	TM0O : Timer 0 output LED0 : LED driver pin
P51	TM7O LED1	in/out	P5DIR1	P5PLU1	TM7O : Timer 7 output LED1 : LED driver pin
P52	TM2O LED2	in/out	P5DIR2	P5PLU2	TM2O : Timer 2 output LED2 : LED driver pin
P53	TM8O LED3	in/out	P5DIR3	P5PLU3	TM8O : Timer 8 output LED3 : LED driver pin
P54	LED4	in/out	P5DIR4	P5PLU4	LED4 : LED driver pin
P60	SEG25 A0	in/out	P6DIR0	P6PLU0	SEG25 : LCD segment output A0: External expansion address
P61	SEG24 A1	in/out	P6DIR1	P6PLU1	SEG24 : LCD segment output A1: External expansion address
P62	SEG23 A2	in/out	P6DIR2	P6PLU2	SEG23 : LCD segment output A2: External expansion address
P63	SEG22 A3	in/out	P6DIR3	P6PLU3	SEG22 : LCD segment output A3: External expansion address
P64	SEG21 A4	in/out	P6DIR4	P6PLU4	SEG21 : LCD segment output A4: External expansion address
P65	SEG20 A5	in/out	P6DIR5	P6PLU5	SEG20 : LCD segment output A5: External expansion address
P66	SEG19 A6	in/out	P6DIR6	P6PLU6	SEG19 : LCD segment output A6: External expansion address
P67	SEG18 A7	in/out	P6DIR7	P6PLU7	SEG18 : LCD segment output A7: External expansion address
P70	SEG17 A8	in/out	P7DIR0	P7PLU0	SEG17 : LCD segment output A8: External expansion address
P71	SEG16 A9	in/out	P7DIR1	P7PLU1	SEG16 : LCD segment output A9: External expansion address
P72	SEG15 A10	in/out	P7DIR2	P7PLU2	SEG15 : LCD segment output A10: External expansion address
P73	SEG14 A11	in/out	P7DIR3	P7PLU3	SEG14 : LCD segment output A11: External expansion address
P74	SEG13 A12	in/out	P7DIR4	P7PLU4	SEG13 : LCD segment output A12: External expansion address
P75	SEG12 A13	in/out	P7DIR5	P7PLU5	SEG12 : LCD segment output A13: External expansion address
P76	SEG11 A14	in/out	P7DIR6	P7PLU6	SEG11 : LCD segment output A14: External expansion address
P77	SEG10 A15	in/out	P7DIR7	P7PLU7	SEG10 : LCD segment output A15: External expansion address

Table 1-3-2 Pin Specification (2/2)

Pins	Special Functions	I/O	Direction Control	Pin Control	Functions Description
P80	SEG0 D0	in/out	P8DIR0	P8PLU0	SEG0 : LCD segment output D0: External expansion data
P81	SEG1 D1	in/out	P8DIR1	P8PLU1	SEG1 : LCD segment output D1: External expansion data
P82	SEG2 D2	in/out	P8DIR2	P8PLU2	SEG2 : LCD segment output D2: External expansion data
P83	SEG3 D3	in/out	P8DIR3	P8PLU3	SEG3 : LCD segment output D3: External expansion data
P84	SEG4 D4	in/out	P8DIR4	P8PLU4	SEG4 : LCD segment output D4: External expansion data
P85	SEG5 D5	in/out	P8DIR5	P8PLU5	SEG5 : LCD segment output D5: External expansion data
P86	SEG6 D6	in/out	P8DIR6	P8PLU6	SEG6 : LCD segment output D6: External expansion data
P87	SEG7 D7	in/out	P8DIR7	P8PLU7	SEG7 : LCD segment output D7: External expansion data
P90	COM0	in/out	P9DIR0	P9PLUD0	COM0 : LCD Common output
P91	COM1	in/out	P9DIR1	P9PLUD1	COM1 : LCD Common output
P92	COM2	in/out	P9DIR2	P9PLUD2	COM2 : LCD Common output
P93	COM3	in/out	P9DIR3	P9PLUD3	COM3 : LCD Common output
PA0	AN0	in/out	PADIR0	PAPLUD0	AN0: Analog 0 input
PA1	AN1	in/out	PADIR1	PAPLUD1	AN1: Analog 1 input
PA2	AN2	in/out	PADIR2	PAPLUD2	AN2: Analog 2 input
PA3	AN3	in/out	PADIR3	PAPLUD3	AN3: Analog 3 input
PA4	AN4	in/out	PADIR4	PAPLUD4	AN4: Analog 4 input
PA5	AN5	in/out	PADIR5	PAPLUD5	AN5: Analog 5 input
PA6	AN6	in/out	PADIR6	PAPLUD6	AN6: Analog 6 input
PA7	AN7	in/out	PADIR7	PAPLUD7	AN7: Analog 7 input
PB0	AN8 SEG46	in/out	PBDIR0	PBPLUD0	AN8: Analog 8 input
PB1	AN9 SEG45	in/out	PBDIR1	PBPLUD1	AN9: Analog 9 input
PB2	AN10 SEG44	in/out	PBDIR2	PBPLUD2	AN10: Analog 10 input
PB3	AN11 SEG43	in/out	PBDIR3	PBPLUD3	AN11: Analog 11 input
PB4	AN12 SEG42	in/out	PBDIR4	PBPLUD4	AN12: Analog 12 input
PB5	AN13 SEG41	TXDB	PBDIR5	PBPLUD5	AN13: Analog 13 input SBO0B : Serial 0 transmission data output TXDB : UART transmission data output
PB6	AN14 SEG40	RXDB	PBDIR6	PBPLUD6	AN14: Analog 14 input SBI0B : Serial 0 reception data input RXDB : UART reception data input
PB7	AN15 SEG39	in/out	PBDIR7	PBPLUD7	AN15: Analog 15 input SBT0B : Serial 0 clock input / output

1-3-3 Pin Functions

Table 1-3-3 Pin Function Summary (1/7)

Name	No.	I/O	Dual Function	Function	Description
VSS VDD	11 17 19 39			Power supply pin	Supply 2.0 V to 5.5 V to VDD and 0 V to VSS.
OSC1 OSC2	12 13	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	15 16	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open.
NRST	18	Input	P27	Reset pin [Active low]	This pin resets the chip when power is turned on, and is assigned to P27 and contains an internal pull-up resistor. Setting this pin low initializes the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and VDD, it is recommended that a discharge diode be placed between NRST and VDD.
P00 P01 P02 P03 P04 P05 P06	20 21 22 23 24 25 26	I/O	SBO0A, KEY10, TXDA SBI0A, KEY11, RXDA SBT0A, KEY12 SBO2, KEY13 SBI2, KEY14 SBT2, KEY15 BUZZER, NDK	I/O port 0	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P0PLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P10 P11 P12 P13 P14 P15	27 28 29 30 31 32	I/O	TM0IO, RMOUT TM1IO TM2IO TM3IO TM7IO TM8IO	I/O port 1	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-upp / pull-down resistor for each bit can be selected individually by the P1PLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Table 1-3-4 Pin Function Summary (2/7)

Name	No.	I/O	Dual Function	Function	Description
P20 P21 P22 P23 P24 P25	33 34 35 36 37 38	Input	IRQ0 IRQ1, ACZ IRQ2 IRQ3 IRQ4 RMIRQ	Input port 2	6-bit input port. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, pull-up resistors are disabled.
P27	18	Input	NRST	I/O port 2	Port P27 has an n-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.
P30 P31 P32 P33 P34 P35 P36	58 59 60 61 62 87 88	I/O	SEG38 SEG37 SEG36 SEG35 SEG34 SEG9, A16 SEG8, A17	I/O port 3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P40 P41 P42 P43 P44 P45 P46 P47	63 64 65 66 67 68 69 70	I/O	KEY0, SDO0, SEG33 KEY1, SDO1, SEG32 KEY2, SDO2, SEG31 KEY3, SDO3, SEG30 KEY4, SDO4, SEG29 KEY5, SDO5, SEG28 KEY6, SDO6, SEG27 KEY7, SDO7, SEG26		8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up resistor for each bit can be selected individually by the P4PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P50 P51 P52 P53 P54	6 7 8 9 10	I/O	TM0O, LED0 TM7O, LED1 TM2O, LED2 TM8O, LED3 LED4	I/O port 5	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P60 P61 P62 P63 P64 P65 P66 P67	71 72 73 74 75 76 77 78	I/O	SEG25 A0 SEG24 A1 SEG23 A2 SEG22 A3 SEG21 A4 SEG20 A5 SEG19 A6 SEG18 A7	I/O port 6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P70 P71 P72 P73 P74 P75 P76 P77	79 80 81 82 83 84 85 86	I/O	SEG17 A8 SEG16 A9 SEG15 A10 SEG14 A11 SEG13 A12 SEG12 A13 SEG11 A14 SEG10 A15	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up resistor for each bit can be selected individually by the P7PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Table 1-3-5 Pin Function Summary (3/7)

Name	No.	I/O	Dual Function	Function	Description
P80 P81 P82 P83 P84 P85 P86 P87	96 95 94 93 92 91 90 89	I/O	SEG0, D0 SEG1, D1 SEG2, D2 SEG3, D3 SEG4, D4 SEG5, D5 SEG6, D6 SEG7, D7	I/O port 8	8-bit CMOS tri-state I/O port. Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P90 P91 P92 P93	97 98 99 100	I/O	COM0 COM1 COM2 COM3	I/O port 9	4-bit CMOS tri-state I/O port. Each individual bit can be switched to an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	41 42 43 44 45 46 47 48	I/O	AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	I/O port A	8-bit CMOS tri-state I/O port.. A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD resister. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode is selected and pull-up resistors are disabled.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	50 51 52 53 54 55 56 57	I/O	AN8, SEG46 AN9, SEG45 AN10, SEG44 AN11, SEG43 AN12, SEG42 AN13, SEG41, SBO0B, TXDB AN14, SEG40, SBI0B, RXDB AN15, SEG39, SBT0B	I/O port B	8-bit CMOS tri-state I/O port.. A pull-up or pull-down resistor for each bit can be selected individually by the PBPLUD resister. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode is selected and pull-up resistors are disabled.
SBO0A SBO2	20 23	Output Output	P00, TXDA P03	Serial interface transmission data output pins	Transmission data output pins for serial interfaces 0, 2. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up and pull-down resistors can be selected by the P0PLUD register. Select output mode by the P0DIR register, and serial data output mode by serial mode register 1 (SC0MD1, SC2MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI2	20 21	Input Input	P01, RXDA P04	Serial interface received data input pins	Receive data output pins for serial interfaces 0 , 2. Pull-up and pull-down resistors can be selected by the P0PLUD register. Select input mode by the P0DIR register, and serial input mode by the serial mode register 1 (SC0MD1, SC2MD1). These can be used as normal I/O pins when the serial interface is not used.

Table 1-3-6 Pin Function Summary (4/7)

Name	No.	I/O	Dual Function	Function	Description
SBT0A SBT2	22 25	I/O I/O	P02 P05	Serial interface clock I/O pins	Clock I/O pins for serial interfaces 0 , 2. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up and pull-down resistors can be selected by the P0PLUD register. Select clock I/O for each communication mode by the P0DIR register and serial mode register 1 (SC0MD1, SC2MD1). These can be used as normal I/O pins when the serial interface is not used.
TXDA TXDB	20 55	Output	SBO0A, P00 SBO0B, PB5	UART transmission data output pins	In the serial interface in UART mode, this pin is configured as the transmission data output pin. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up and pull-down resistors can be selected by the P0PLUD and PBPLU resister. Select output mode by the P0DIR and PBDIR register, and serial data output by serial 0 mode register 1 (SC0MD1). This can be used as normal I/O pin when the serial interface is not used.
RXDA RXDB	21 56	Input	SBI0A, P01 SBI0B, PB6	UART received data input pin	In the serial interface in UART mode, this pin is configured as the received data input pin. Pull-up and pull-down resistors can be selected by the P0PLUD and PBPLU register. Set this pin to the input mode by the P0DIR and PBDIR register, and to the serial input mode by the serial 0 mode register 1 (SC0MD1). This can be used as normal I/O pin when the serial interface is not used.
TM0IO TM1IO TM2IO TM3IO	27 28 29 30	I/O	P10, RMOUT P11 P12 P13	Timer I/O pins	Event counter clock input pins, timer output and PWM signal output pins for 8-bit timers 0 to 3. To use these pins as event clock inputs, configure them as inputs by the P1DIR register. When the pins are used as inputs, pull-up and pull-down resistors can be select by the P1PLUD register. For timer output, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. When not used for timer I/O, these can be used as normal I/O pins.
RMOUT	27	I/O	P10,TM0IO	Remote control transmission signal output pin	Output pin for remote control transmission signal with a carrier signal. For remote control carrier output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. Also, set to the remote control carrier output by the remote control carrier output control register (RMCTR). This can be used as a normal I/O pin when remote control is not used.

Table 1-3-7 Pin Function Summary (5/7)

Name	No.	I/O	Dual Function	Function	Description
BUZZER	26	Output	P06	Buzzer output	Piezoelectric buzzer driver pin. The driving frequency can be selected by the DLYCTR register. Select output mode by the P0DIR register and select P06 buzzer output by the DLYCTR register. When not used for buzzer output, this pin can be used as a normal I/O pin.
TM7IO TM8IO	31 32	I/O	P14 P15	Timer I/O pin	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer 7, 8. To use this pin as event clock input, select input mode with the P1DIR register. In the input mode, pull-up and pull-down resistors can be selected with the P1PLUD register. For timer output, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD), and set to the output mode by the P1DIR register. When not used for timer I/O, this can be used as normal I/O pin.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	63 64 65 66 67 68 69 70	Output	KEY0, SEG33 KEY1, SEG32 KEY2, SEG31 KEY3, SEG30 KEY4, SEG29 KEY5, SEG28 KEY6, SEG27 KEY7, SEG26	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 4 synchronous output control register (P4SYO). Set to the output mode by the P4DIR register. When not used for synchronous output, these pins can be used as a normal I/O pins.
V_{ref+} V_{ref-}	40 49	- -		+power supply for A/D converter - power supply for A/D converter	Reference power supply pins for the A/D converter. Normally, the values of $V_{ref+}=V_{DD}$ and $V_{ref-}=V_{SS}$ are used.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11 AN12 AN13 AN14 AN15	41 42 44 45 46 47 48 49 50 51 52 53 54 55 56 57	Input	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	Analog input pins	Analog input pins for an 16-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4 RMIRQ IRQ6 IRQ7	33 34 35 36 37 38 58 59	Input	P20 P21, ACZ P22 P23 P24 P25 P30 P31	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4,6,7 can be selected with the IRQnICR register. IRQ1 is an external interrupt pin that is able to deternine AC zero crossings. Both edge for IRQ2, 3, 4, 6, 7 are valid for interrupt. RMIRQ is Remote control interrupt pin. When these are not used for interrupts, these can be used as normal input pins.

Table 1-3-8 Pin Function Summary (6/7)

Name	No.	I/O	Dual Function	Function	Description
ACZ	42		P21, IRQ1	AC zero-cross detection input pin	An input pin for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs a high level when the input is at an intermediate level. It outputs a low level at all other times. ACZ input signal is connected to the P21 input circuit and the IQR1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as a normal P21 input.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	63 64 65 66 67 68 69 70	Input	P40, SEG33, SDO0 P41, SEG32, SDO1 P42, SEG31, SDO2 P43, SEG30, SDO3 P44, SEG29, SDO4 P45, SEG28, SDO5 P46, SEG27, SDO6 P47, SEG26, SDO7	Key interrupt input pins	Input pins for interrupt based on ORed result of pin inputs. Key input pin for 2 bit and 1 bit can be selected individually by the key interrupt control register (P4IMD), (P0IMD). When not used for KEY input, these pins can be used as normal I/O pins.
KEY10 KEY11 KEY12 KEY13 KEY14 KEY15	20 21 22 23 24 25				
LED0 LED1 LED2 LED3 LED4	6 7 8 9 10	output	P50, TM0O P51, TM7O P52, TM2O P53, TM8O P54	LED driver pins	Large current output pins, These pins can be used as timer output pins. Each bit can be set individually as output mode by the P5OMD register. When not used for LED output, this pin can be used as a normal I/O pin.
TM0O TM7O TM2O TM8O	6 7 8 9	output	P50, LED0 P51, LED1 P52, LED2 P53, LED3	Timer output pins	Timer output and PWM signal output pins for 8-bit timer 0, 2 and 16-bit timer 7, 8. For timer output, PWM signal output, select the timer output by the port 5 output mode register (P5OMD) and set to the output mode by the P5DIR register.
V_{LC1} V_{LC2} V_{LC3}	1 2 3			Input pins for LCD power supply	Power supply pins for LCD . Voltage applied should be $5.5\ V \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} \geq 0\ V$. *1

Table 1-3-9 Pin Function Summary (7/7)

Name	No.	I/O	Dual Function	Function	Description
COM0 COM1 COM2 COM3	97 98 99 100	output	P90 P91 P92 P93	Output pins for LCD common	These pins output the common signal of the required timing to the LCD display. Connect to the common pins of LCD display panel. At reset, V_{SS} level is output. *2
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7 SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15 SEG16 SEG17 SEG18 SEG19 SEG20 SEG21 SEG22 SEG23 SEG24 SEG25 SEG26 SEG27 SEG28 SEG29 SEG30 SEG31 SEG32 SEG33 SEG34 SEG35 SEG36 SEG37 SEG38 SEG39 SEG40 SEG41 SEG42 SEG43 SEG44 SEG45 SEG46	96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50	output	P80 P81 P82 P83 P84 P85 P86 P87 P36 P35 P77 P76 P75 P74 P73 P72 P71 P70 P67 P66 P65 P64 P63 P62 P61 P60 P47, KEY7, SDO7 P46, KEY6, SDO6 P45, KEY5, SDO5 P44, KEY4, SDO4 P43, KEY3, SDO3 P42, KEY2, SDO2 P41, KEY1, SDO1 P40, KEY0, SDO0 P34 P33 P32 P31 P30 PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	LCD segment output pins	These pins are LCD segment driver pins. When not used segment output, these pins can be used as normal I/O pins by setting the LCD control register (LCCTR1 to 4). SEG0 to 7 can be switched in 8-bit units to I/O ports. SEG8 to 33, SEG35 to 38 can be switched in 2-bit units to I/O ports. SEG34, 39 to 46 can be switched in 1-bit units to I/O ports.
MMOD	14	Input		Memory mode switch input pin	This pin sets the memory expansion mode. Be sure to set the input low.

*1 The voltage input to V_{LC1} pin can be devided to V_{LC2} pin and V_{LC3} pin, with the internal voltage divider resistors.

*2 COM0 to 3 can be switched to normal ports 1 bit unit with the LCCTR1 register.

1-4 Block Diagram

1-4-1 Block Diagram

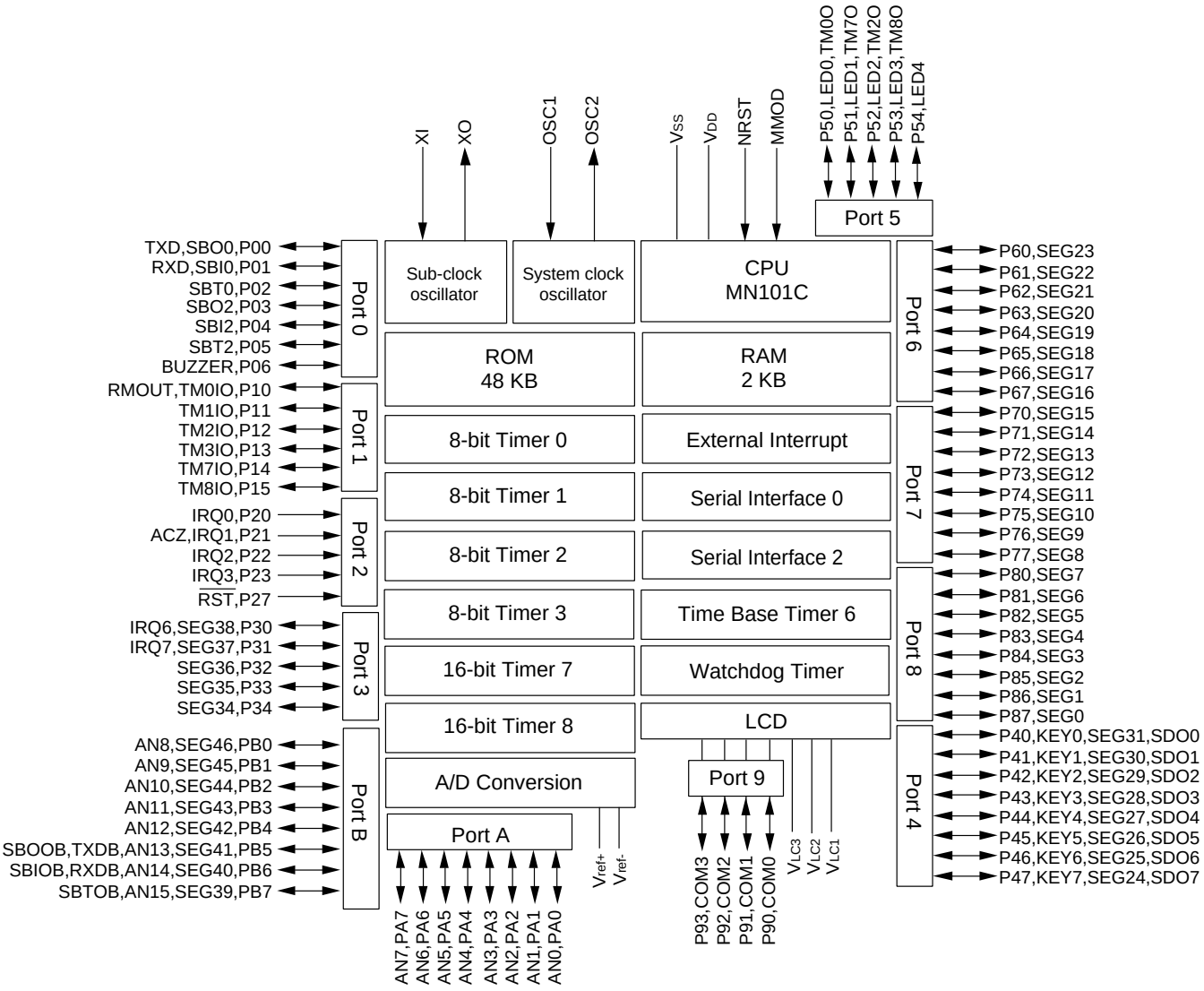

Figure 1-4-1 Block Diagram

1-5 Electrical Characteristics

This LSI user's manual describes the standard specification. Machine cycle (system clock fs) is described based on the standard mode : 1/2 of high oscillation at NORMAL mode, or on the clock frequency : 1/2 of low oscillation at SLOW mode. Please ask our sales offices for the product specifications.

Contents \ Model	MN101C57D
Structure	CMOS integrated circuit
Application	General purpose
Function	CMOS, 8-bit, single-chip microcontroller
Pin configuration	Fig. 1-3-1
External dimention	Fig. 1-7-1

1-5-1 Absolute Maximum Ratings*2,*3

No.	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	- 0.3 to +7.0	V
2	Input clamp current (ACZ)		IC	- 400 to 400	µA
3	Input pin voltage		V_I	- 0.3 to V_{DD} +0.3	V
4	Output pin voltage		V_O	- 0.3 to V_{DD} +0.3	
5	I/O pin voltage		V_{IO1}	- 0.3 to V_{DD} +0.3	
6	Peak output current	P5	I_{OL1} (peak)	30	mA
7		Other than P5	I_{OL2} (peak)	20	
8		All pins	I_{OH} (peak)	- 10	
9	Average output current *1	P5	I_{OL1} (avg)	20	
10		Other than P5	I_{OL2} (avg)	15	
11		All pins	I_{OH} (avg)	- 5	
12	Power dissipation		P_T	400	mW
13	Operating temperature		T_{opr}	- 40 to +85	°C
14	Storage temperature		T_{stg}	- 55 to +125	

*1 Applied to any 100-ms period.

*2 Connect at least one bypass capacitor of 0.1 µF or larger between the power supply pin and the ground for latch-up prevention.

*3 The absolute maximum ratings are the tolerance for the LSI to be operated properly, and not assures proper operation by itself.

1-5-2 Operating Conditions

Ta=-40 °C to +85 °C V_{SS}=0 V
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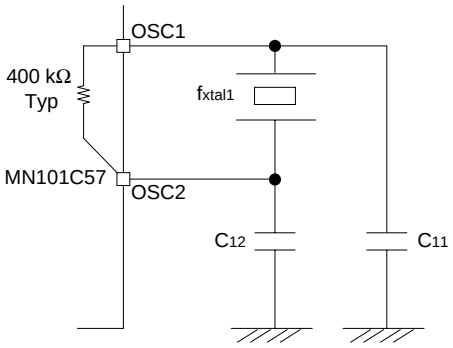
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *4							
1	Power supply voltage	V_{DD1}	fosc≤20 MHz	4.5		5.5	V
2		V_{DD2}	fosc≤8.38 MHz	2.7		5.5	
3		V_{DD3}	fosc≤4.19 MHz	2.2 (2.5)		5.5	
4		V_{DD4}	fosc≤2.0 MHz	2.0 (2.5)		5.5	
5		V_{DD5}	fx=32.768 kHz	2.0 (2.5)		5.5	
6	Voltage to maintain RAM data	V_{DD6}	During STOP mode	1.8		5.5	
Operation speed *5							
7	Instruction execution time	t_{c1}	V_{DD}=4.5 V to 5.5 V	0.10			µs
8		t_{c2}	V_{DD}=2.7 V to 5.5 V	0.238			
9		t_{c3}	V_{DD}=2.2 V to 5.5 V	0.50			
10		t_{c4}	V_{DD}=2.0 V to 5.5 V	1.00			
11		t_{c5}	V_{DD}=2.0 V to 5.5 V		61		

*4 fosc : Input clock frequency to OSC1 pin.
fx : Input clock frequency to XI pin.

*5 tc1, tc2, tc3, tc4 : When OSC1 is the CPU clock.
tc5 : When XI is the CPU clock.

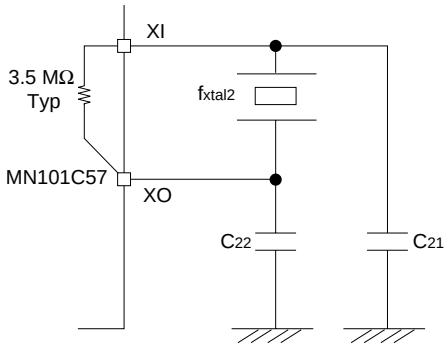
Ta=-40 °C to +85 °C V_{SS}=0 V
Flash EEPROM vers. is in ( ).

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Crystal oscillator 1 Fig. 1-5-1 [NORMAL mode : fs=fosc/2]							
12	Crystal frequency	f_{xtal1}	V_{DD}=Power supply voltage (Refer to the values of Power supply voltage 1t o 4.)	1.0		20	MHz
13	External capacitors	C_{11}			20		pF
14		C_{12}			20		
15	Internal feedback resistor	R_{f10}	V_{DD}=5.0 V		400		kΩ
Crystal oscillator 2 Fig. 1-5-2 [SLOW mode : fs=fx/2]							
16	Crystal frequency	f_{xtal2}	V_{DD}=2.0 V (2.5 V) to 5.5 V		32.768		kHz
17	External capacitors	C_{21}			20		pF
18		C_{22}			20		
19	Internal feedback resistor	R_{f20}	V_{DD}=5.0 V		3.5		MΩ



The feedback resistor is built-in.

Figure 1-5-1 Crystal Oscillator 1



The feedback resistor is built-in.

Figure 1-5-2 Crystal Oscillator 2

Note : Connect external capacitors that suits the used pin. When crystal oscillator or ceramic oscillator is used, the frequency is changed depending on the condenser rate. Therefore, consult the manufacturer of the pin for the appropreate external capacitor.

Ta=-40 °C to +85 °C V_{DD}=5.0 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
20	Clock frequency	f_{OSC1}		1.0		20.0	MHz
21	High level pulse width *6	t_{wh1}	Fig. 1-5-3	22.5			ns
22	Low level pulse width *6	t_{wl1}		22.5			
23	Rising time *7	t_{wr1}	Fig. 1-5-3	0		5.0	
24	Falling time *7	t_{wf1}		0		5.0	
External clock input 2 XI (XO is unconnected)							
25	Clock frequency	f_{OSC2}		32.768		100	kHz
26	High level pulse width *6	t_{wh2}	Fig. 1-5-4	4.5			µs
27	Low level pulse width *6	t_{wl2}		4.5			
28	Rising time *7	t_{wr2}	Fig. 1-5-4	0		20	ns
29	Falling time *7	t_{wf2}		0		20	

*6 The clock duty rate in the standard mode should be 45% to 55%.

*7 Rising time and falling time differ depending on the oscillation frequency.
The maximum values are standard, not the stipulated values.

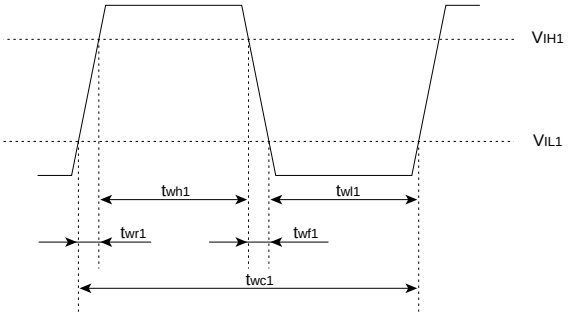


Figure 1-5-3 OSC1 Timing Chart

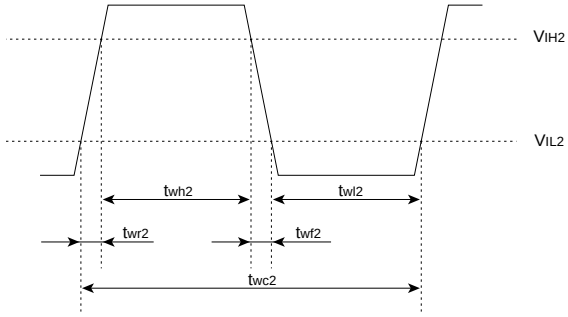


Figure 1-5-4 XI Timing Chart

1-5-3 DC Characteristics

Ta=-40 °C to +85 °C V_{SS}=0 V
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	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current (without load at output) *8 [NORMAL mode : fs=fosc/2 SLOW mode : fs=fx/2]							
1	Power supply current	I_{DD1}	fosc=20 MHz V_{DD}=5 V		15	30	mA
2		I_{DD2}	fosc=8.38 MHz V_{DD}=5 V		8	16	
3		I_{DD3}	fosc=4.19 MHz V_{DD}=5 V		5	10	
4		I_{DD4}	fx=32.768 kHz V_{DD}=3 V		30	60	µA
5	Suplly current during HALT1 mode	I_{DD5}	fx=32.768 kHz V_{DD}=3 V Ta=25 °C		4	8	
6		I_{DD6}	fx=32.768kHz V_{DD}=3 V Ta=85 °C			30	
7	Supply current during STOP mode	I_{DD7}	V_{DD}=5 V Ta=25 °C			2	
8			V_{DD}=5 V Ta=85 °C			50	

*8 Measured under conditions without load.

- The supply current during operation, I_{DD1}(I_{DD2}, I_{DD3}), is measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 20-MHz(8.39-MHz) square wave of V_{DD} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD4}, is measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32.768-kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT1 mode, I_{DD5}(I_{DD6}), is measured under the following conditions : After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and an 32.768-kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD7}, is measured under the following conditions : After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and the OSC1 and XI pins are unconnected.

Ta=-40 °C to +85 °C V_{DD}=2.0 V (2.5 V) to 5.5 V V_{SS}=0 V
Flash EEPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 MMOD							
9	Input high voltage 1	V_{IH1}		0.8 V_{DD}		V_{DD}	V
10	Input high voltage 2	V_{IH2}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
11	Input low voltage 1	V_{IL1}		0		0.2 V_{DD}	
12	Input low voltage 2	V_{IL2}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
13	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD}			± 2	µA
Input pin 2 P20 to P25 (Shmitt trigger input)							
14	Input high voltage	V_{IH3}		0.8 V_{DD}		V_{DD}	V
15	Input low voltage	V_{IL3}		0		0.2 V_{DD}	
16	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD}			± 2	µA
17	Input high current	I_{IH1}	V_{DD}=5.0 V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	

Ta=-40 °C to +85 °C V_{DD}=2.0 V (2.5 V) to 5.5 V V_{SS}=0 V
Flash EEPROM vers. is in ( ).

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 1 P27 (NRST) (Schmitt trigger input)							
18	Input high voltage	V_{IH4}		0.8 V_{DD}		V_{DD}	V
19	Input low voltage	V_{IL4}		0		0.15 V_{DD}	
20	Input leakage current	I_{LK3}	V_{IN}=0 V to V_{DD}			± 10	µA
21	Input high current	I_{IH2}	V_{DD}=5.0 V V=1.5 V Pull-up resistor ON	-30	-100	-300	
22	Output low voltage	V_{OL1}	V_{DD}=5.0 V V_{OL}=1.0 mA			0.5	V
I/O pin 2 P00 to P06, P10 to P15 (Schmitt trigger input)							
23	Input high voltage	V_{IH5}		0.8 V_{DD}		V_{DD}	V
24	Input low voltage	V_{IL5}		0		0.2 V_{DD}	
25	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD}			± 2	µA
26	Input high current	I_{IH3}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
27	Input low current	I_{IL3}	V_{DD}=5.0 V V_{IN}=3.5 V Pull-down resistor ON	30	100	300	
28	Output high voltage	V_{OH1}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
29	Output low voltage	V_{OL2}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	

Ta=-40 °C to +85 °C VDD=2.0 V (2.5 V) to 5.5 V VSS=0 V
Flash EEPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 3 P35, P36, P60 to P67, P70 to P77, P80 to P87							
30	Input high voltage 1	V_{IH6}		0.8 V_{DD}		V_{DD}	V
31	Input high voltage 2	V_{IH7}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
32	Input low voltage 1	V_{IL6}		0		0.2 V_{DD}	
33	Input low voltage 2	V_{IL7}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
34	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD}			± 2	µA
35	Input high current 1	I_{IH4}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
36	Output high voltage	V_{OH2}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
37	Output low voltage	V_{OL3}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	
I/O pin 4 P30 to P34, P40 to P47, P90 to P93, PB0 to PB7 (Schmitt trigger input)							
38	Input high voltage	V_{IH8}		0.8 V_{DD}		V_{DD}	V
39	Input low voltage	V_{IL8}		0		0.2 V_{DD}	
40	Input leakage current	I_{LK6}	V_{IN}=0 V to V_{DD}			± 2	µA
41	Input high current	I_{IH5}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
42	Output high voltage	V_{OH3}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
43	Output low voltage	V_{OL4}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	

Ta=-40 °C to +85 °C VDD=2.0 V (2.5 V) to 5.5 V VSS=0 V
Flash EEPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 5 P50 to P54							
44	Input high voltage 1	V_{IH9}		0.8 V_{DD}		V_{DD}	V
45	Input high voltage 2	V_{IH10}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
46	Input low voltage 1	V_{IL9}		0		0.2 V_{DD}	
47	Input low voltage 2	V_{IL10}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
48	Input leakage current	I_{LK7}	V_{IN}=0 V to V_{DD}			± 2	µA
49	Input high current	I_{IH6}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
50	Output high voltage	V_{OH4}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
51	Output low voltage 1	V_{OL5}	V_{DD}=5.0 V I_{OL}=1.0 mA (LED output OFF)			0.5	
52	Output low voltage 2	V_{OL6}	V_{DD}=5.0 V I_{OL}=15 mA (LED output OFF)			1.0	
I/O pin 6 PA0 to PA7 (Schmitt trigger input)							
53	Input high voltage 1	V_{IH11}		0.8 V_{DD}		V_{DD}	V
54	Input high voltage 2	V_{IH12}	V_{DD}=4.5 V to 5.5 V	0.7 V_{DD}		V_{DD}	
55	Input low voltage 1	V_{IL11}		0		0.2 V_{DD}	
56	Input low voltage 2	V_{IL12}	V_{DD}=4.5 V to 5.5 V	0		0.3 V_{DD}	
57	Input leakage current	I_{LK8}	V_{IN}=0 V to V_{DD}			± 2	µA
58	Input high current	I_{IH7}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	-30	-100	-300	
59	Input low current	I_{IH4}	V_{DD}=5.0 V V_{IN}=1.5 V Pull-up resistor ON	30	100	300	
60	Output high voltage	V_{OH5}	V_{DD}=5.0 V I_{OH}=-0.5 mA	4.5			V
61	Output low voltage	V_{OL7}	V_{DD}=5.0 V I_{OL}=1.0 mA			0.5	

Ta=-40 °C to +85 °C VDD=2.0 V (2.5 V) to 5.5 V VSS=0 V
Flash EEPROM vers. is in ( ).

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 4 P21 (when used as ACZ pin) V_{DD}=5.0 V							
62	Input high voltage 1	V_{DHH}	Fig. 1-5-5	4.5			V
63	Input high voltage 2	V_{DHL}		1.5			
64	Input low voltage 1	V_{DLH}				3.5	
65	Input low voltage 2	V_{DLL}				0.5	
66	Input leakage current	I_{LK10}	V_{IN}=0 V to V_{DD}			± 2	µA
67	Input clamp current	I_{C3}	V_{IN}>V_{DD} V_{IN}<0 V			± 400	
Display output pin 1 COM0 to COM3 *9 (V_{LC1}, V_{SS} voltage output)							
68	Output impedance	Z_{OCOM1}	V_{DD}=5.0 V V_{LC1}=5.0 V		3	6	kΩ
69		Z_{OCOM2}	V_{DD}=3.0 V V_{LC1}=3.0 V		8	15	
Display output pin 2 SEG0 to SEG46 *10 (V_{LC1}, V_{SS} voltage output)							
70	Output impedance	Z_{OSEG1}	V_{DD}=5.0 V V_{LC1}=5.0 V		15	30	kΩ
71		Z_{OSEG2}	V_{DD}=3.0 V V_{LC1}=3.0 V		30	60	
Display power supply voltage pin 1 V_{LC1}, V_{LC2}, V_{LC3}							
72	Internal deivision resistor	R_{VL1}	Ta=+25 °C *11 (V_{LC1} - V_{SS} impedance)	142.5	285	570	kΩ
73		R_{VL2}		15	30	60	

*9 COM0 to COM3 also function as P90 to P93.

*10 SEG0 to SEG46 also function as P30 to P36, P40 to P47, P60 to P67, P70 to P77, P80 to P87, and PB0 to PB7.

*11 The total resistance between V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and V_{SS}.

1-5-4 A/C Characteristics

Ta=-40 °C to +85 °C V_{DD}=5.0 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
ACZ pin							
1	Rising time	t_{rs}	Fig. 1-5-5	30			µs
2	Falling time	t_{fs}		30			

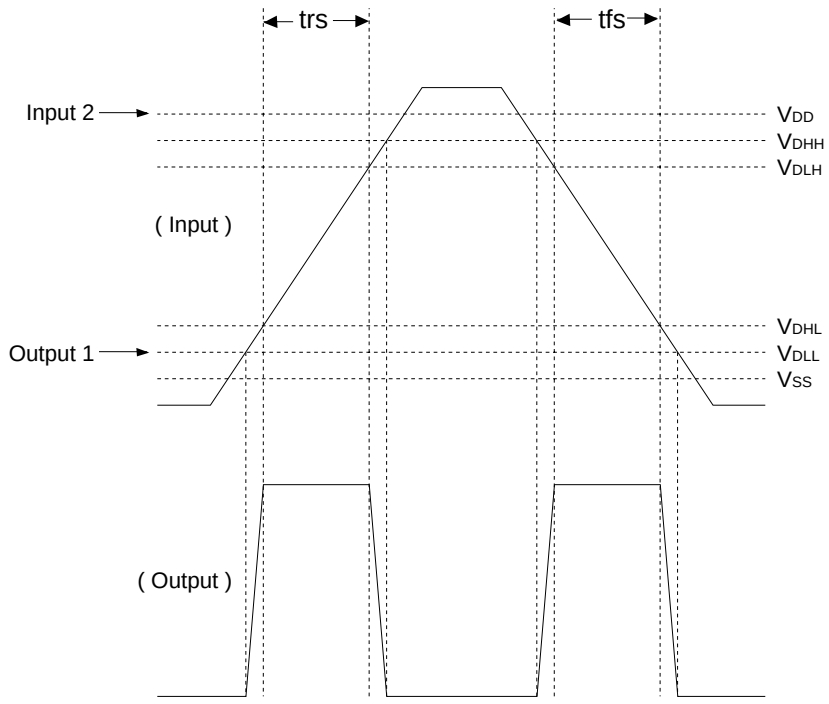


Figure 1-5-5 Operation of AC Zero-Cross Detection Circuit

1-5-5 A/D Converter Characteristics *11

Ta=-40 °C to +85 °C V_{DD}=5.0 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	bits
2	Non-linearity error 1		V_{DD}=5.0 V V_{SS}=0 V V_{ref+}=5.0 V V_{erf-}=0 V T_{AD}=800 ns			± 3	LSB
3	Differential non-linearity error 1					± 3	
4	Zero transition voltage		V_{DD}=5.0 V V_{SS}=0 V V_{ref+}=5.0 V V_{ref-}=0 V T_{AD}=1.00 µs		10	30	mV
5	Full-scale transition voltage			4970	4990		
6	A/D conversion time		f_{OSC}=8 MHz T_{AD}=1.00 µs	12		28	µs
7			fx=32.768 kHz T_{AD}=15.2 µs	183.12		427.28	
8	Sampling time		f_{OSC}=8 MHz T_{AD}=1.00 µs	2.0		18.0	
9			fx=32.768 kHz T_{AD}=15.2 µs	30.52		274.68	
10	Reference voltage	V_{erf+}	*	2.0		V_{DD}	V
11		V_{erf-}	*	V_{SS}		3.0	
12	Analog input voltage			V_{erf-}		V_{erf+}	
13	Analog input leakage current		V_{ADIN}=0 V to 5 V When channel OFF			± 2	µA
14	Reference voltage pin input leakage current		When V_{erf+} is OFF $V_{erf-} \leq V_{erf+} \leq V_{DD}$			± 10	
15	Ladder resistance	R_{LADD}	V_{DD}=5.0 V	20	50	80	kΩ

*11 T_{AD} means A/D conversion cycle.
The values of 2 to 5 are guaranteed on the condition that V_{DD}=V_{ref+}=5 V, V_{SS}=V_{ref-}=0 V.
* The gap between V_{ref+} and V_{ref-} should be set over 2 V.

1-6 Cautions for Circuit Setup

1-6-1 General Usage

■Connection of V_{DD} pin, and V_{SS} pin

All of the V_{DD} and V_{SS} pins should be connected directly to the power source and ground in the external. Put them on printed circuit board after the location of LSI (package) pin is confirmed.
Connection error may lead a fusion and breakdown of a micro controller.

■Cautions for Operation

(1) If you install the product close to high-field emissions (under the cathode ray tube, etc), shield the package surface to ensure normal performance.
(2) Operation temperature should be well considered. Each product has different condition. For example, if the operation temperature is over the condition, improper operation could be occurred.
(3) Operation voltage should be also well considered. Each product has different operating range.
- If the operation voltage is over the operating range, duration of the product could be shortened.
- If the operation voltage is below the operating range, improper operation could be occurred.

1-6-2 Unused Pins

■Unused Pins (output pins and LCD output pins)
Set unused pins (output pins and LCD output pins) open.

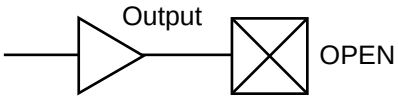


Figure 1-6-1 Unused Pins (only for output)

■Unused Pins (only for input)
Insert some 10 kΩ resistor to unused pins (only for input) for pull-up or pull-down. If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and causes power supply noise.

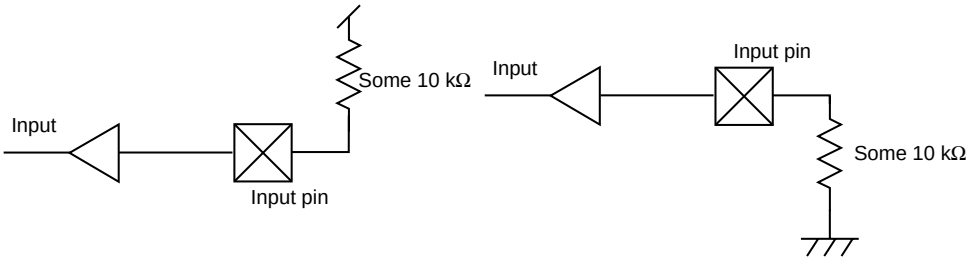


Figure 1-6-2 Unused Pins (only for input)

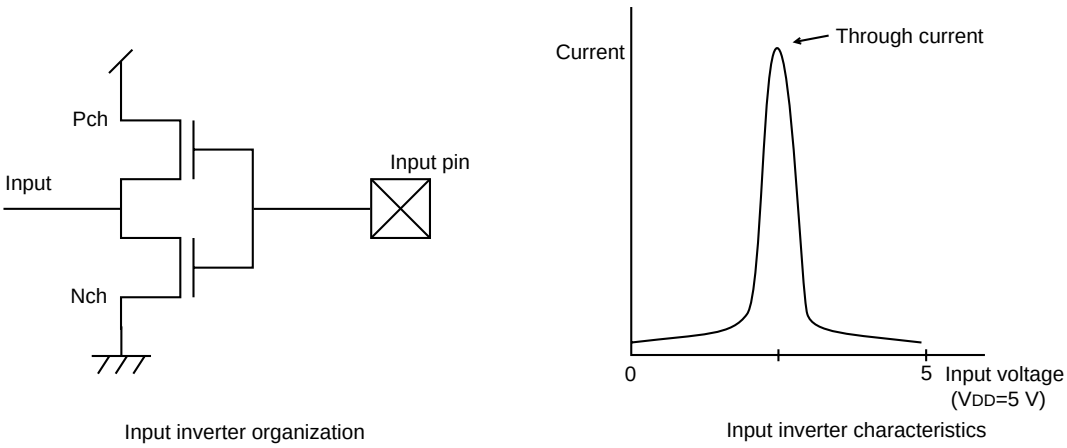


Figure 1-6-3 Input Inverter Organization and Characteristics

■Unused pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor : output off) at reset, to stabilize input, set some 10 kΩ resistor to be pull-up or pull-down. If the output is on at reset, set them open.

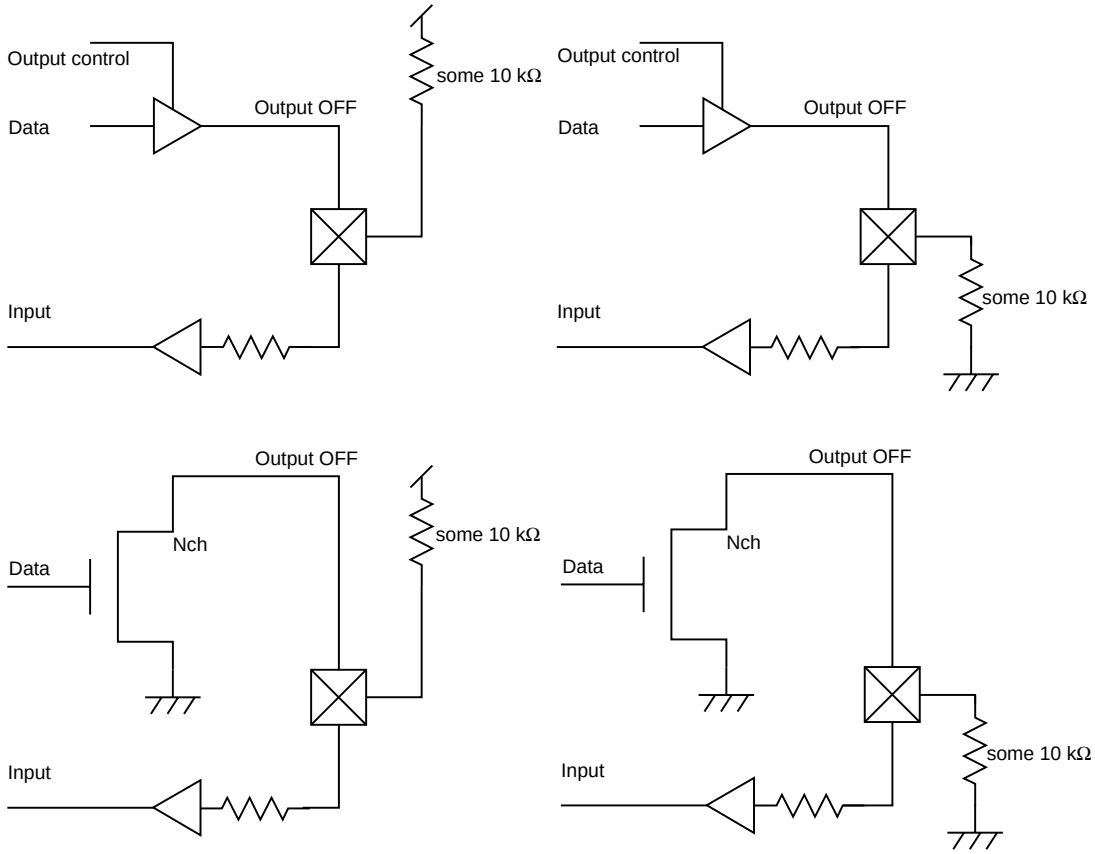


Figure 1-6-4 Unused I/O pins (high impedance output at reset)

1-6-3 Power Supply

■The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed the destruction of microcontroller by a large current flow could be occurred.

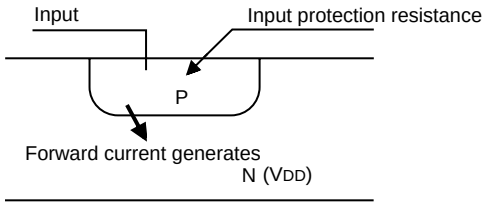
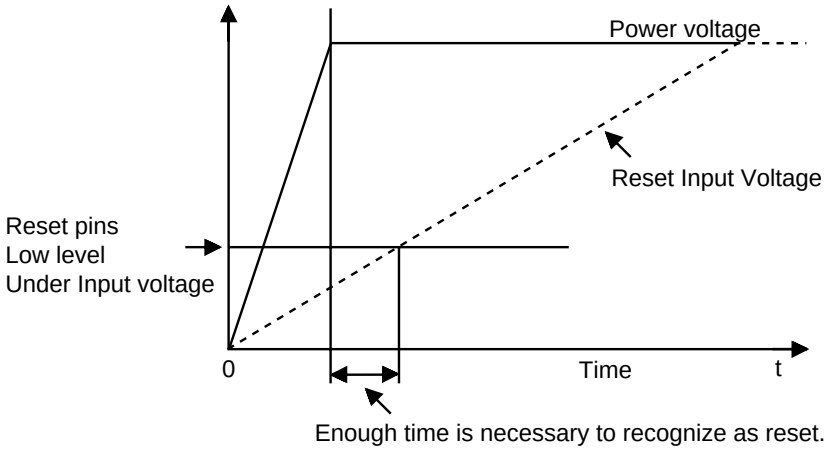


Figure 1-6-5 VDD and Input Pin Voltage

■The Relation between VDD and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time before rising , in order to be recognized as a reset signal.



[☞ Chapter 2. 2-6-1 Reset Operation]

Figure 1-6-6 Power Supply and Reset Input Voltage

1-6-4 Power Supply Circuit

■Cautions for Setting Circuits with V_{DD}

The MOS logic such a microcomputer is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver. Figure 1-6-6 shows an example for a circuit with V_{DD} (Emitter follower type).

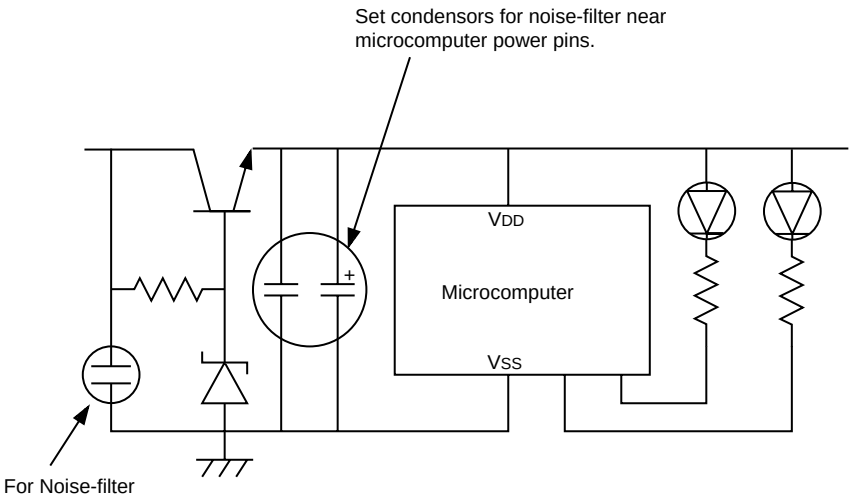


Figure 1-6-7 An Example for a Circuit of V_{DD} Supply (Emitter follower type)

1-6-5 Oscillator

Ceramic or crystal oscillator can be used with this LSI's oscillation clock.

■Recommended oscillator

Figure 1-6-8 shows basic configuration of ceramic oscillator connecion, and table 1-6-1 shows recommended oscillator and the circuit constants.

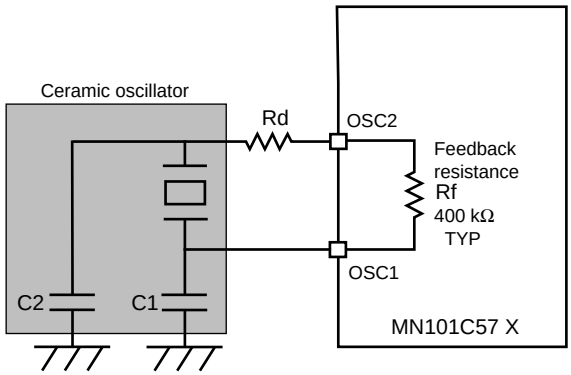


Figure 1-6-8 Basic Configuration of Ceramic Oscillator Connection

Table 1-6-1 Recommended Ceramic Oscillators and the Circuit Constants
(MATSUSHITA ELECTRONIC COMPONENTS CO.,LTD.)

Frequency	Part number	Recommended circuit constant	
		Load capacity C1=C2	Dumping resistance Rd (Ω)
20 MHz	EFOMC2005A(T)4	33 pF ± 5 pF(built-in)	-
8.38 MHz	EFOS8384E(B)5	33 pF ± 5 pF(built-in)	-
	EFOMC8384A(T)4	33 pF ± 5 pF(built-in)	-
4.19 MHz	EFOS4194E(B)5	33 pF ± 5 pF(built-in)	-
	EFOMC4194A(T)4	33 pF ± 5 pF(built-in)	-
2 MHz	EFOS2004A(T)4	33 pF ± 5 pF(built-in)	-
	EFOS2004E(B)5	33 pF ± 5 pF(built-in)	-

Manufacturer : MATSUSHITA ELECTRONIC COMPONENTS CO.,LTD.
Contact to : CERAMIC BUSINESS UNIT
LCR DEVICE COMPANY
MATSUSHITA ELECTRONIC COMPONENTS CO.,LTD.
URL : http://www.maco.panasonic.co.jp/htm-binl/maco/index.html

Table 1-6-2 Recommended Ceramic Oscillators and the Circuit Constants
(TOYAMA MURATA MANUFACTURING CO., LTD.)

Frequency	Part number	Recommended circuit constant	
		Load capacity C1=C2	Dumping resistance Rd (Ω)
20 MHz	CSTCW20M0X51-R0	6 pF(built-in)	-
	CSTCG20M0V51-R0	5 pF(built-in)	-
	CSALS20M0X53-B0	7 pF	-
8.38 MHz	CSTCE8M38G55-R0	33 pF(built-in)	-
	CSTLS8M38G56-B0	47 pF(built-in)	-
4.19 MHz	CSTCR4M19G55-R0	39 pF(built-in)	-
	CSTLS4M19G56-B0	47 pF(built-in)	-
2 MHz	CSTCC2M00G56-R0	47 pF(built-in)	-
	CSTLS2M00G56-B0	47 pF(built-in)	-

Manufacturer : TOYAMA MURATA MANUFACTURING CO., LTD.
Contact to : TOYAMA MURATA MANUFACTURING CO., LTD.
Product Engineering Service Section 1
Planning Department
Piezoelectronic Components Group.
TEL : 076-429-1221 (switchboard)

Above recommended ranges are result obtained from unit oscillating evaluation of this LSI.
After evaluate the actual oscillating on the target board, dumping resistance may be set, if necessary.

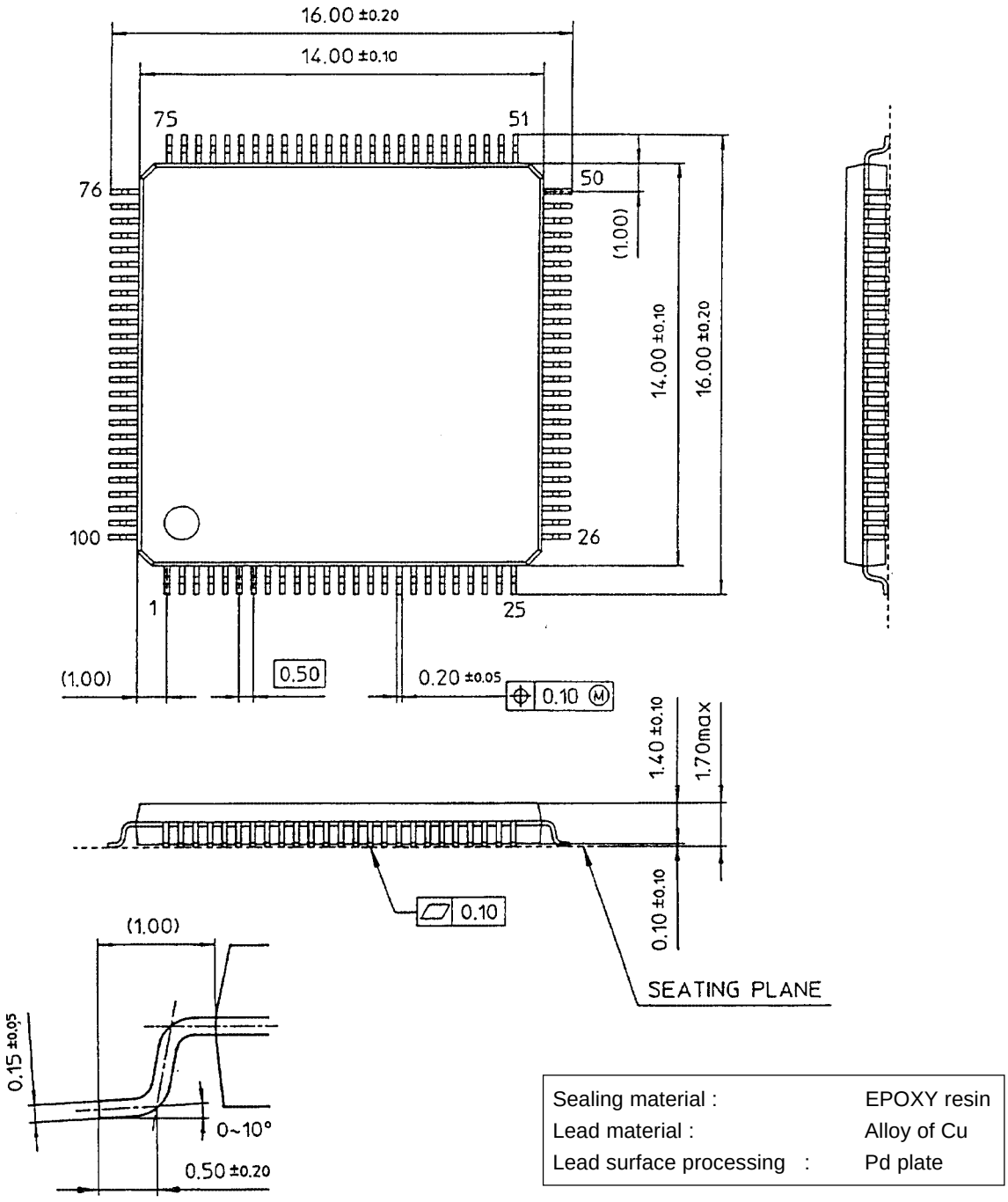
We do not evaluate oscillating of crystal oscillator on this LSI. Set the circuit constant as is recommendation of the oscillator manufacturer.

Circuit constant of each ceramic or crystal oscillator, which is connected to OSC1/OSC2 or XI/XO, differs depending on stray capacitance of the oscillator and the system circuit. Therefore, consult the oscillator manufacturer for the proper circuit constant.

1-7 Package Dimension

Package Code : LQFP100-P-1414

Units : mm



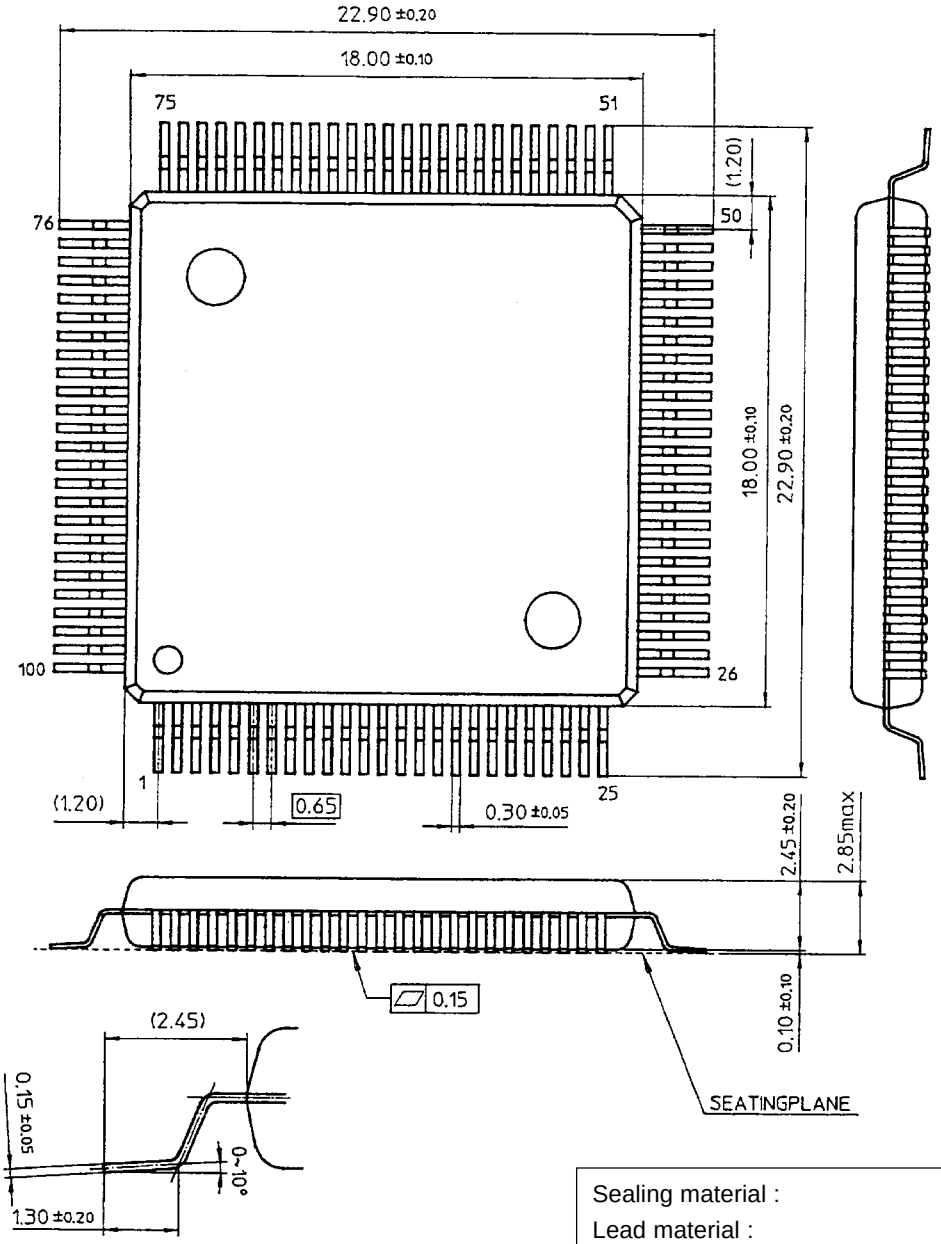
Sealing material :	EPOXY resin
Lead material :	Alloy of Cu
Lead surface processing :	Pd plate

Figure 1-7-1 100-Pin LQFP

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales office.

Package Code : QFP100-P-1818B

Units : mm



Sealing material :	EPOXY resin
Lead material :	Alloy of Cu
Lead surface processing :	Pd plate

Figure 1-7-2 100-Pin QFP

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales office.

1-8 Operation Mode Check List

Date:

SE No.

Model Name	MN101C57

Customer		Countersign	

1. Supply voltage operating range

CPU Operation	Used	Unused	Supply Voltage during Operation
At High Speed OSC1 Operation			V to V
At Low Speed XI Operation			V to V
At HALT0			V to V
At HALT1			V to V
At STOP			V to V

2. Type and frequency of oscillation input

Type	System Clock OSC1 Input	Timer Clock XI Input
External Clock		
Crystal		
Ceramic		
Frequency	MHz	kHz
Unused		

3. System operating clock

OSC1 Only	
Switching OSC1 to XI	

4. Oscillation divider Settieng

Normal mode		Slow mode	
1 divide		2 divide	
2 divide		8 divide	
4 divide		32 divide	
8 divide			
16 divide			
32 divide			
64 divide			

5. LCD display mode

LCD Unused	
Static	
1/2 duty , 1/2 bias	
1/3 duty , 1/3 bias	
1/4 duty , 1/3 bias	

6. LCD power supply

Internal divider resistor	At high pressure		V_{LC1}= V
	At low pressure		V_{LC1}= V
External divider resistor (At R= kW)			V_{LC1}= V

When placing an order for masks, please present this document.

Chapter 2 Basic CPU

2-1 Overview

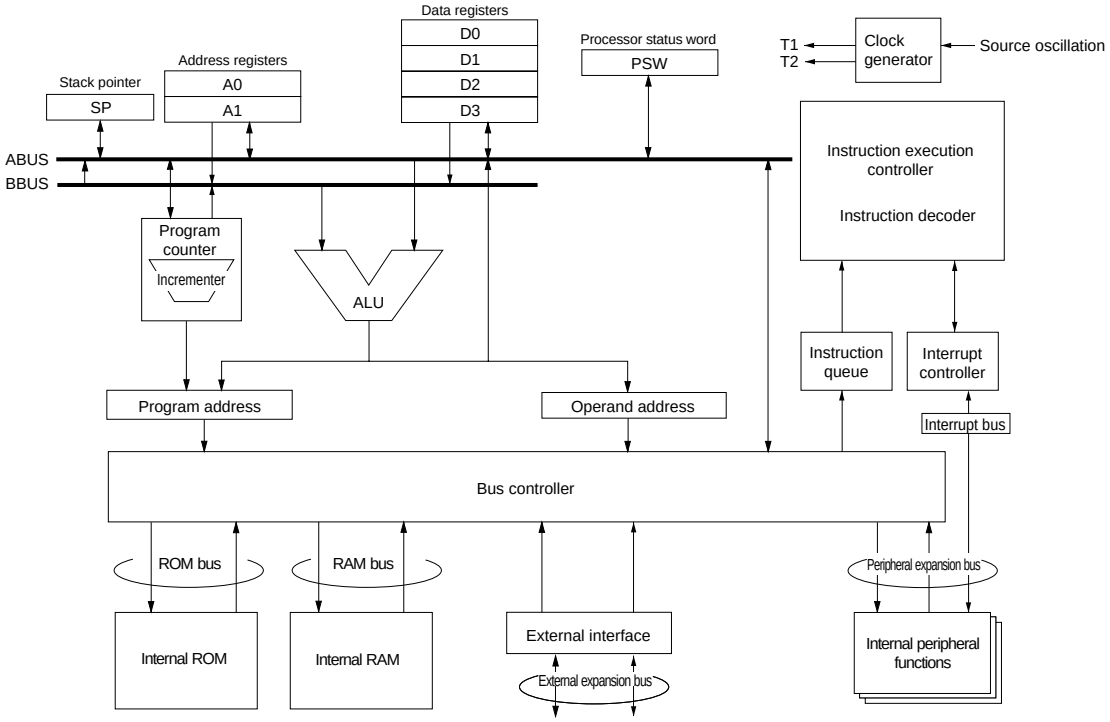
The MN101C series has a flexible optimized hardware configuration as an embedded microcomputer and a simple, efficient instruction set for both economy and speed. Specific features are as follows:

1. Minimized code sizes with instruction lengths based on 4-bit increments
   The series keeps code sizes down by adopting a basic instruction length of one byte and variable word lengths based on 4-bit increments. As a result, the series minimizes code sizes in spite of its simple instruction set limiting data transfers to and from memory to load/store operations.
2. Minimum instruction execution time of one cycle in this LSI is 100 ns .
3. Minimized register set that simplifies the architecture and supports C language
   The instruction set has been determined, depending on the size and capacity of hardware, after an analysis of embedded application programing code and creation code by C language compiler. Therefore, the set is simple instruction using the minimal register set required for C language compiler. [☞ MN101C LSI User's Manual" (Architecture Instructions)]

Table 2-1-1 Basic Specifications

Structure	Load / store architecture	
	Six registers	Data : 8-bit x 4 Address : 16-bit x 2
	Other	PC : 19-bit PSW : 8-bit SP : 16-bit
Instructions	Number of instructions	37
	Addressing modes	9
	Instruction length	Basic portion : 1 byte (min.) Extended portion : 0.5-byte x n (0≤n≤9)
Basic performance	Internal operating frequency (max)	10 MHz
	Instruction execution	Min. 1 cycle
	Inter-register operation	Min. 2 cycles
	Load / store	Min. 2 cycles
	Conditional branch	2 to 3 cycles
Pipeline	3-stage (instruction fetch, decode, execution)	
Address space	256 KB (max. 64 KB for data)	
	Instruction / data common space	
External bus	Address	18-bit (max.)
	Data	8-bit
	Minimum bus cycle	1 clock (100 ns)
Interrupt	Vector interrupt	3 interrupt levels
Low-power dissipation mode	STOP mode	
	HALT mode	

2-1-1 Block Diagram



Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic resonator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores up to 2 bytes of pre-fetched instructions.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ALU	Executes arithmetic operations, logic operations, shift operations, and calculates operand addresses for register relative indirect addressing mode.
Internal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Stores the addresses specifying memory for data transfer. Stores the base address for register relative indirect addressing mode.
Data register	Holds data for operations. Two 8-bit registers can be connected to form a 16-bit register.
Interrupt controller	Detects interrupt requests from peripheral functions and requests CPU shift to interrupt processing.
Bus controller	Controls connection of CPU internal bus and CPU external bus. Includes bus usage arbitration function.
Internal peripheral functions	Includes peripheral functions (timer, serial interface, A/D converter, D/A converter, etc.). Peripheral functions vary with model.

Figure 2-1-1 Block Diagram and Function

2-1-2 CPU Control Registers

This LSI locates the peripheral circuit registers in memory space (x'03F00' to x'03FFF') with memory-mapped I/O. CPU control registers are also located in this memory space.

Table 2-1-2 CPU Control Registers

Address	Registers	R/W	Function
X'3F00'	CPUM	R/W*1	CPU mode control register
X'3F01'	MEMCTR	R/W	Memory control register
X'3F0A'	Reserved		
X'3F0B'	Reserved		
X'3F0D'	Reserved		
X'3FE0'	Reserved (for debugger)		
X'3FE1'	NMICR	R/W	Non maskable interrupt control register [☞ Chapter 3]
X'3FE2' to X'3FFE'	xxxICR	R/W	Mascable interrupt control register [☞ Chapter 3]
X'3FFF'	Reserved (For reading out interrupt vector data in interrupt process)		

* Part of the register is only readable

2-1-3 Instruction Execution Controller

The instruction execution controller consists of four blocks: memory, instruction queue, instruction registers, and instruction decoder.

Instructions are fetched in 1-byte units, and temporarily stored in the 2-byte instruction queue. Transfer is made in 1-byte or half-byte units from the instruction queue to the instruction register to be decoded by the instruction decoder.

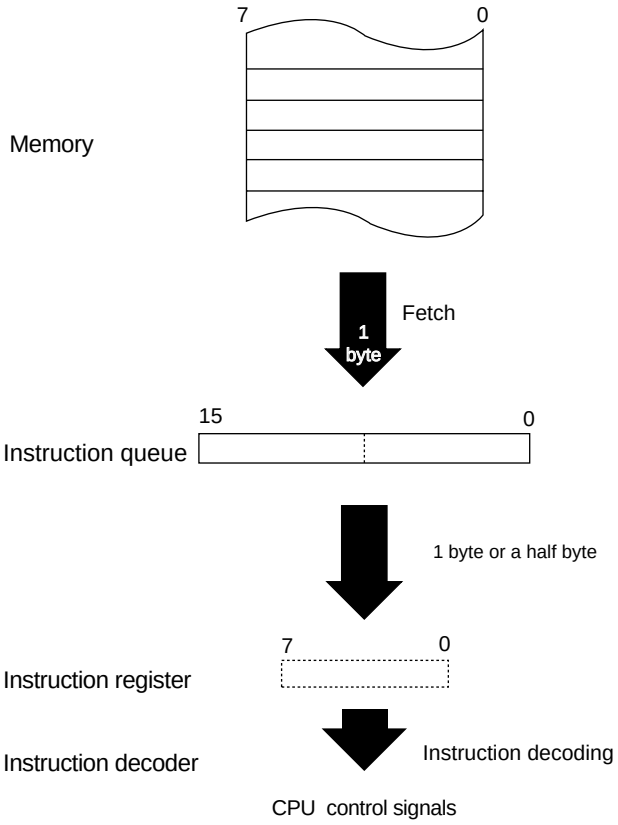


Figure 2-1-2 Instruction Execution Controller Configuration

2-1-4 Pipeline Process

Pipeline process means that reading and decoding are executed at the same time on different instructions, which are given nonstop. Pipeline process realizes speedy processing of consective instructions/ executions. This process is executed with instruction queue and instruction decoder.

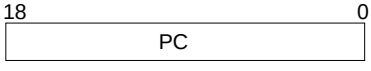
Instruction queue is buffer that fetches the second instruction in advance. That is controlled to fetch the next instruction when instruction queue is empty at each cycle on execution. At the last cycle of instruction execution, the first word (operation code) of executed instruction is stored to instruction register. At that time, the next operand or operation code is fetched to instruction queue, so that the next instruction can be executed immediately, even if register direct (da) or immediate (imm) are needed at the first cycle of the next instruction execution. But on some other instruction such a branch instruction, instruction queue becomes empty on the time that the next operation code to be executed is stored to instruction register at the last cycle. Therefore, only when instruction queue is empty, and direct address (da) or immediate data (imm) are needed, instruction queue keeps waiting for a cycle.

Instruction queue is controlled automatically by hardware so that there is no need to control by software. But when instruction execution time is estimated, operation of instruction queue should be into consideration. Instruction decoder generates control signal at each cycle of instruction execution by micro program control. Instruction decoder uses pipeline process to decode instruction queue at one cycle before control signal is needed.

2-1-5 Registers for Address

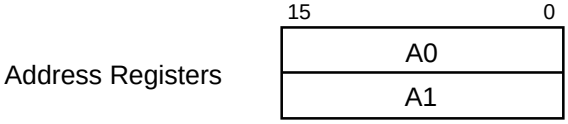
Registers for address include program counter (PC), address registers (A0, A1), and stack pointer (SP).

■Program Counter (PC)
This register gives the address of the currently executing instruction. It is 19 bits wide to provide access to a 256 KB address space in half byte(4-bit increments). The LSB of the program counter is used to indicate half byte instruction. The program counter after reset is stored from the value of vector table at the address of 4000.



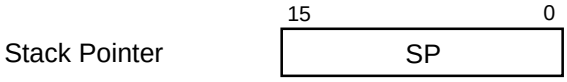
■Address Registers (A0, A1)

These registers are used as address pointers specifying data locations in memory. They support the operations involved in address calculations (i.e. addition, subtraction and comparison). Those pointers are 2-byte data. Transfers between these registers and memory are always in 16-bit units. Either odd or even address can be transferred. At reset, the value of address register is undefined.



■Stack Pointer (SP)

This register gives the address of the byte at the top of the stack. It is decremented during push operations and incremented during pop operations. Ar reset, the value of SP is undefined.



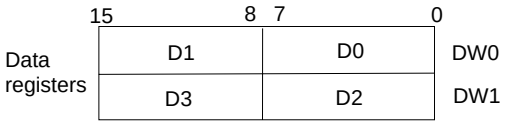
2-1-6 Registers for Operation

Registers for operation include four data registers (D0, D1, D2, D3).

■Data Registers (D0, D1, D2, D3)

Data registers D0 to D3 are 8-bit general-purpose registers that support all arithmetic, logical and shift operations. All registers can be used for data transfers with memory.

The four data registers may be paired to form the 16-bit data registers DW0 (D0+D1) and DW1 (D2+D3). At reset, the value of Dn is undefined.



2-1-7 Processor Status Word

Processor status word (PSW) is an 8-bit register that stores flags for operation results, interrupt mask level, and maskable interrupt enable. PSW is automatically pushed onto the stack when an interrupt occurs and is automatically popped when the interrupt service routine returns.

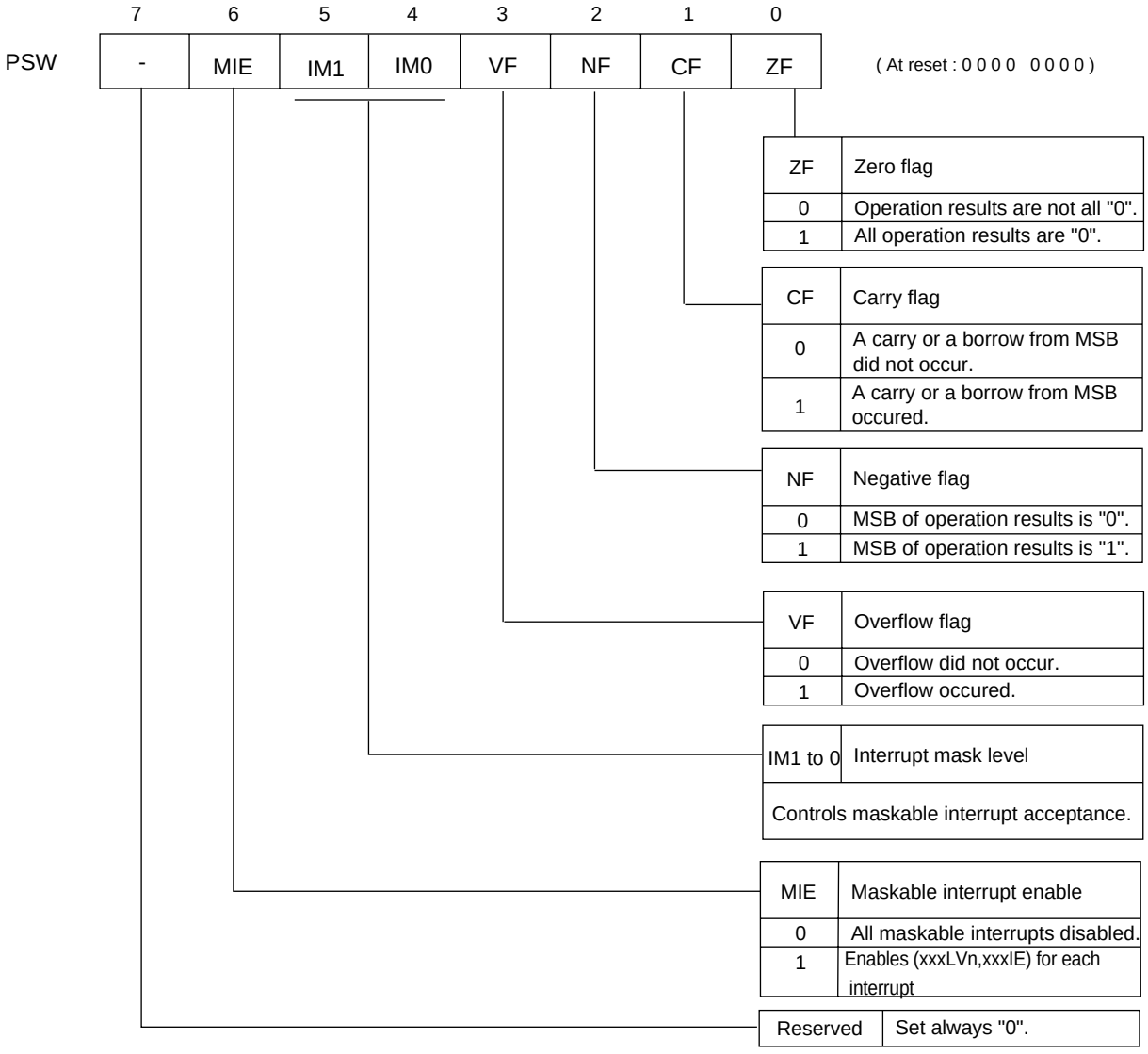

7 6 5 4 3 2 1 0
PSW
- MIE IM1 IM0 VF NF CF ZF
(At reset : 0 0 0 0 0 0 0 0)
ZF Zero flag
0 Operation results are not all "0".
1 All operation results are "0".
CF Carry flag
0 A carry or a borrow from MSB did not occur.
1 A carry or a borrow from MSB occured.
NF Negative flag
0 MSB of operation results is "0".
1 MSB of operation results is "1".
VF Overflow flag
0 Overflow did not occur.
1 Overflow occured.
IM1 to 0 Interrupt mask level
Controls maskable interrupt acceptance.
MIE Maskable interrupt enable
0 All maskable interrupts disabled.
1 Enables (xxxLVn,xxxIE) for each interrupt
Reserved Set always "0".

Figure 2-1-3 Processor Status Word(PSW)

■Zero Flag (ZF)
Zero flag (ZF) is set to "1", when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0".

■Carry Flag (CF)
Carry flag (CF) is set to "1", when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0", when no carry or borrow occurs.

■Negative Flag (NF)
Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value.

■Overflow Flag (VF)
Overflow flag (VF) is set to "1", when the arithmetic operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0".
Overflow flag is used to handle a signed value.

■Interrupt Mask Level (IM1 and IM0)
Interrupt mask level (IM1 and IM0) controls the maskable interrupt acceptance in accordance with the interrupt factor interrupt priority for the interrupt control circuit in the CPU. The two-bit control flag defines levels '0' to '3'. Level 0 is the highest mask level. The interrupt request will be accepted only when the level set in the interrupt level flag (xxxLVn) of the interrupt control register (xxxICR) is higher than the interrupt mask level. When the interrupt is accepted, the level is reset to IM1-IM0, and interrupts whose mask levels are the same or lower are rejected during the accepted interrupt processing.

Table 2-1-3 Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt levels
	IM1	IM0		
Mask level 0	0	0	High	Non-maskable interrupt (NMI) only
Mask level 1	0	1	.	NMI, Level 0
Mask level 2	1	0	.	NMI, Level 0 to 1
Mask level 3	1	1	Low	NMI, Level 0 to 2

■Maskable Interrupt Enable (MIE)
Maskable interrupt enable flag (MIE) enables/disables acceptance of maskable interrupts by the CPU's internal interrupt acceptance circuit. A '1' enables maskable interrupts; a '0' disables all maskable interrupts regardless of the interrupt mask level (IM1-IM0) setting in PSW.
This flag is not changed by interrupts.

2-1-8 Addressing Modes

This LSI supports the nine addressing modes.

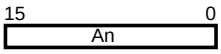
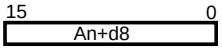
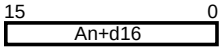
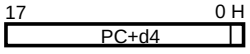
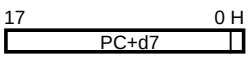
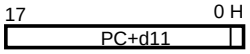
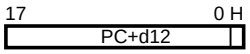
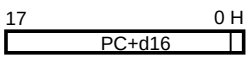
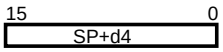
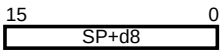
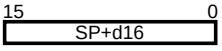
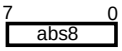
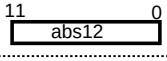
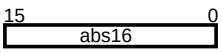
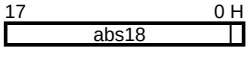
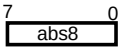
Each instruction uses a combination of the following addressing modes.

1) Register direct
2) Immediate
3) Register indirect
4) Register relative indirect
5) Stack relative indirect
6) Absolute
7) RAM short
8) I/O short
9) Handy

These addressing modes are well-suited for C language compilers. All of the addressing modes can be used for data transfer instructions. In modes that allow half-byte addressing, the relative value can be specified in half-byte (4-bit) increments, so that instruction length can be shorter. Handy addressing reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combining handy addresssing with absolute addressing reduces code size. For transfer data between memory, 7 addressing modes ; register indirect, register relative indirect, stack relative indirect, absolute, RAM short, I/O short, handy can be used. For operation instruction, register direct and immediate can be used. Refer to instruction's manual for the MN101C series.

This LSI is designed for 8-bit data access. It is possible to tranfer data in 16-bit increments by specifying either all odd or all even addresses.

Table 2-1-4 Addressing Modes

Addressing mode		Effective address	Explanation
Register direct	Dn/DWn An/SP PSW	-	Directly specifies the register. Only internal registers can be specified.
Immediate	imm4/imm8 imm16	-	Directly specifies the operand or mask value appended to the instruction code.
Register indirect	(An)		Specifies the address using an address register.
Register relative indirect	(d8, An)		Specifies the address using an address register with 8-bit displacement.
	(d16, An)		Specifies the address using an address register with 16-bit displacement.
	(d4, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 4-bit displacement and H bit.
	(d7, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 7-bit displacement and H bit.
	(d11, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 11-bit displacement and H bit.
	(d12, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 12-bit displacement and H bit.
	(d16, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 16-bit displacement and H bit.
Stack relative indirect	(d4, SP)		Specifies the address using the stack pointer with 4-bit displacement.
	(d8, SP)		Specifies the address using the stack pointer with 8-bit displacement.
	(d16, SP)		Specifies the address using the stack pointer with 16-bit displacement.
Absolute	(abs8)		Specifies the address using the operand value appended to the instruction code. Optimum operand length can be used to specify the address.
	(abs12)		
	(abs16)		
	(abs18) (branch instructions only)	 * 1	
RAM short	(abs8)		Specifies an 8-bit offset from the address x'00000'.
I/O short	(io8)		Specifies an 8-bit offset from the top address (x'03F00') of the special function register area.
Handy	(HA)	-	Reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combined use with absolute addressing reduces code size.

* 1 H: half-byte bit

2-2 Memory Space

2-2-1 Memory Mode

ROM is the read only area and RAM is the memory area which contains readable/writable data. In addition to these, peripheral resources such as memory-mapped special registers are allocated. The MN101C series supports one memory mode (single chip mode) in its memory model.

Table 2-2-1 Memory Mode Setup

Memory mode	MMOD pin	EXMEM flag in (MEMCTR register)	EXADV3 to 1 flag in (EXADV register)
Single chip mode	L	0	1/0

2-2-2 Single-chip Mode

In single-chip mode, the system consists of only internal memory. This is the optimized memory model and allows construction of systems with the highest performance.

The single-chip mode uses only internal ROM and internal RAM. The MN101C series devices offer up to 12 KB of RAM and up to 240 KB of ROM. This LSI offers 2048 bytes of RAM and 64 KB of ROM.

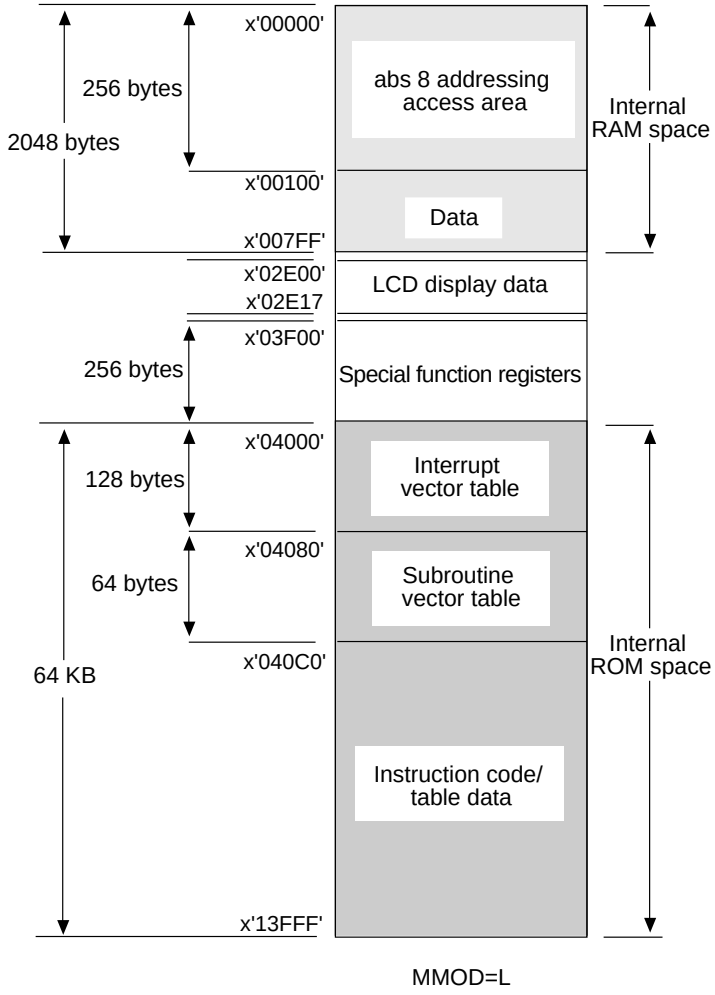


Figure 2-2-1 Single-chip Mode

*Differs depending upon the model. [☞ Table 2-2-2. Internal ROM / Internal RAM]

Table 2-2-2. Internal ROM / Internal RAM

Model	Internal RAM		Internal ROM	
	Address	bytes	Address	bytes
MN101C57C	X'00000' to X'007FF'	2048	X'04000' to X'0FFFF'	48 K
MN101C57D	X'00000' to X'007FF'	2048	X'04000' to X'13FFF'	64 K

The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before it is used.

2-2-3 Memory Expansion Mode

The MN101C series can be connected with external ROM, RAM and other external devices for operation. In memory expansion mode, memory space can be expanded exteriorly using internal ROM and RAM.

The memory expansion mode is set by assigning EXMEM flag (bp4) of the memory control register (MEMCTR) on single chip mode. Address output to pins can be controlled with pins A8 to A17 of the address expansion control register(EXADV) by setteng the bit7 to bit5 of the EXADV.
Memory areas can be externally expanded as follows :

ROM: x'20000'-x'3FFFF' (128 KB)
RAM: x'02F00'-x'03EFF' (4 KB)

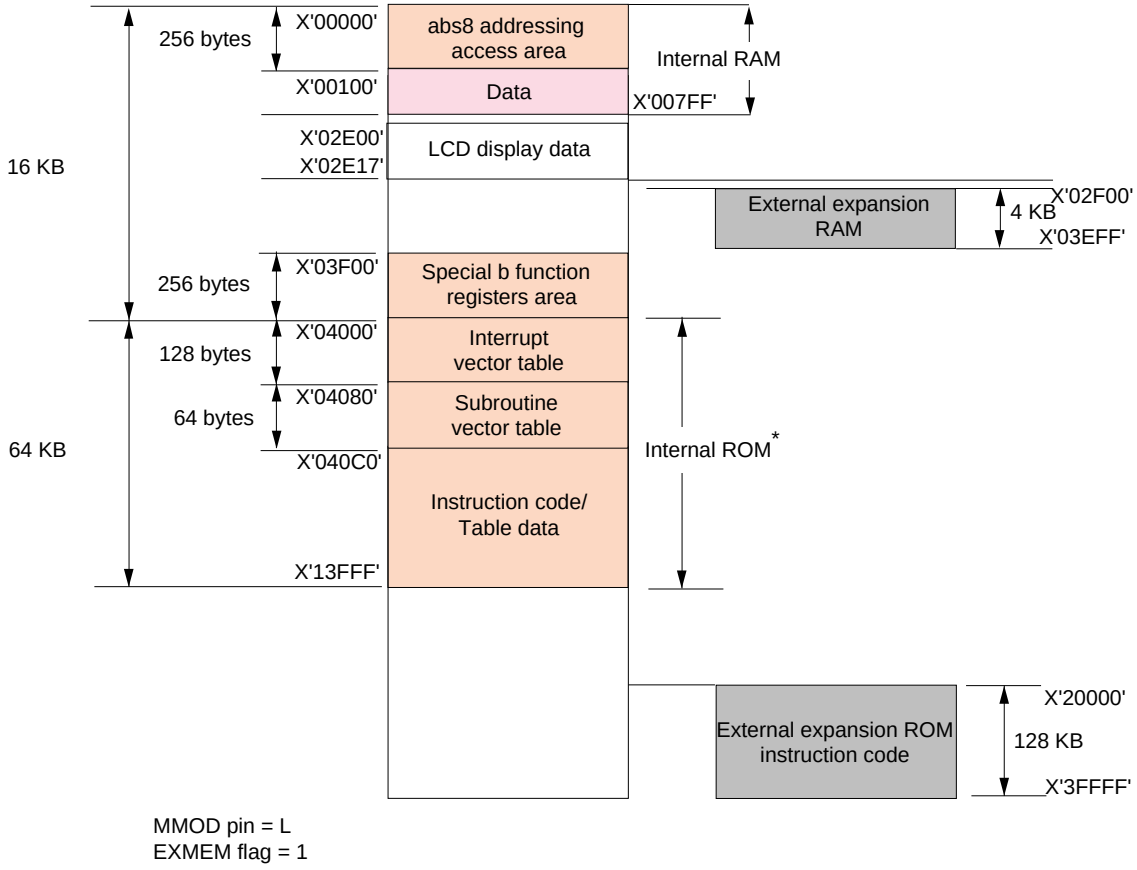


Figure 2-2-2 Memory Expansion Mode

Differs depending upon the model. [☞ Table 2-2-2. Internal ROM / Internal RAM]

> The value of internal RAM is uncertain when power is applied to it.
> It needs to be initialized before it is used.

2-2-4 Special Function Registers

The MN101C series locates the special registers (I/O spaces) at the address x'03F00' to x'03FFF' in memory space. The special function registers of this LSI are located as shown below.

Table 2-2-3 Register Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
03F0X	CPUM	MEMCTR	WDCTR	DLYCTR	Reserved		ACTMD			Reserved	Reserved	Reserved		Reserved	EXADV	Reserved
03F1X	P0OUT	P1OUT	P2OUT	P3OUT	P4OUT	P5OUT	P6OUT	P7OUT	P8OUT	P9OUT	PAOUT	PBOUT			P4SYO	
03F2X	P0IN	P1IN	P2IN	P3IN	P4IN	P5IN	P6IN	P7IN	P8IN	P9IN	PAIN	PBIN			FLOAT	P1OMD
03F3X	P0DIR	P1DIR		P3DIR	P4DIR	P5DIR	P6DIR	P7DIR	P8DIR	P9DIR	PAIDIR	PBDIR	PAIMD	PBIMD	P4IMD	P5OMD
03F4X	P0PLUD	P1PLUD	P2PLU	P3PLU	P4PLU	P5PLU	P6PLU	P7PLU	P8PLU	P9PLU	PAPLUD	PBPLUD		P0IMD		P5LED
03F5X	TM0BC	TM1BC	TM0OC	TM1OC	TM0MD	TM1MD	CK0MD	CK1MD	TM2BC	TM3BC	TM2OC	TM3OC	TM2MD	TM3MD	CK2MD	CK3MD
03F6X									TM6BC	TM6OC	TM6MD	TBCLR	TM7MD3	TM8MD3	RMCTR	PSCMD
03F7X	TM7BCL	TM7BCH	TM7OC1L	TM7OC1H	TM7PR1L	TM7PR1H	TM7ICL	TM7ICH	TM7MD1	TM7MD2	TM7OC2L	TM7OC2H	TM7PR2L	TM7PR2H	TM7DEAD PR1	TM7DEAD PR2
03F8X	TM8BCL	TM8BCH	TM8OC1L	TM8OC1H	TM8PR1L	TM8PR1H	TM8ICL	TM8ICH	TM8MD1	TM8MD2	TM8OC2L	TM8OC2H	TM8PR2L	TM8PR2H	NFCTR	EDGDT
03F9X	SC0MD0	SC0MD1	SC0MD2	SC0MD3	RXBUF0	TXBUF0	SC0ODC	SC0CKS								
03FAX	SC2MD0	SC2MD1	SC2TRB				SC2ODC	SC2CKS								
03FBX	ANCTR0	ANCTR1	ANCTR2	ANBUF0	ANBUF1							Reserved	Reserved	Reserved	Reserved	Reserved
03FCX						RMCTR1	RMCTR2	RMCTR3	RMCTR4	RMCTR5	RMCTR6	RMCTR7	RMCTR8	RMDAT1	RMDAT2	RMICTR
03FDX	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		LCDMD1	LCDMD2	LCCTR1	LCCTR2	LCCTR3	LCCTR4	Reserved
03FEX	Reserved	NMICR	IRQ0ICR	IRQ1ICR	IRQ2ICR	IRQ3ICR	IRQ4ICR	IRQ5ICR	IRQ6ICR	TM0ICR	TM1ICR	TM2ICR	TM3ICR	IRQ7ICR	RMICR	TM6ICR
03FFX	TBICR	TM7ICR	TM7OC2 ICR	TM8ICR	TM8OC2 ICR	SC0RICR	SC0TICR		SC2ICR		ADICR					

	CPU mode, memory control	I/O ports			
		PORT output	PORT input	I/O mode control	Registor control
		Timer control			
		Serial I/F control			
		A/D control			
		Remote control			
		LCD control			
		Interrupt control			

2-3 Bus Interface

2-3-1 Bus Controller

The MN101C series provides separate buses to the internal memory and internal peripheral circuits to reduce bus line loads and thus realize faster operation.

There are four such buses: ROM bus, RAM bus, and peripheral expansion bus (I/O bus). They are connected to the internal ROM, internal RAM, internal peripheral circuits, and external interfaces respectively. A functional block diagram of the bus controller is given below.

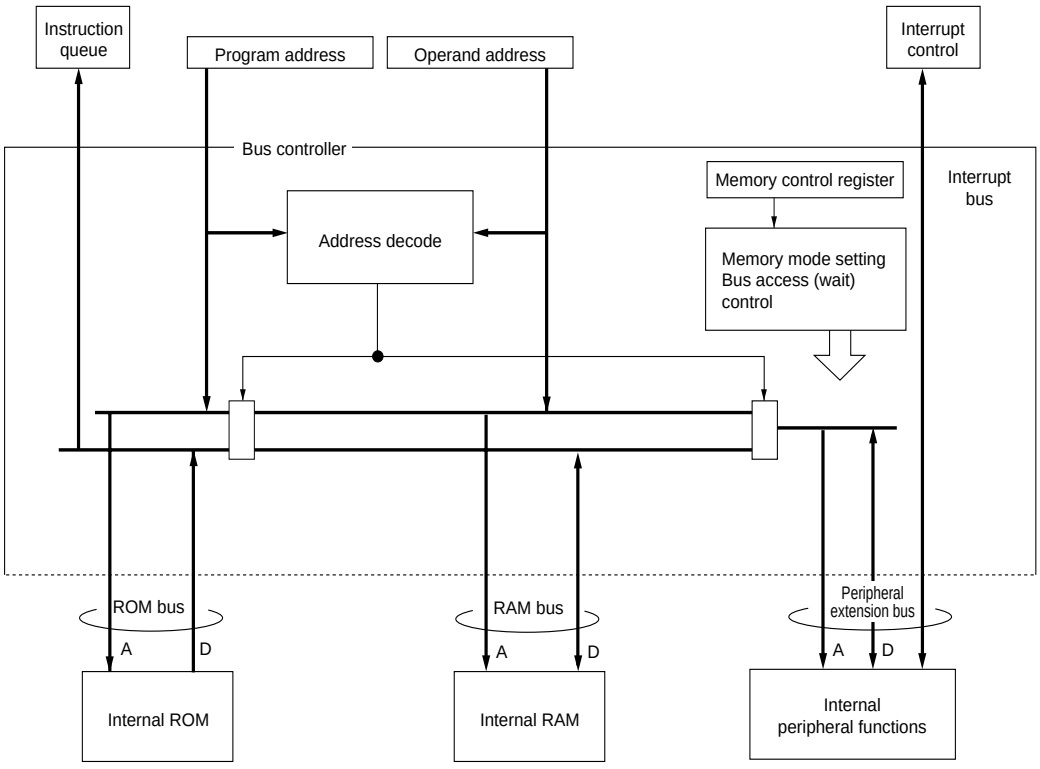


Figure 2-3-1 Functional Block Diagram of the Bus Controller

2-3-2 Control Registers

Bus interface is controlled by two registers : the memory control register (MEMCTR) and the expansion address register (EXADV).

■Memory Control Register (MEMCTR)

	7	6	5	4	3	2	1	0
MEMCTR	IOW1	IOW0	IVBM	EXMEM	EXWH	IRWE	EXW1	EXW0

(At reset : 1 1 0 0 1 0 1 1)

EXW1 to 0	Fixed wait cycles	Bus cycle at 20 MHz oscillation
0 0	No wait cycles	100 ns
0 1	1 wait cycle	150 ns
1 0	2 wait cycles	200 ns
1 1	3 wait cycles	250 ns

IRWE	Software write enable flag for interrupt request flag
0	Software write disable Even if data is written to each interrupt control register (xxxICR), the state of the interrupt request flag (xxxIR) will not change.
1	Software write enable

EXWH	Fixed wait cycle mode or handshake mode
0	Handshake mode
1	Fixed wait cycle mode

EXMEM	Memory expansion mode
0	Do not expand external memory
1	Expand external memory

IVBM	Base address setting for interrupt vector table
0	Interrupt vector base = x'04000'
1	Interrupt vector base = x'00100'

IOW1 to 0	Wait cycles when accessing special register area	Bus cycle at 20 MHz oscillation
0 0	No wait cycles	100 ns
0 1	1 wait cycle	150 ns
1 0	2 wait cycles	200 ns
1 1	3 wait cycles	250 ns

Figure 2-3-2 Memory Control Register (MEMCTR: x'3F01' R/W)

The IOW1-IOW0 wait settings affect accesses to the special registers located at the addresses x'3F00'-x'3FFF'. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is a function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. For this LSI, wait cycle setting is not always necessary. Select "no-wait cycle" for high performance system construction.

■Expansion Address Control Register (EXADV)

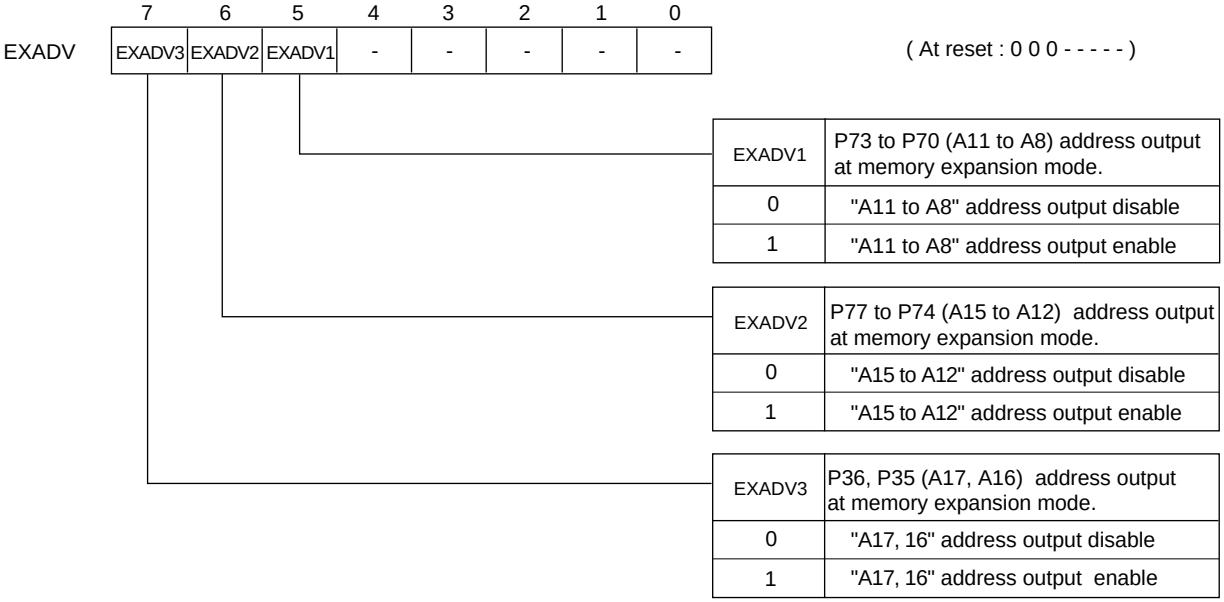

7 6 5 4 3 2 1 0
EXADV
EXADV3 EXADV2 EXADV1 - - - - -
(At reset : 0 0 0 - - - - -)
EXADV1 P73 to P70 (A11 to A8) address output at memory expansion mode.
0 "A11 to A8" address output disable
1 "A11 to A8" address output enable
EXADV2 P77 to P74 (A15 to A12) address output at memory expansion mode.
0 "A15 to A12" address output disable
1 "A15 to A12" address output enable
EXADV3 P36, P35 (A17, A16) address output at memory expansion mode.
0 "A17, 16" address output disable
1 "A17, 16" address output enable

Figure 2-3-3 Expansion Address Control Register (EXADV : x'03F0E', R/W)

In memory expansion mode, unused address pins can be used as general ports.

2-3-3 Fixed Wait Cycle Mode

This mode accesses ROM, RAM, or other low-speed devices connected to the external expansion bus by inserting the number of wait cycles specified in the external fixed wait counter (EXW) field of the memory control register (MEMCTR).

Fixed wait cycle mode automatically inserts the number of wait cycles specified by the fixed wait counter (EXW1-0) in the MEMCTR. After reset, MEMCTR specifies the fixed wait cycle to three wait cycles. To change to handshake mode or to use a different number, modify the appropriate bits in MEMCTR.

2-3-4 Handshake Mode

Handshake mode uses the interlock control method in the data transfer sequence, with transfer enable signals (NRE, NWE) and a data acknowledge signal (NDK).

Handshake mode adjusts the wait cycle for each external device that has a different access speed when the DK generation circuit is provided for each device. CPU of this LSI keeps waiting until the reception of data acknowledge signal to ensure sufficient wait time so that external device can reception data with no error.

[☞ "MN101C LSI User's Manual" (Architecture Instructions)]

On handshake mode, watchdog timer can be used to detect NDK's not being received. The reception of NDK is waited until the non-maskable interrupt is generated by the overflow of watchdog timer.

■Access Timing with No Wait Cycles

The NRE or NWE timing is determined based on OSC2. However, since the delay from OSC1 to RE or WE varies depending upon the product, use NRE or NWE as the reference when synchronizing with other devices. Operation timing is same as the timing when the division factor is 2 (The beginning state after releasing reset) at NORMAL mode (OSC high speed oscillation selection).

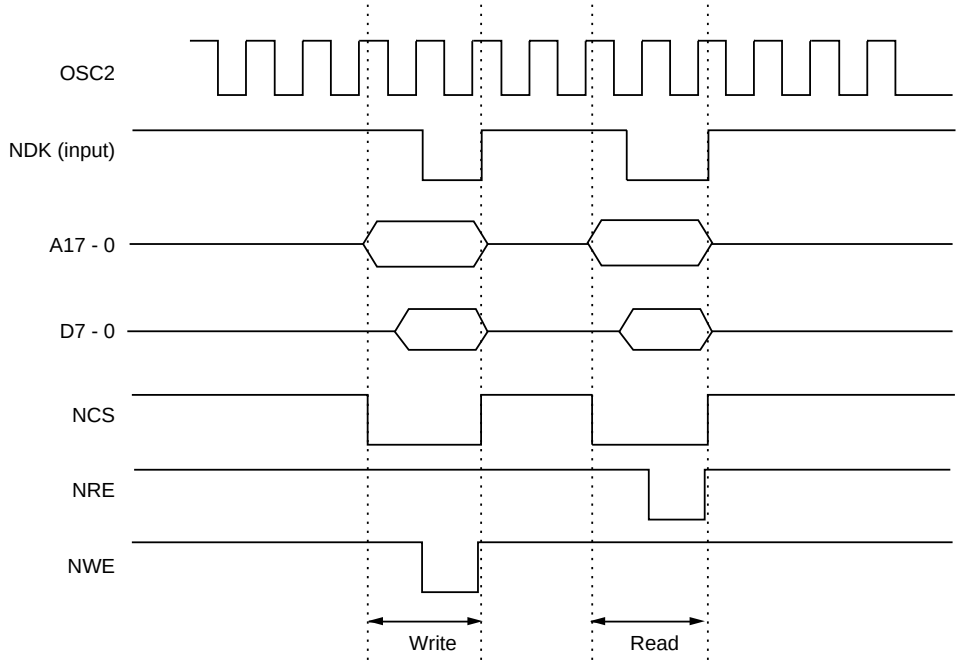


Figure 2-3-4 ROM and RAM Access Timing with No Wait Cycles

■Access Timing with 1 Wait Cycle

Access timing with 2 or 3 wait cycles follows the same pattern. The latter part of the cycle is extended and the timing is the same.

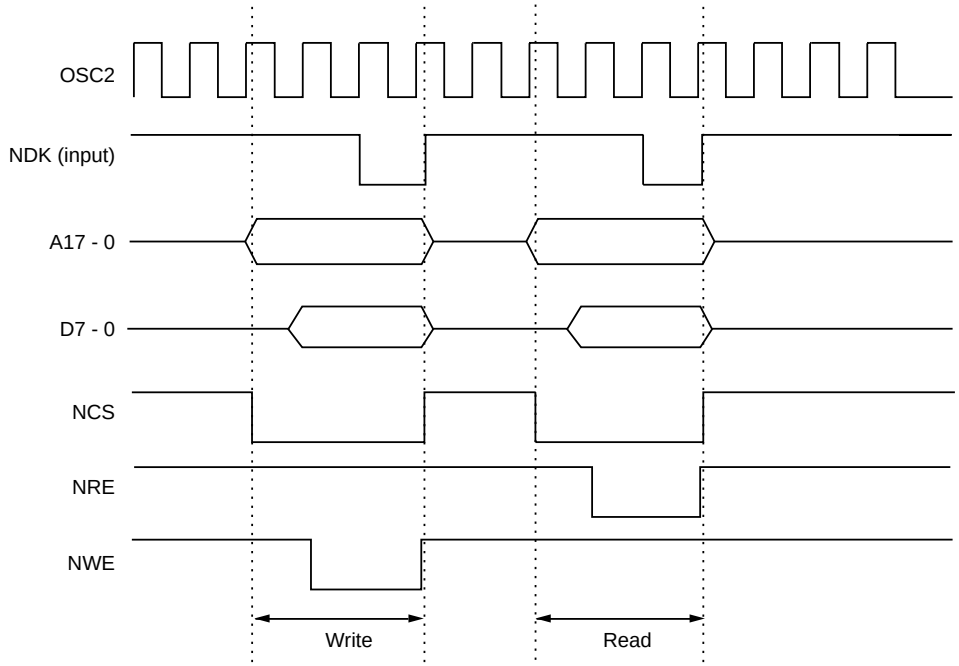


Figure 2-3-5 ROM and RAM Access Timing with 1 Wait Cycle

2-3-5 External Memory Connection Example

■SRAM Connection Example

This example shows connection to SRAM.

The external expansion RAM area is 'X02F00' to 'X03EFF'.

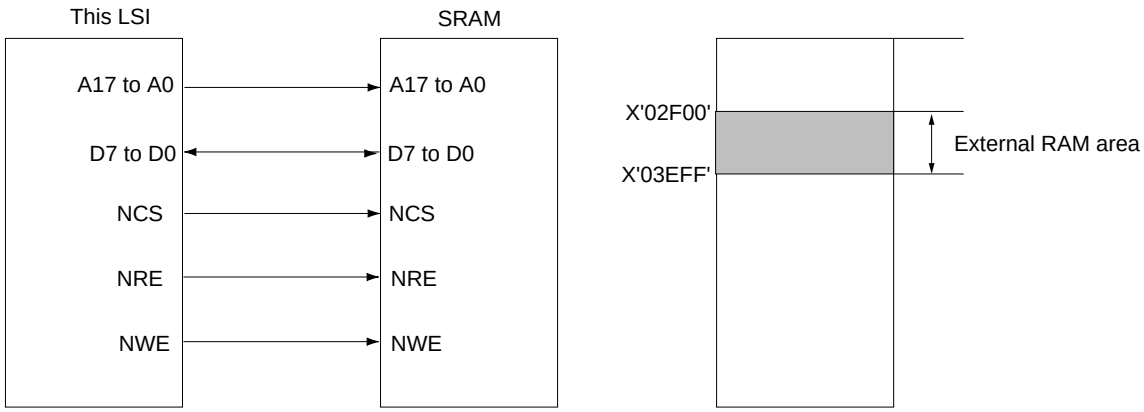


Figure 2-3-6 SRAM Connection Example

2-4 Standby Function

2-4-1 Outline

This LSI has two sets of system clock oscillator pins (high- and low-frequency) for two CPU operating modes (NORMAL and SLOW), each with two standby modes (HALT and STOP).

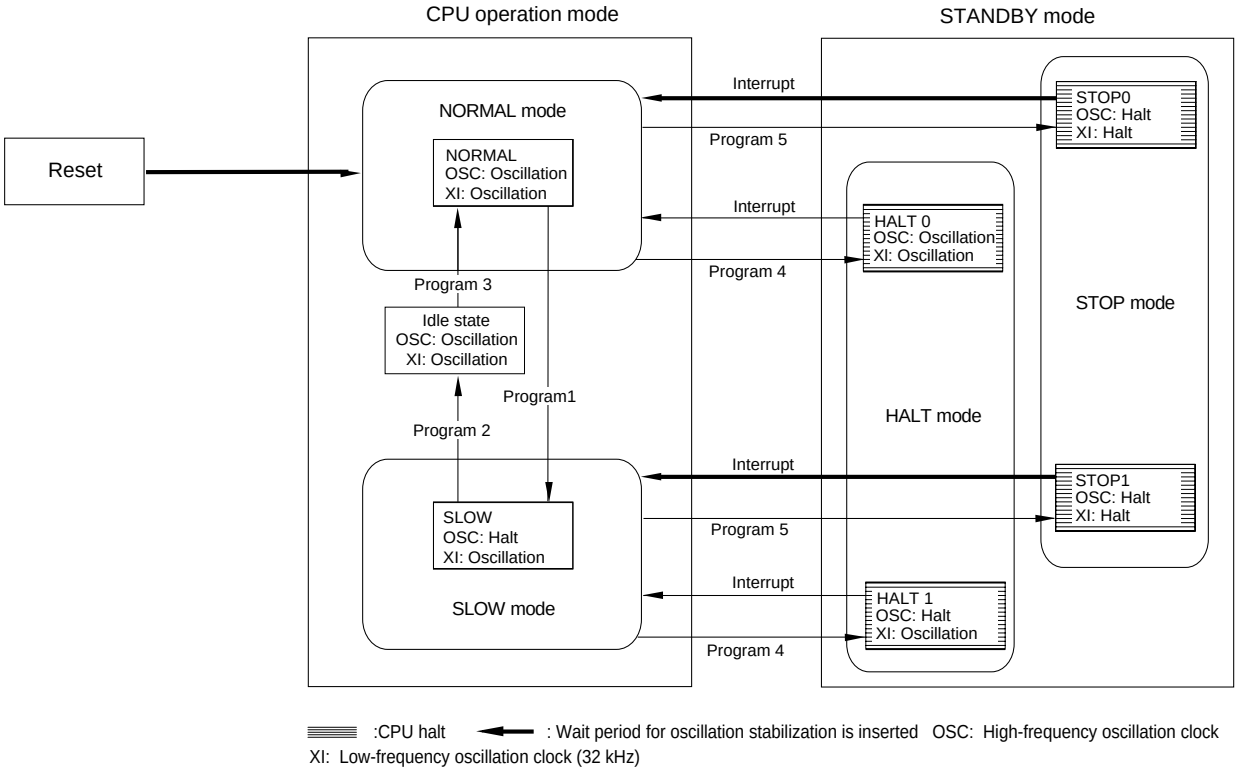


Figure 2-4-1 Transition Between Operation Modes

■HALT Modes (HALT0, HALT1)

– The CPU stops operating. But both of the oscillators remain operational in HALT0 and only the high-frequency oscillator stops operating in HALT1.
– An interrupt returns the CPU to the previous CPU operating mode that is, to NORMAL from HALT0 or to SLOW from HALT1.

■STOP Modes (STOP0, STOP1)

– The CPU and both of the oscillators stop operating.
– An interrupt restarts the oscillators and, after allowing time for them to stabilize, returns the CPU to the previous CPU operating mode - that is, to NORMAL from STOP0 or to SLOW from STOP1.

■SLOW Mode

– This mode executes the software programs using the low-frequency clock. Since the high-frequency oscillator is turned off, the device consumes less power while executing the software.

■IDLE Mode

– This mode allows time for the high-frequency oscillator to stabilize when the software is changing from SLOW to NORMAL mode.

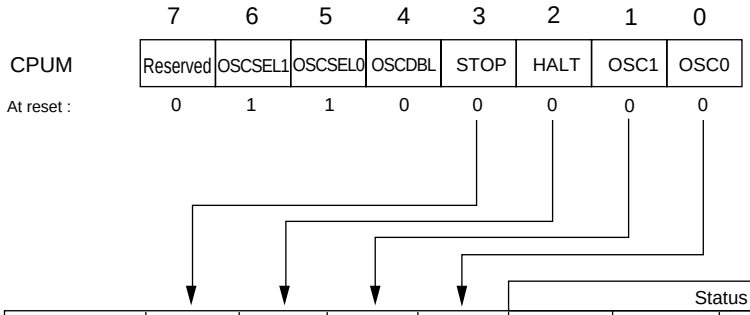
To reduce power dissipation in STOP and HALT modes, it is necessary to check the stability of both the output current from pins and port level of input pins. For output pins, the output level should match the external level or direction control should be changed to input mode. For input pins, the external level should be fixed.

This LSI has two system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and XI is for low-frequency operation (SLOW mode). Transition between NORMAL and SLOW modes or to standby mode is controlled by the CPU mode control register (CPUM). Reset and interrupts are the return factors from standby mode. A wait period is inserted for oscillation stabilization at reset and when returning from STOP mode, but not when returning from HALT mode. High/low-frequency oscillation mode is automatically returned to the same state as existed before entering standby mode.

To stabilize the synchronization at the moment of switching clock speed between high-frequency and low-frequency, high-frequency oscillation frequency (fosc) should be set to 2.5 times or higher frequency than the low-frequency oscillation frequency (fx).

2-4-2 CPU Mode Control Register

Transition to other modes is controlled by operating the related flags in the CPU mode control register (CPUM).



Operation mode	STOP	HALT	OSC1	OSC0	Status: OSCI /OSCO	Status: XI/XO	Status: System clock	Status: CPU
NORMAL	0	0	0	0	Oscillation	Oscillation	OSCI	Operating
IDLE	0	0	0	1	Oscillation	Oscillation	XI	Operating
SLOW	0	0	1	1	Halt	Oscillation	XI	Operating
HALT0	0	1	0	0	Oscillation	Oscillation	OSCI	Halt
HALT1	0	1	1	1	Halt	Oscillation	XI	Halt
STOP0	1	0	0	0	Halt	Halt	Halt	Halt
STOP1	1	0	1	1	Halt	Halt	Halt	Halt

Figure 2-4-2 Operating Mode Control and Clock Oscillation On/Off (CPUM : x'3F00', R/W)

The procedure for transition from NORMAL to HALT or STOP mode is shown below.

(1) If the return factor is a maskable interrupt, set the MIE flag in the PSW to "1" and set the interrupt mask (IM) to a level permitting acceptance of the interrupt.
(2) Clear the interrupt request flag (xxxIR) in the maskable interrupt control register (xxxICR) , set the interrupt enable flag (xxxIE) for the return factor, and set the IE flag in the PSW.
(3) Set CPUM to HALT or STOP mode.

IRWE flag of Memory control (MEMCTR) should be set for interrupt request flag to be cleared by software.

2-4-3 Transition between SLOW and NORMAL

This LSI has two CPU operating modes, NORMAL and SLOW. Transition from SLOW to NORMAL requires passing through an idle state.

A sample program for transition from NORMAL to SLOW mode is shown below.

```
Program 1
        MOV   x'3', D0          ; Set SLOW mode.
        MOV   D0, (CPUM)
```

Transition from NORMAL to SLOW mode, when the low-frequency clock has fully stabilized, can be done by writing to the CPU mode control register. In this case, transition through the idle state is not necessary.
For transition from the SLOW to NORMAL mode, the program must maintain the idle state until high-frequency clock oscillation is fully stable. In the idle state, the CPU operates on the low-frequency clock.

This stabilization time is the same as that required after a reset, but here the program must do the counting.
We recommend selecting the oscillation stabilization interval after consulting with the oscillator manufacturer.

Sample program for transition from SLOW to NORMAL mode is shown below.

```
Program 2
                MOV         x'01', D0           ; Set IDLE mode.
                MOV         D0, (CPUM)
```

```
Program 3
        MOV   x'0B', D0     ; A loop to keep approx. 6.7 ms with low-frequency clock (32 kHz)
LOOP    ADD   -1, D0        ; operation when changed to high-frequency clock (20 MHz).
        BNE   LOOP          ;
        SUB   D0, D0        ;
        MOV   D0, (CPUM)    ;  Set NORMAL mode.
```

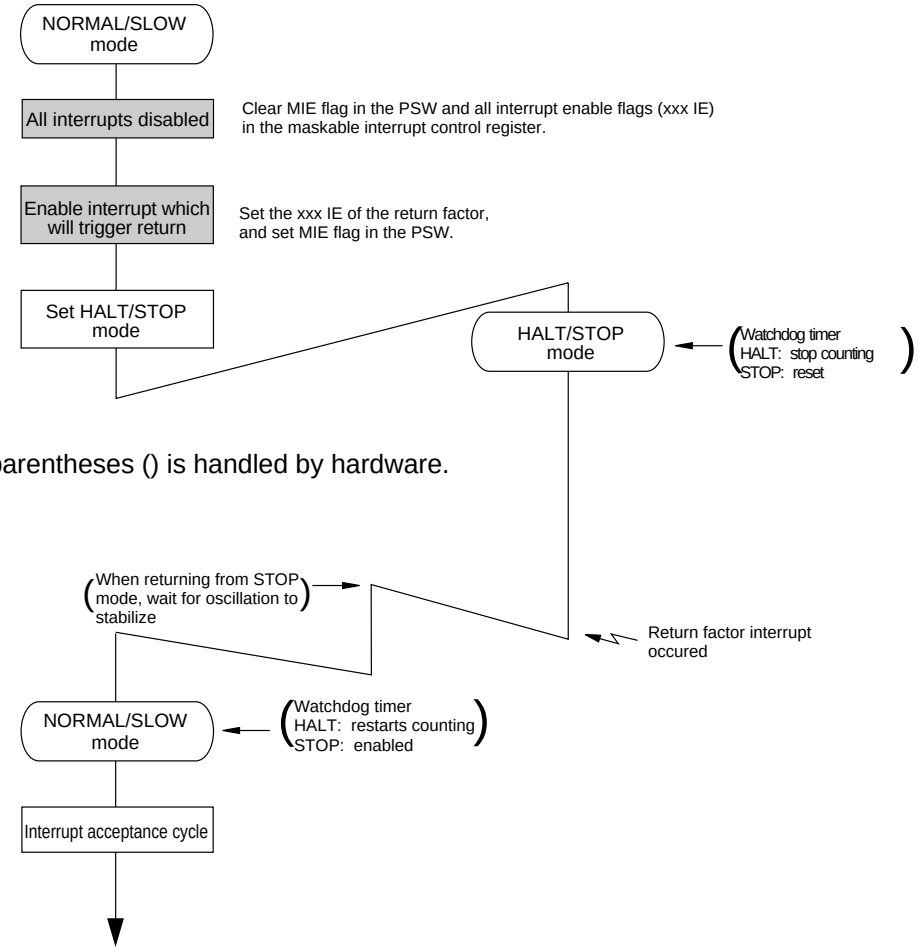
2-4-4 Transition to STANDBY Modes

The program initiates transitions from a CPU operating mode to the corresponding STANDBY (HALT/STOP) modes by specifying the new mode in the CPU mode control register (CPUM). Interrupts initiate the return.

To initiating a transition to a STANDBY mode, the program requires in advance to,

(1) Set the maskable interrupt enable flag (MIE) in the processor status word (PSW) to '0' to disable all maskable interrupts temporarily.

(2) Set the interrupt enable flags (xxxIE) in the interrupt control registers (xxxICR) to '1' or '0' to specify which interrupts do and do not initiate the return from the STANDBY mode. Set MIE '1' to enable those maskable interrupts.


NORMAL/SLOW mode
All interrupts disabled
Clear MIE flag in the PSW and all interrupt enable flags (xxx IE) in the maskable interrupt control register.
Enable interrupt which will trigger return
Set the xxx IE of the return factor, and set MIE flag in the PSW.
Set HALT/STOP mode
HALT/STOP mode
(Watchdog timer HALT: stop counting STOP: reset)
(When returning from STOP mode, wait for oscillation to stabilize)
Return factor interrupt occured
NORMAL/SLOW mode
(Watchdog timer HALT: restarts counting STOP: enabled)
Interrupt acceptance cycle

Processing inside parentheses () is handled by hardware.

Figure 2-4-3 Transition to/from STANDBY Mode

> **!** If the interrupt is enabled and interrupt priority level of the interrupt to be used is not equal to or higher than the mask level in PSW before transition to HALT or STOP mode, it is impossible to return to CPU operation mode by maskable interrupt.

■Transition to HALT modes

The system transfers from NORMAL mode to HALT0 mode, and from SLOW mode to HALT1 mode. The CPU stops operating, but the oscillators remain operational. There are two ways to leave a HALT mode: a reset or an interrupt. A reset produces a normal reset; an interrupt, an immediate return to the CPU state prior to the transition to the HALT mode. The watchdog timer, if enabled, resumes counting.

Program 4

```
        MOV     x'4',  D0      ; Set HALT mode.
        MOV     D0,  (CPUM)
        NOP                    ; After written in CPUM, some NOP
        NOP                    ; instructions (three or less) are
        NOP                    ; executed.
```

■Transition to STOP mode

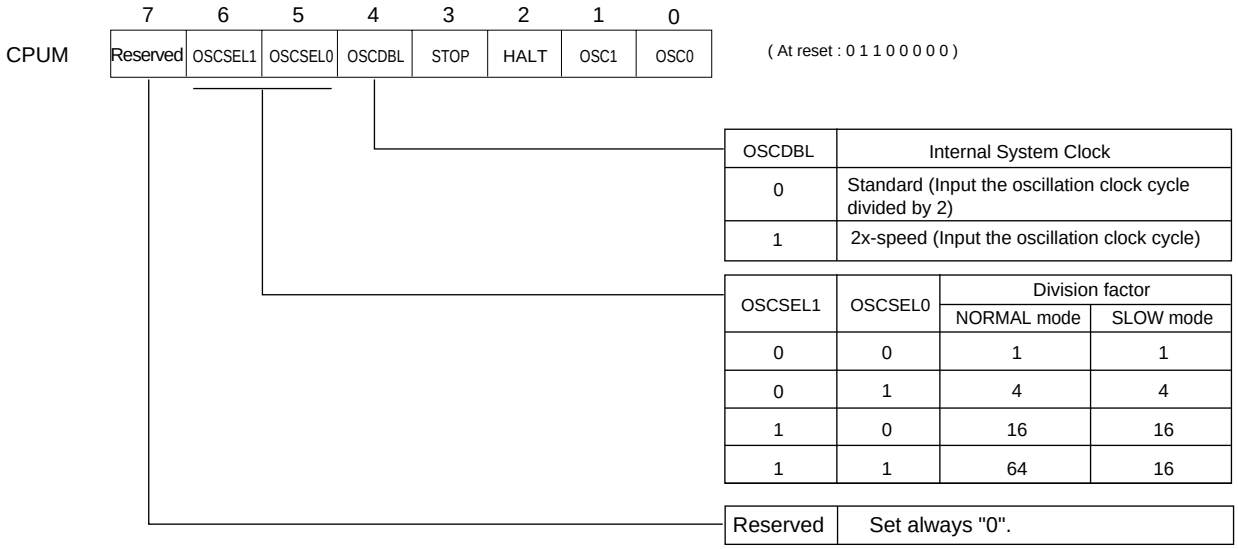
The system transfers from NORMAL mode to STOP0 mode, and from SLOW mode to STOP1 mode. In both cases, oscillation and the CPU are both halted. There are two ways to leave a STOP mode: a reset or an interrupt.

Program 5

```
        MOV     x'8',  D0      ; Set STOP mode
        MOV     D0,  (CPUM)
        NOP                    ; After written in CPUM, some NOP
        NOP                    ; instructions (three or less) are
        NOP                    ; executed.
```

2-5 Clock Switching

This LSI can select the best operation clock for system by switching clock cycle division rate through program. Division rate is determined by both flags of the CPU mode control register (CPUM). At the highest-frequency, CPU can be operated in the same clock cycle to the external clock hence providing a wider operating frequency range.



OSCDBL	Internal System Clock
0	Standard (Input the oscillation clock cycle divided by 2)
1	2x-speed (Input the oscillation clock cycle)

OSCSEL1	OSCSEL0	Division factor	
		NORMAL mode	SLOW mode
0	0	1	1
0	1	4	4
1	0	16	16
1	1	64	16

Reserved	Set always "0".

Figure 2-5-1 CPU Mode Control Register (CPUM : x'03F00', R/W)

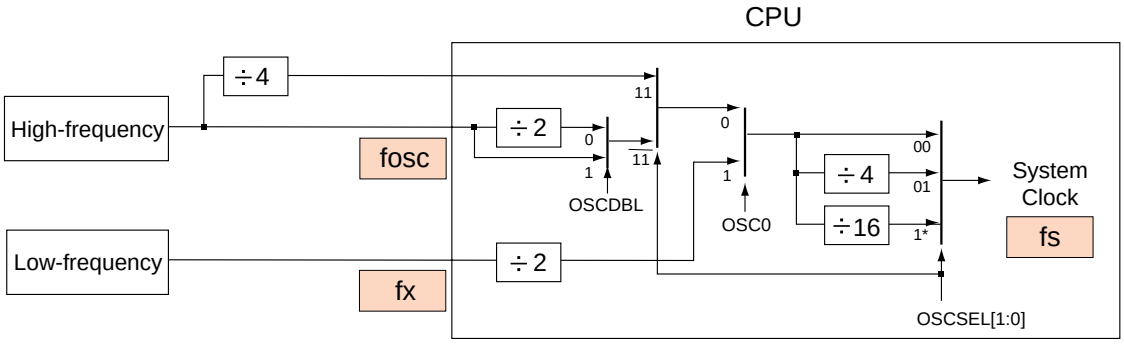


Figure 2-5-2 Clock Switching Circuit

OSCSEL1	OSCSEL0	OSCDBL	Division factor for High-frequency(OSC) Input (NORMAL mode)
0	0	0	2
0	0	1	1
0	1	0	8
0	1	1	4
1	0	0	32
1	0	1	16
1	1	0	64
1	1	1	64

Figure 2-5-3 Setting Division Rate at NORMAL mode by combination of OSCSEL and OSCDBL

OSCSEL1	OSCSEL0	Division factor for Low-frequency(XI/XO) Input (SLOW mode)
0	0	2
0	1	8
1	0	32
1	1	32

Figure 2-5-4 Setting Division Rate at SLOW mode by combination of OSCSEL

On clock switching, set each flag of OSCDBL, OSCSEL, and OSC0, individualy. Even if those flags are mapped on the same special functions register, set three times.

2-6 Reset

2-6-1 Reset operation

The CPU contents are reset and registers are initialized when the NRST pin (P27) is pulled to low.

■Initiating a Reset

There are two methods to initiate a reset.

(1) Drive the NRST pin low for at least four clock cycles.
NRST pin should be holded "low" for more than 4 clock cycles (200 ns at a 20 MHz).

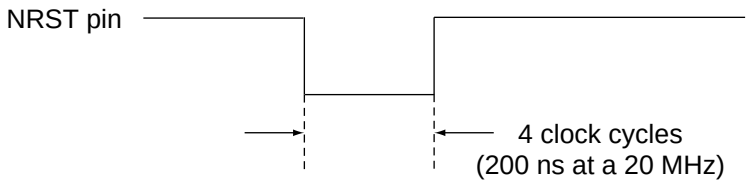


Figure 2-6-1 Minimum Reset Pulse Width

(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transfering to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.

[☞ Chapter 4. 4-4-2 Registers]

This LSI's starting mode is NORMAL mode in which high oscillation is the base clock.

When the power voltage low circuit is connected to NRST pin, circuit that gives pulse for enough low level time at sudeen unconnected. And reset can be generated even if its pulse is low level as the oscillation clock is under 4 clocks, take notice of noise.

■Sequence at Reset

(1) When reset pin comes to high level from low level, system closk starts count operation by the internal 10-bit counter (watchdog timer dual function). The period from starting its count from its overflow is called oscillation stabilization wait time.

(2) During reset, internal register and special function register are initiated.

(3) After oscillation stabilization wait time is finished, internal reset is released and program is started from the address written on x'04000' of vector table.

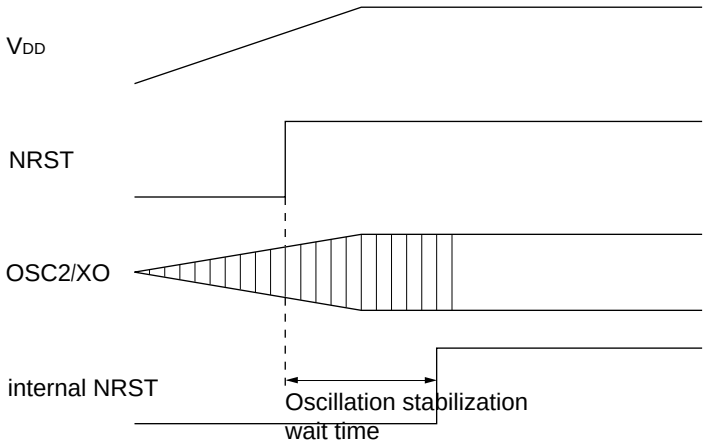


Figure 2-6-2 Reset Released Sequence

2-6-2 Oscillation Stabilization Wait time

Oscillation stabilization wait time is the period from the stop of oscillation circuit to the stablization for oscillation. Oscillaion stabilization wait time is automatically inserted at releasing from reset and at recovering from STOP mode. At recovering from STOP mode the oscillation stabilization wait time control register (DLYCTR) is set to select the oscillation stabilization wait time. At releasing from reset, oscillation stabilization wait time is fixed.

The timer that counts oscillation stabilization wait time is also used as a watchdog timer. That is used as a runaway detective timer at anytime except at releasing from reset and at recovering from STOP mode. Watchdog timer is initiated at reset and at STOP mode and starts counting from the initialize value (x'0000') when system clock (fs) is as clock source. After oscillation stabilization wait time is finished, it continues counting as a watchdog timer. [☞ Chapter 9 Watchdog timer]

■Block Diagram of Oscillation Stabilization Wait Time Function (watchdog timer)

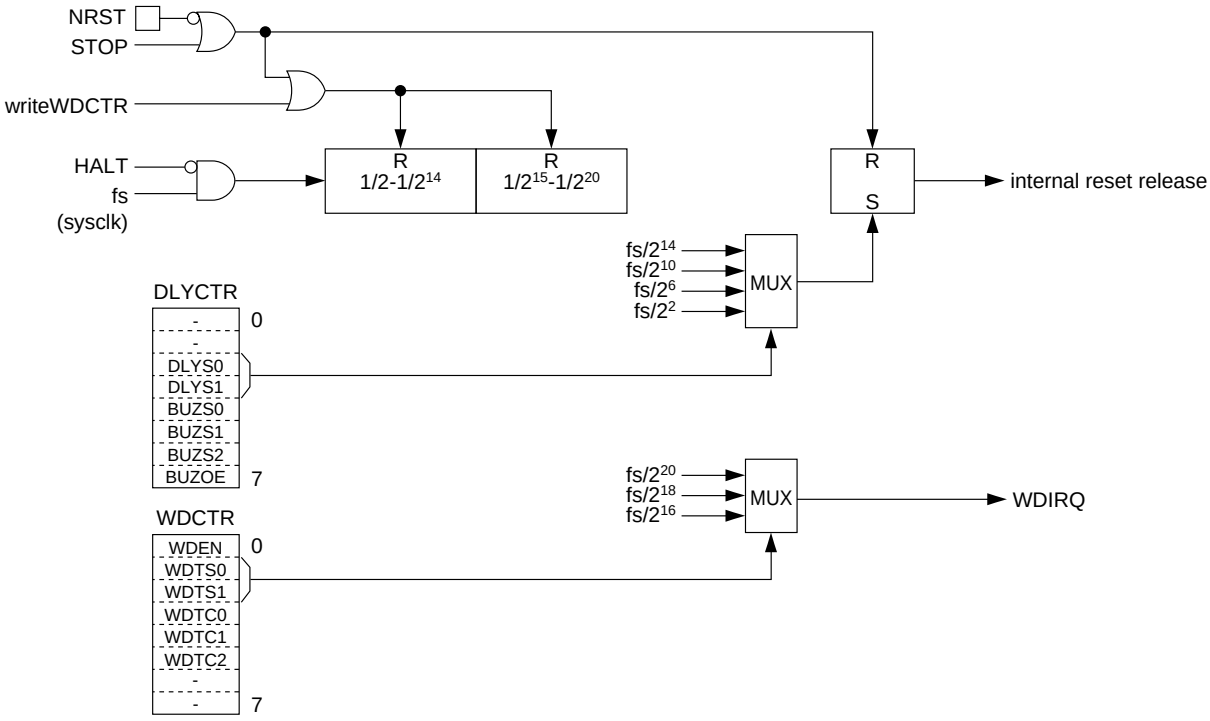
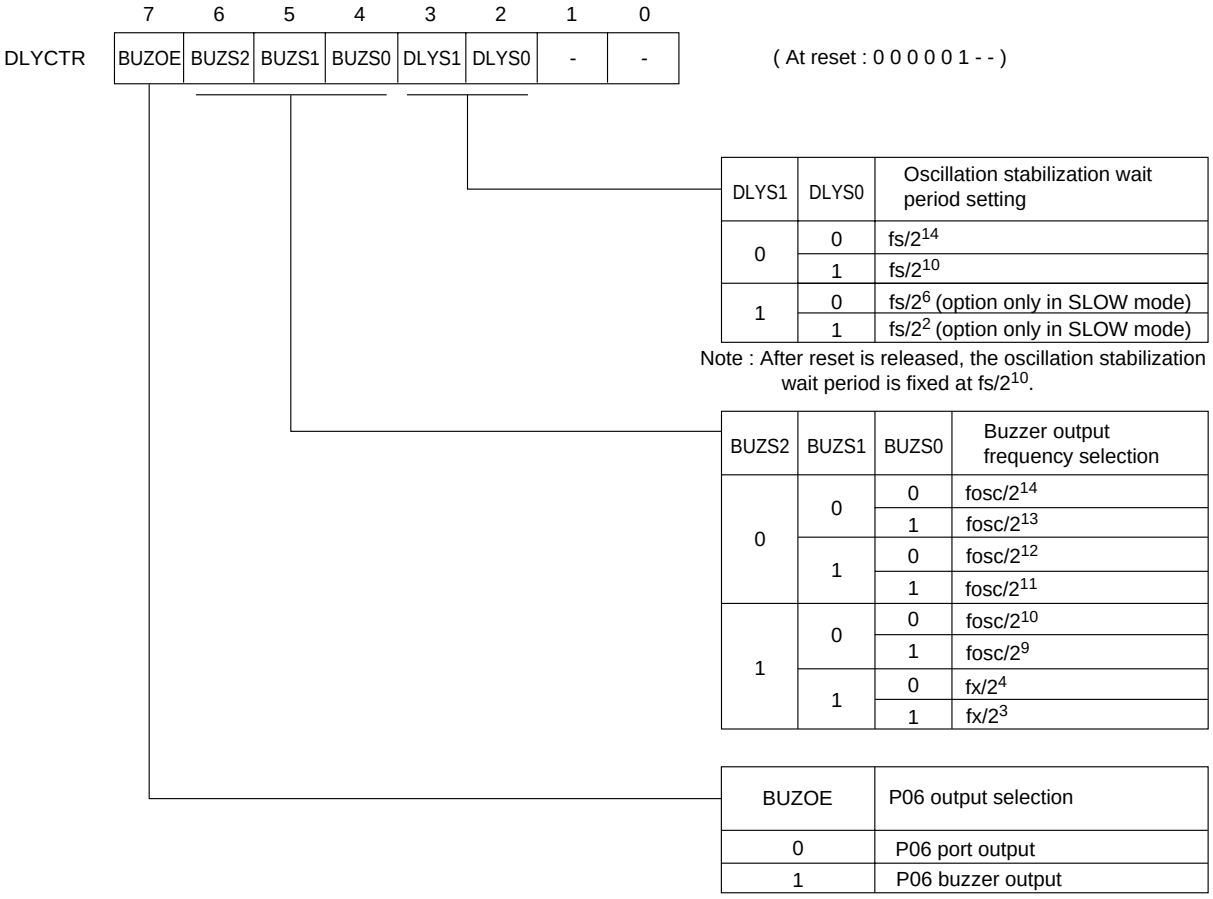


Figure 2-6-3 Block Diagram of Osillation Stabilization Wait Time Function (watchdog timer)

■Oscillation Stabilization Wait Time Control Register



DLYS1	DLYS0	Oscillation stabilization wait period setting
0	0	$fs/2^{14}$
	1	$fs/2^{10}$
1	0	$fs/2^{6}$ (option only in SLOW mode)
	1	$fs/2^{2}$ (option only in SLOW mode)

Note : After reset is released, the oscillation stabilization wait period is fixed at $fs/2^{10}$.

BUZS2	BUZS1	BUZS0	Buzzer output frequency selection
0	0	0	$fosc/2^{14}$
		1	$fosc/2^{13}$
	1	0	$fosc/2^{12}$
		1	$fosc/2^{11}$
1	0	0	$fosc/2^{10}$
		1	$fosc/2^{9}$
	1	0	$fx/2^{4}$
		1	$fx/2^{3}$

BUZOE	P06 output selection
0	P06 port output
1	P06 buzzer output

Figure 2-6-4 Osillation stabilization wait time control register (DLYCTR : x'03F03', R/W)

■Control the Osillation Stabilization Wait Time

At recovering from STOP mode, the bit 3-2 (DLYS1, DLYS0) of the oscillation stabilization wait time control register can be set to select the oscillation stabilization wait time from 2^{14}, 2^{10}, 2^{6}, 2^{2} x system clock. The DLYCTR register is also used for controlling of buzzer functions.

[☞ Chapter 10 Buzzer]

At releasing from reset, the oscillation stabilization wait time is fixed to "2^{10} x system clock". System clock is controlled through the CPU mode control register (CPUM).

Table 2-6-1 Oscillation Stabilization Wait Tim

DLYS1	DLYS0	Oscillation stabilization wait time
0	0	2^{14} x Systemclock
0	1	2^{10}x Systemclock
1	0	2^{6} x Systemclock
1	1	2^{2} x Systemclock

Chapter 3 Interrupts

3

3-1 Overview

This LSI speeds up interrupt response with circuitry that automatically loads the branch address to the corresponding interrupt service routine from an interrupt vector table : reset, non-maskable interrupts (NMI), 9 maskable peripheral interrupts, and 14 internal interrupts.

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. After the interrupt is accepted, the program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack. And an interrupts handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted. Max.12 machine cycles before execution, and max 11 machine cycles after execution.

Each interrupt has a interrupt control register, which controls the interrupts. Interrupt control register consists of the interrupt level field (LV1-0), interrupt enable flag (IE), and interrupt request flag (IR).

Interrupt request flag (IR) is set to "1" by an interrupt request, and cleared to "0" by the interrupt acceptance. This flag is managed by hardware, but can be rewritten by software.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. There is no interrupt enable flag in non-maskable interrupt (NMI). Once this interrupt request flag is set, it is accepted without any conditions. Interrupt enable flag is set in maskable interrupt. Interrupt enable flag of maskable interrupt is valid when the maskable interrupt enable flag (MIE flag) of PSW is "1".

Maskable interrupts have had vector numbers by hardware, but their priority can be changed by setting interrupts level field. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. Maskable interrupts are accepted when its level is higher than the interrupt mask level (IM1-0) of PSW. Non-maskable interrupts are always accepted, regardless of the interrupt mask level.

3-1-1 Functions

Table 3-1-1 Interrupt Functions

Interrupt type	Reset (interrupt)	Non-maskable interrupt	Maskable interrupt
Vector number	0	1	2 to 26
Table address	x'04000'	x'04004'	x'04008' to x'04068
Starting address	Address specified by vector table		
Interrupt level	-	-	Can be set to levels 0 to 2 by software
Interrupt factor	NRST pin input	Errors detection, PI interrupt	External pin input Internal peripheral function
Generated operation	Direct input to CPU core	Input to CPU core from non-maskable interrupt control register (NMICR)	Input interrupt request level set in interrupt level flag (xxxLVn) of maskable interrupt control register (xxxICR) to CPU core.
Accept operation	Always accepts	Always accepts	Accepted only by the interrupt control of the register (xxxICR) and the interrupt mask level in PSW.
Machine cycles till acceptance	12	12	12
PSW status after acceptance	All flags are cleared to "0".	The interrupt mask level flag in PSW is cleared to "00".	Values of the interrupt level flag (xxxLVn) are set to the interrupt mask level (masking all interrupt requests with the same or the lower priority).

3-1-2 Block Diagram

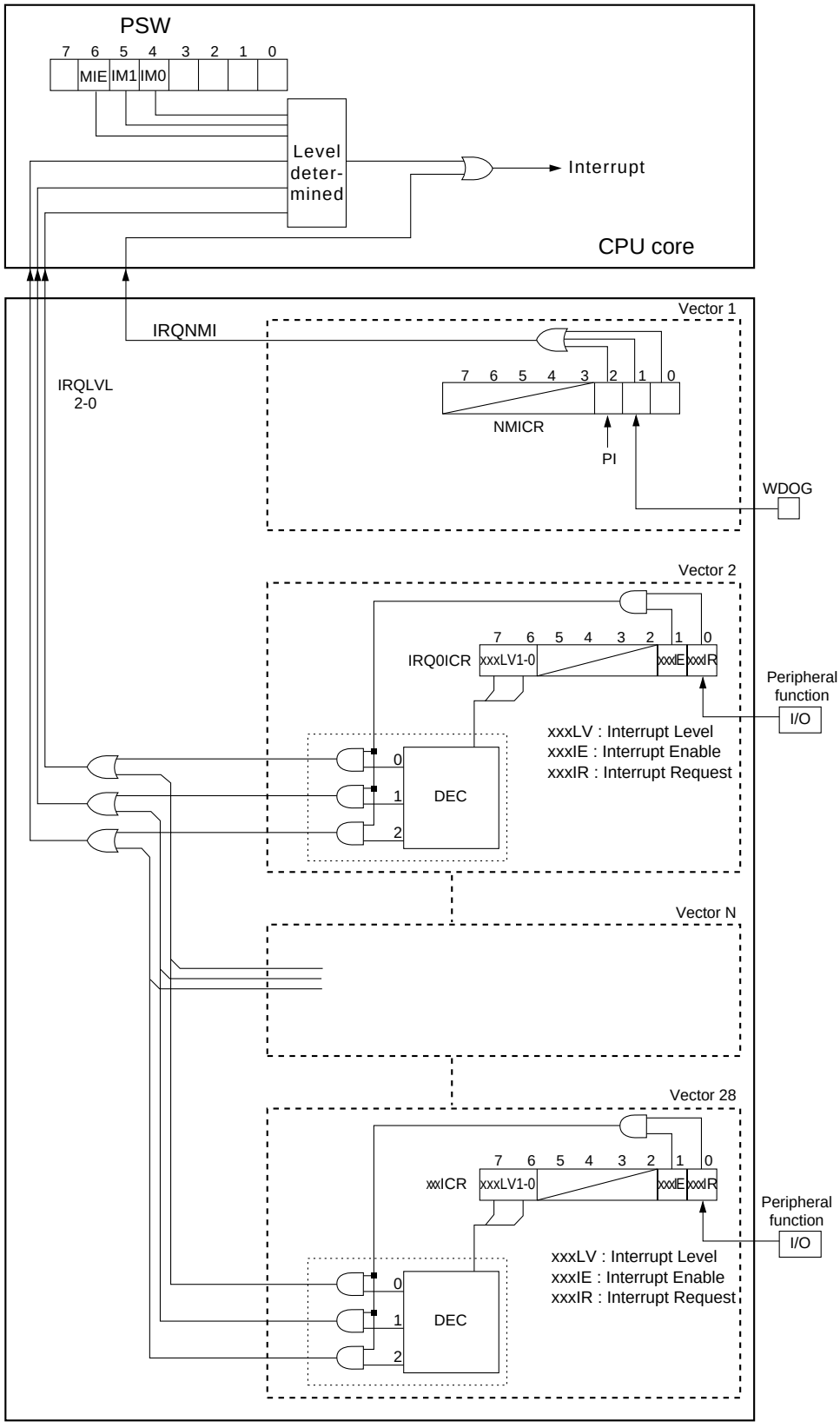


Figure 3-1-1 Interrupt Block Diagram

3-1-3 Operation

■Interrupt Processing Sequence

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. The program counter (PC) and processor status word (PSW) and hard addressing data (HA) are saved onto the stack, and program is branched to the address specified by the corresponding interrupt vector.

An interrupt handler ends by restoring the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

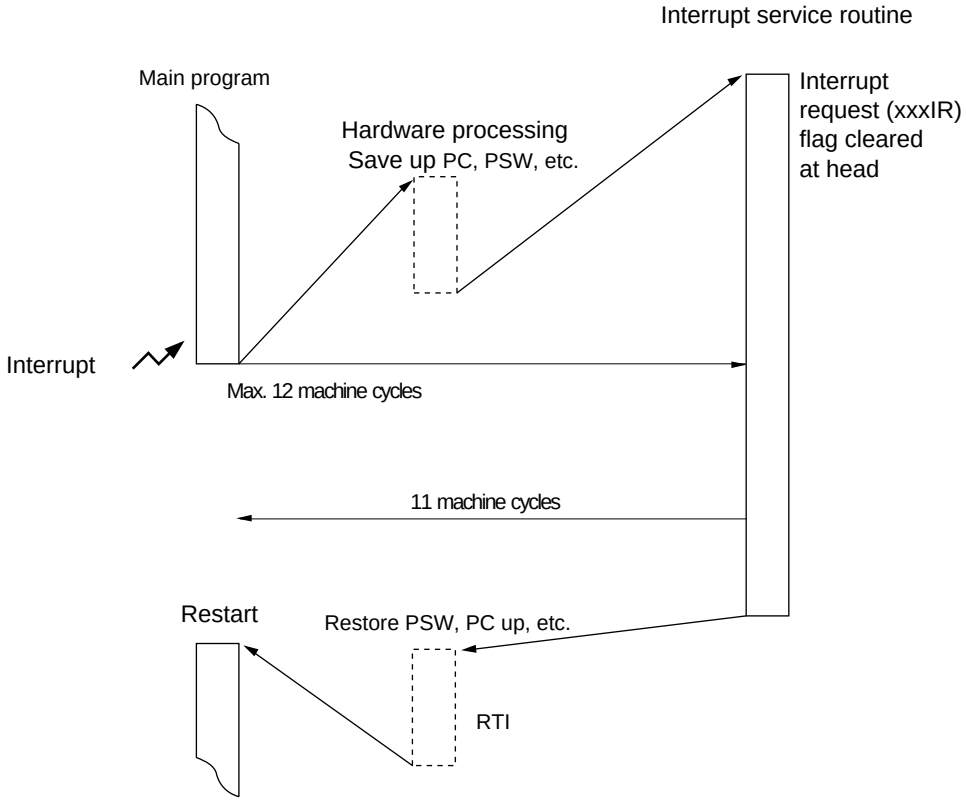


Figure 3-1-2 Interrupt Processing Sequence (maskable interrupts)

■Interrupt Group and Vector Addresses

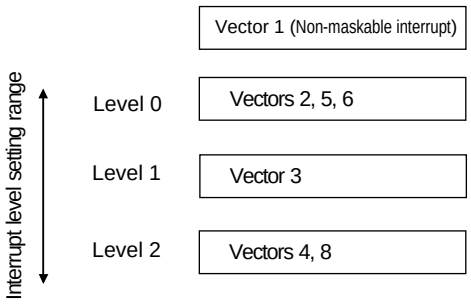
Here is the list of interrupt vector address and interrupt group.

Table 3-1-2 Interrupt Vector Address and Interrupt Group

Vector Number	Vector Address	Interrupt group (Interrupt source)		Control Register (address)	
0	x'04000'	Reset	-	-	-
1	x'04004'	Non-maskable interrupt	NMI	NMICR	x'03FE1'
2	x'04008'	External interrupt 0	IRQ0	IRQ0ICR	x'03FE2'
3	x'0400C'	External interrupt 1	IRQ1	IRQ1ICR	x'03FE3'
4	x'04010'	External interrupt 2	IRQ2	IRQ2ICR	x'03FE4'
5	x'04014'	External interrupt 3	IRQ3	IRQ3ICR	x'03FE5'
6	x'04018'	External interrupt 4	IRQ4	IRQ4ICR	x'03FE6'
7	x'0401C'	External interrupt 5	IRQ5	IRQ5ICR	x'03FE7'
8	x'04020'	External interrupt 6	IRQ6	IRQ6ICR	x'03FE8'
9	x'04024'	Timer 0 interrupt	TM0IRQ	TM0ICR	x'03FE9'
10	x'04028'	Timer 1 interrupt	TM1IRQ	TM1ICR	x'03FEA'
11	x'0402C'	Timer 2 interrupt	TM2IRQ	TM2ICR	x'03FEB'
12	x'04030'	Timer 3 interrupt	TM3IRQ	TM3ICR	x'03FEC'
13	x'04034'	External interrupt 7	IRQ7	IRQ7ICR	x'03FED'
14	x'04038'	Remote control interrupt	RMIRQ	RMICR	x'03FEE'
15	x'0403C'	Timer 6 interrupt	TM6IRQ	TM6ICR	x'03FEF'
16	x'04040'	Time base interrupt	TBIRQ	TBICR	x'03FF0'
17	x'04044'	Timer 7 interrupt	TM7IRQ	TM7ICR	x'03FF1'
18	x'04048'	Timer 7 compare2-match	T7OC2IRQ	T7OC2ICR	x'03FF2'
19	x'0404C'	Timer 8 interrupt	TM8IRQ	TM8ICR	x'03FF3'
20	x'04050'	Timer 8 compare2-match	T8OC2IRQ	T8OC2ICR	x'03FF4'
21	x'04054'	Serial 0 interrupt 1	SC0RIRQ	SC0RICR	x'03FF5'
22	x'04058'	Serial 0 interrupt 2	SC0TIRQ	SC0TICR	x'03FF6'
23	x'0405C'	Reserved	-	-	-
24	x'04060'	Serial 2 interrupt	SC2IRQ	SC2ICR	x'03FF8'
25	x'04064'	Reserved	-	-	-
26	x'04068'	A/D conversion interrupt	ADIRQ	ADICR	x'03FFA'
27	x'0406C'	Reserved	-	-	-
28	x'04070'	Reserved	-	-	-
29	x'04074'	Reserved	-	-	-
30	x'04078'	Reserved	-	-	-

■Interrupt Level and Priority

This LSI allocated vector numbers and interrupt control registers (except reset interrupt) to each interrupt. The interrupt level (except reset interrupt, non-maskable interrupt) can be set by software, per each interrupt group. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupts simultaneously, vector 3 will be accepted.



Priority	Interrupt vector No.
1	Vector 1
2	Vector 2
3	Vector 5
4	Vector 6
5	Vector 3
6	Vector 4
7	Vector 8

Figure 3-1-3 Interrupt Priority Outline

■Determination of Interrupt Acceptance

The following is the procedure from interrupt request input to acceptance.

(1) The interrupt request flag (xxxIR) in the corresponding external interrupt control register(IRQnICR) and internal interrupt control register (xxxICR) are set to '1'.

(2) An interrupt request is input to the CPU. (If the interrupt enable flag (xxxIE) of the same register is '1'.)

(3) The interrupt request signal is set for each interrupt. The interrupt level (IL) is input to the CPU.

(4) The interrupt request is accepted. (If IL has higher priority than IM and MIE is '1'.)

(5) After the interrupt is accepted, the hardware resets the interrupt request flag (xxxIR) in the interrupt control register (xxxICR) to '0'.

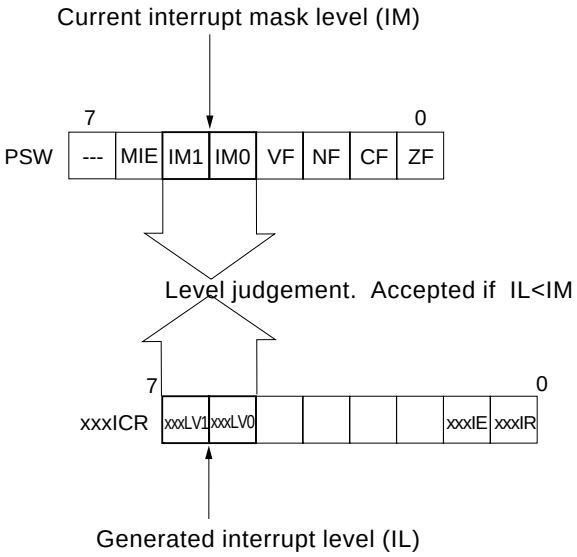


Figure 3-1-4 Determination of Interrupt Acceptance

Acceptance of an interrupt does not reset the corresponding interrupt enable flag (xxxIE) to "0".

MIE='0' and interrupts are disabled when:

- MIE in the PSW is reset to '0' by a program
- Reset is detected

MIE='1' and interrupts are enabled when:

- MIE in the PSW is set to '1' by a program

The interrupt mask level (IM=IM1 - IM0) in the processor status word (PSW) changes when:

- The program alters it directly,
- A reset initializes it to 0 (00b),
- Maskable interrupt is accepted (the interrupt level becomes the interrupt mask level).
- Execution of the RTI instruction at the end of an interrupt service routine restores the processor status word (PSW) and thus the previous interrupt mask level.

The MN101C series does not reset the maskable interrupt enable (MIE) flag of the processor status word (PSW) to "0" when accepting interrupts.

Non-maskable interrupts have priority over maskable ones.

■Interrupt Acceptance Operation

When accepting an interrupt, the MN101C57 hardware saves the handy address register, the return address from the program counter, and the processor status word (PSW) to the stack and branches program to the interrupt handler using the starting address in the vector table.

The following is the hardware processing sequence invoked by interrupt acceptance.

1. The stack pointer (SP) is updated.
   (SP-6 → SP)
2. The contents of the handy address register (HA) are saved to the stack.
   Upper half of HA → (SP+5)
   Lower half of HA → (SP+4)
3. The contents of the program counter (PC) -i.e., the return address- are saved to the stack.
   PC bits 18, 17, and 0 → (SP+3)
   PC bits 16-9 → (SP+2)
   PC bits 8-1 → (SP+1)
4. The contents of the PSW are saved to the stack.
   PSW → (SP)
5. The interrupt level (xxxLVn) for the interrupt is copied to the interrupt mask (IMn) in the PSW.
   Interrupt level (xxxLVn) → IMn
6. The hardware branches program to the address in the vector table.

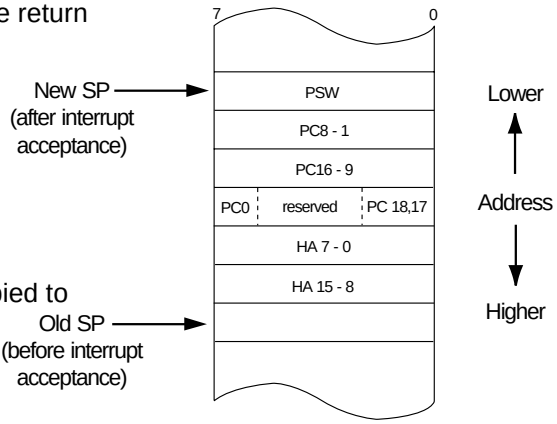


Figure 3-1-5 Stack Operation during interrupt acceptance

■Interrupt Return Operation

An interrupt handler ends by restoring the contents of any registers saved to the stack during processing by the POP instruction and other means, and the RTI instruction restores the program to the point at execution was interrupted.

The following is the processing sequence invoked by the RTI instruction.

1. The contents of the PSW are restored from the stack. (SP)
2. The contents of the program counter (PC) - i.e., the return address- are restored from the stack. (SP+1 to SP+3)
3. The contents of the handy address register (HA) are restored from the stack. (SP+4, SP+5)
4. The stack pointer is updated. (SP+6 → SP)
5. Execution branches program to the address in the program counter.

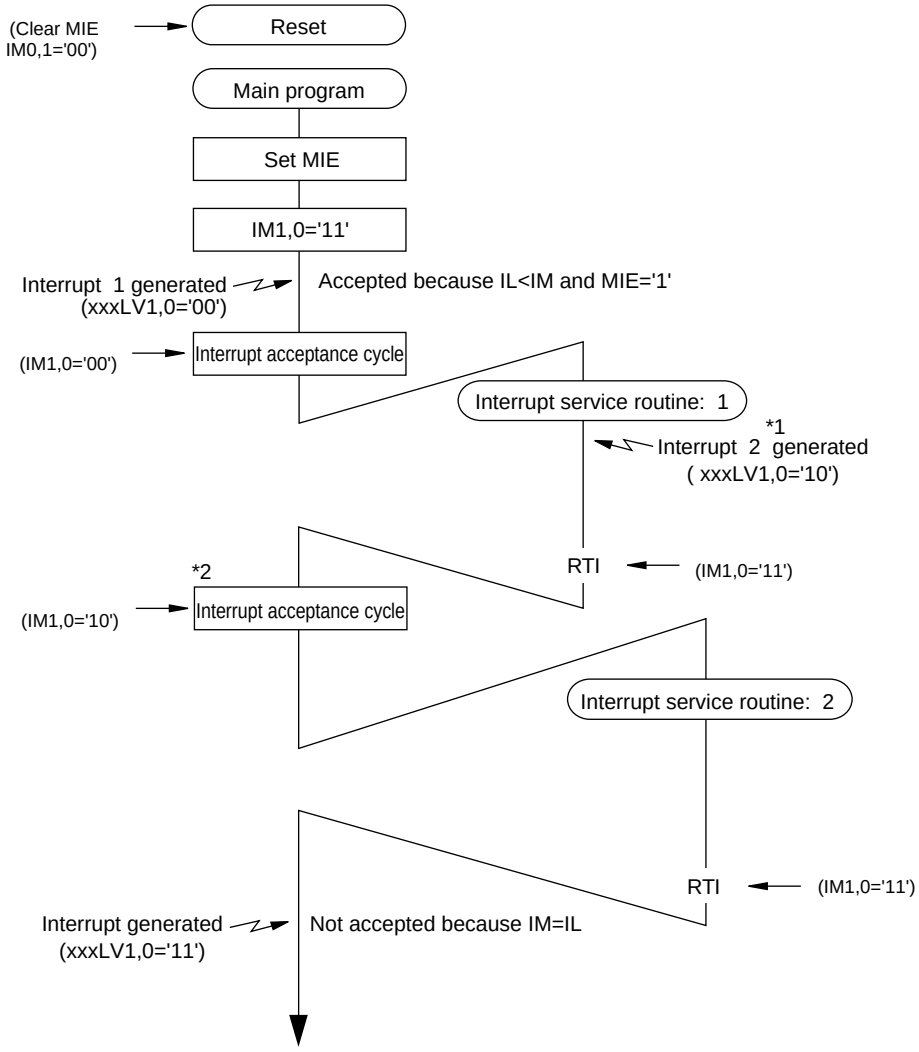
The handy address register is an internal register used by the handy addressing function. The hardware saves its contents to the stack to prevent the interrupt from interfering with operation of the function.

Registers such as data register, or address register are not saved, so that PUSH instruction from program should be used to save them onto the stack, if necessary.

The address bp6 to bp2, when program counter (PC) are saved to the stack, are reserved. Do not change it by program.

■Maskable Interrupt

Figure 3-1-6 shows the processing flow when a second interrupt with a lower priority level (xxxLV1-xxxLV0='10') arrives during the processing of one with a higher priority level (xxxLV1-xxxLV0='00').



Parentheses ( ) indicate hardware processing.

*1 If during the processing of the first interrupt, an interrupt request with an interrupt level (IL) numerically lower than the interrupt mask (IM) arrives, it is accepted as a nested interrupt. If IL ≥ IM, however, the interrupt is not accepted.

*2 The second interrupt, postponed because its interrupt level (IL) was numerically greater than the interrupt mask (IM) for the first interrupt service routine, is accepted when the first interrupt handler returns.

Figure 3-1-6 Processing Sequence for Maskable Interrupts

■Multiplex Interrupt

When an MN101C57 series device accepts an interrupt, it automatically disables acceptance of subsequent interrupts with the same or lower priority level. When the hardware accepts an interrupt, it copies the interrupt level (xxxLVn) for the interrupt to the interrupt mask (IM) in the PSW. As a result, subsequent interrupts with the same or lower priority levels are automatically masked. Only interrupts with higher priority levels are accepted. The net result is that interrupts are normally processed in decreasing order of priority. It is, however, possible to alter this arrangement.

1. To disable interrupt nesting
   - Reset the MIE bit in the PSW to "0".
   - Raise the priority level of the interrupt mask (IM) in the PSW.
2. To enable interrupts with lower priority than the currently accepted interrupt
   - Lower the priority level of the interrupt mask (IM) in the PSW.

Multiplex interrupts are only enabled for interrupts with levels higher than the PSW interrupt mask level (IM).

It is possible to forcibly rewrite IM to accept an interrupt with a priority lower than the interrupt being processed, but be careful of stack overflow.

Do not operate the maskable interrupt control register (xxxICR) when multiple interrupts are enabled. If operation is necessary, first clear the PSW MIE flag.

Figure 3-1-7 shows the processing flow for multiple interrupts (interrupt 1: xxxLV1-xxxLV0='10', and interrupt 2: xxxLV1-xxxLV0='00').

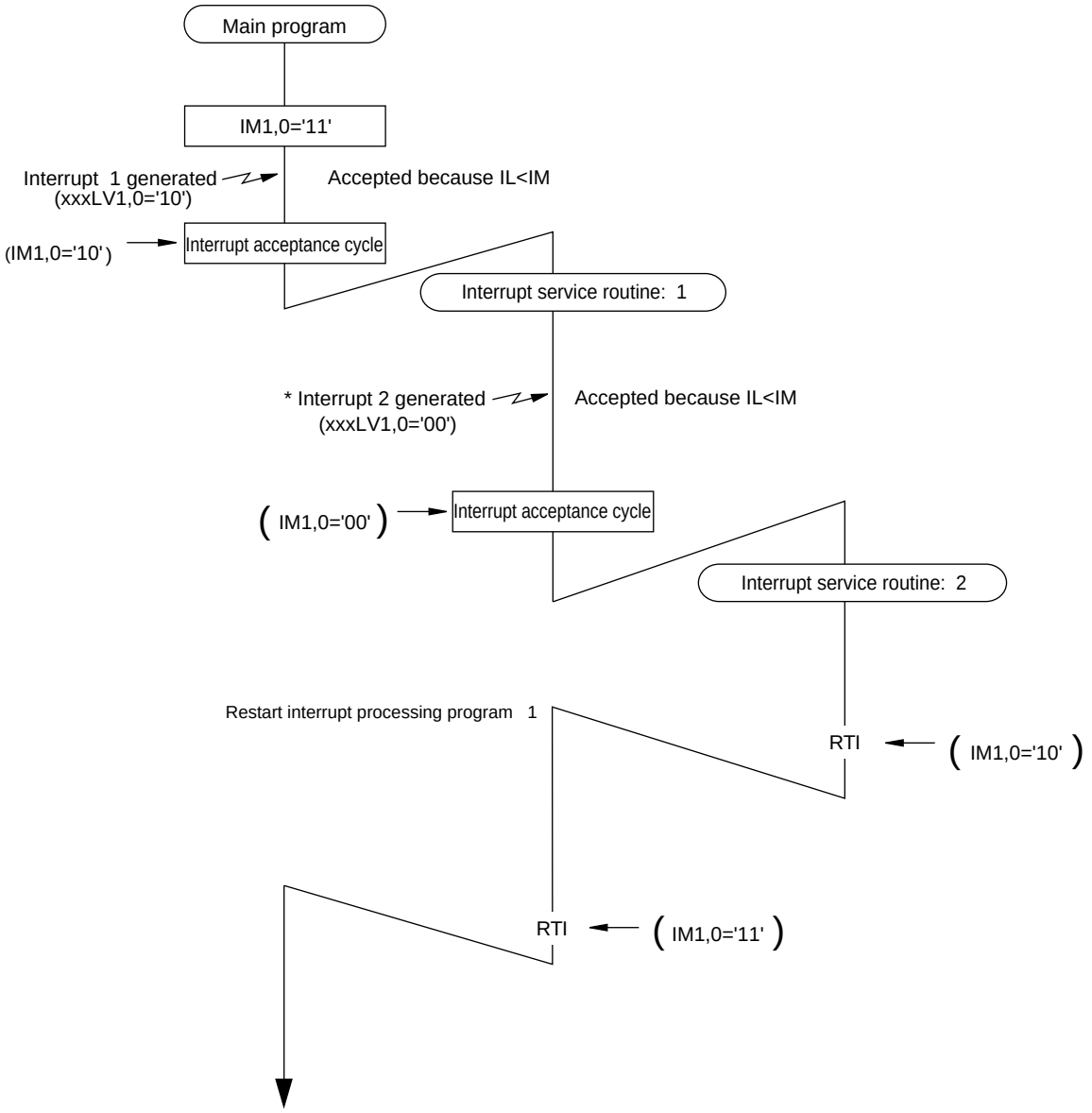


Figure 3-1-7 Processing Sequence with Multiple Interrupts Enabled

3-1-4 Interrupt Flag Setup

■ Interrupt request flag (IR) setup by the software

The interrupt request flag is operated by the hardware. That is set to "1" when any interrupt factor is generated, and cleared to "0" when the interrupt is accepted. If you want to operate it by the software, the IRWE flag of MEMCTR should be set to "1".

■ Interrupt flag setup procedure

A setup procedure of the interrupt request flag set by the hardware and the software shows as follows ;

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp6 : MIE = 0	(1) Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2) Select the interrupt factor.	(2) Select the interrupt factor such as interrupt edge selection, or timer interrupt cycle change.
(3) Enable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 1	(3) Set the IRWE flag of MEMCTR to enable the interrupt request flag to be rewritten. This is necessary only when the interrupt request flag is changed by the software.
(4) Rewrite the interrupt request flag. xxxICR bp0 : xxxIR	(4) Rewrite the interrupt request flag (xxxIR) of the interrupt control register (xxxICR).
(5) Disable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 0	(5) Clear the IRWE flag so that interrupt request flag can not be rewritten by the software.
(6) Set the interrupt level. xxxICR bp7-6 : xxxLV1-0 PSW bp5-4 : IM1-0	(6) Set the interrupt level by the xxxLV1-0 flag of the interrupt control register (xxxICR). Set the IM1-0 flag of PSW when the interrupt acceptance level of CPU should be changed.
(7) Enable the interrupt. xxxICR bp1 : xxxIE = 1	(7) Set the xxxIE flag of the interrupt control register (xxxICR) to enable the interrupt.
(8) Enable all maskable interrupts. PSW bp6 : MIE = 1	(8) Set the MIE flag of PSW to enable maskable interrupts.

3-2 Control Registers

3-2-1 Registers List

Table 3-2-1 Interrupt Control Registers

Register	Address	R/W	Functions	Page
NMICR	x'03FE1'	R/W	Non-maskable interrupt control register	Ⅲ - 16
IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	Ⅲ - 17
IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	Ⅲ - 18
IRQ2ICR	x'03FE4'	R/W	External interrupt 2 control register	Ⅲ - 19
IRQ3ICR	x'03FE5'	R/W	External interrupt 3 control register	Ⅲ - 20
IRQ4ICR	x'03FE6'	R/W	External interrupt 4 control register	Ⅲ - 21
IRQ5ICR	x'03FE7'	R/W	External interrupt 5 control register	Ⅲ - 22
IRQ6ICR	x'03FE8'	R/W	External interrupt 6 control register	Ⅲ - 23
TM0ICR	x'03FE9'	R/W	Timer 0 interrupt control register (Timer 0 compare-match)	Ⅲ - 24
TM1ICR	x'03FEA'	R/W	Timer 1 interrupt control register (Timer 1 compare-match)	Ⅲ - 25
TM2ICR	x'03FEB'	R/W	Timer 2 interrupt control register (Timer 2 compare-match)	Ⅲ - 26
TM3ICR	x'03FEC'	R/W	Timer 3 interrupt control register (Timer 3 compare-match)	Ⅲ - 27
IRQ7ICR	x'03FED'	R/W	External interrupt 7 control register	Ⅲ - 28
RMICR	x'03FEE'	R/W	Remote control interrupt control register	Ⅲ - 29
TM6ICR	x'03FEF'	R/W	Timer 6 interrupt control register (Timer 6 compare-match)	Ⅲ - 30
TBICR	x'03FF0'	R/W	Time base interrupt control register (Time base period)	Ⅲ - 31
TM7ICR	x'03FF1'	R/W	Timer 7 interrupt control register (Timer 7 compare-match)	Ⅲ - 32
T7OC2ICR	x'03FF2'	R/W	Timer 7 compare register 2-match interrupt control register	Ⅲ - 33
TM8ICR	x'03FF3'	R/W	Timer 8 interrupt control register (Timer 8 compare-match)	Ⅲ - 34
T8OC2ICR	x'03FF4'	R/W	Timer 8 compare register 2-match interrupt control register	Ⅲ - 35
SC0RICR	x'03FF5'	R/W	Serial 0 nterrupt control register 1	Ⅲ - 36
SC0TICR	x'03FF6'	R/W	Serial 0 interrupt control register 2	Ⅲ - 37
SC2ICR	x'03FF8'	R/W	Serial 2 interrupt control register	Ⅲ - 38
ADICR	x'03FFA'	R/W	A/D conversion interrupt control register (A/D conversion complete)	Ⅲ - 39

R/W : Readable / Writable.

Writing to the interrupt control register should be done after that all maskable interrupts are set to be disable by the MIE flag of the PSW register.

If the interrupt level flag (xxxLVn) is set to "level 3", its vector is disabled, regardless of interrupt enable flag and interrupt request flag.

3-2-2 Interrupt Control Registers

The interrupt control registers include the non-maskable interrupt control register (NMICR), the external interrupt control register and the internal interrupt control registers (xxxICR).

■Non-Maskable Interrupt Control Register (NMICR address: x'3FE1')

The non-maskable interrupt control register (NMICR) is stored the non maskable interrupt request. When the non-maskable interrupt request is generated, the interrupt is accepted regardless of the interrupt mask level (IMn) of PSW. The hardware then branches program to the address stored at location x'4004' in the interrupt vector table. The watchdog timer overflow interrupt request flag (WDIR) is set to "1" when the watchdog timer overflows. The program interrupt request flag (PIR) is set to "1" when the undefined instruction is executed.
Setting PIR or WDIR flag to be "1" enable non-maskable interrupt request to be set compulsory.

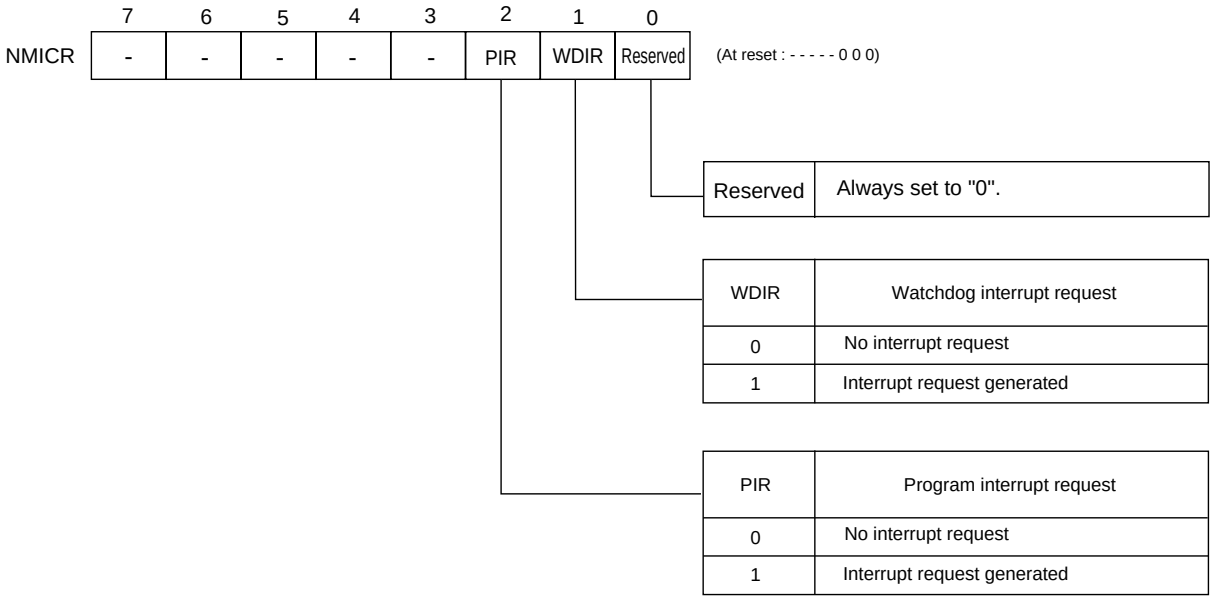


Figure 3-2-1 Non-Maskable Interrupt Control Register (NMICR:x'03FE1', R/W)

On this LSI, when undefined instruction is decoded, the program interrupt request flag (PIR) is set to "1", and the non-maskable interrupt is generated.
When the PIR flag is confirmed to be set using the non-maskable interrupt service routine, the reset via the software, which the reset pin (P27) outputs "0", is recommended.

Once the WDIR becomes "1" by generation of non-maskable interrupt, only the program can clear it to "0".

■External Interrupt 0 Control Register (IRQ0ICR)

The external interrupt 0 control register (IRQ0ICR) controls interrupt level of the external interrupt 0, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

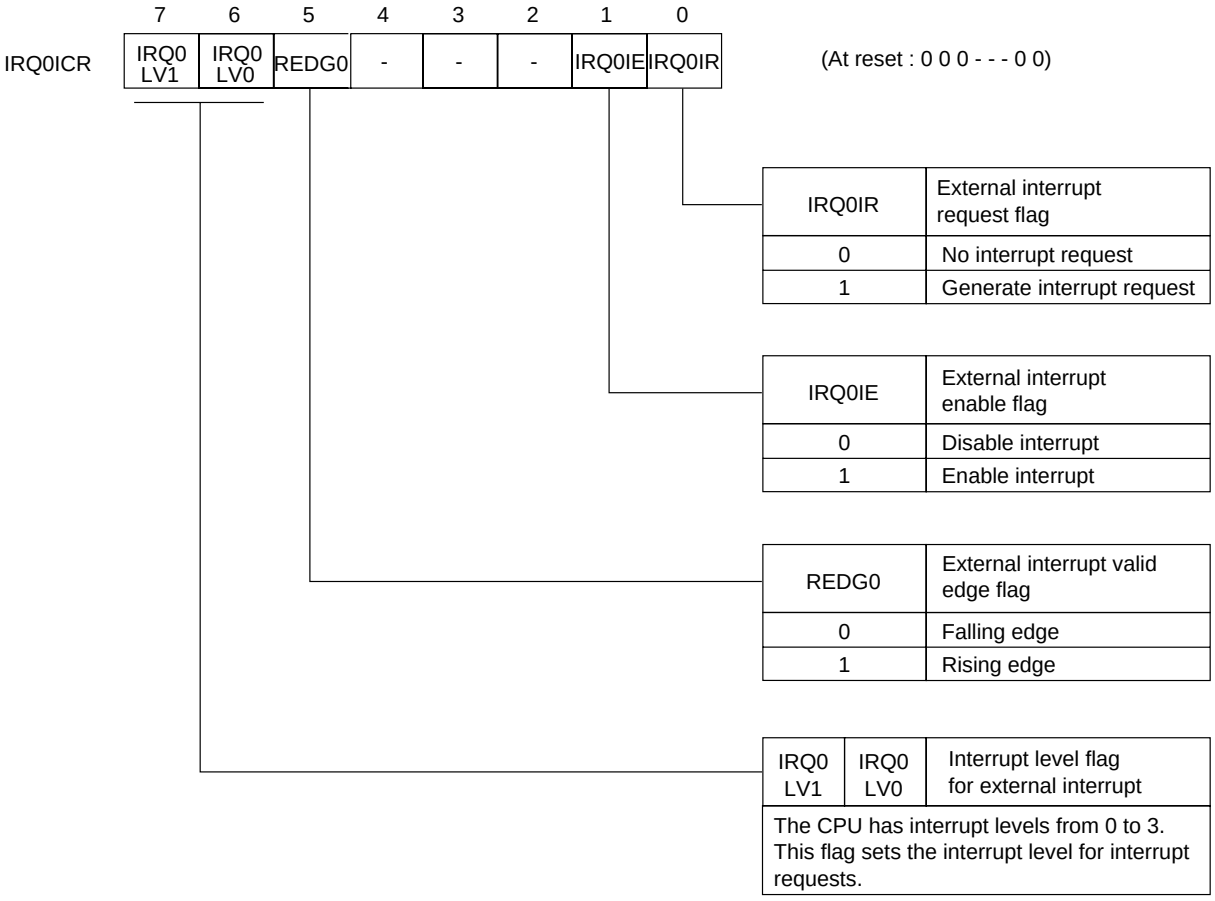


Figure 3-2-2 External Interrupt 0 Control Register (IRQ0ICR : x'03FE2', R/W)

■External Interrupt 1 Control Register (IRQ1ICR)

The external interrupt 1 control register (IRQ1ICR) controls interrupt level of external interrupt 1, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

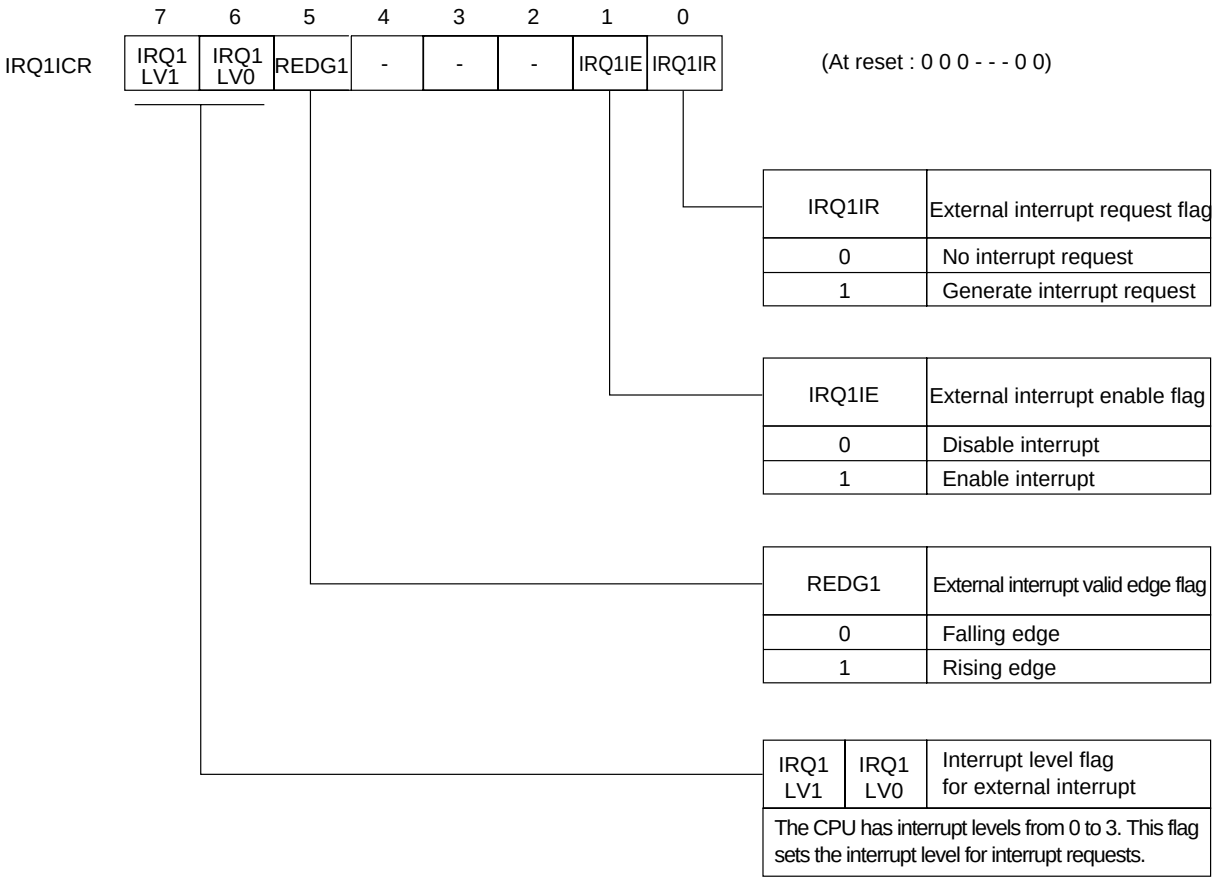


Figure 3-2-3 External Interrupt 1 Control Register (IRQ1ICR : x'03FE3', R/W)

■External Interrupt 2 Control Register (IRQ2ICR)

The external interrupt 2 control register (IRQ2ICR) controls interrupt level of external interrupt 2, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

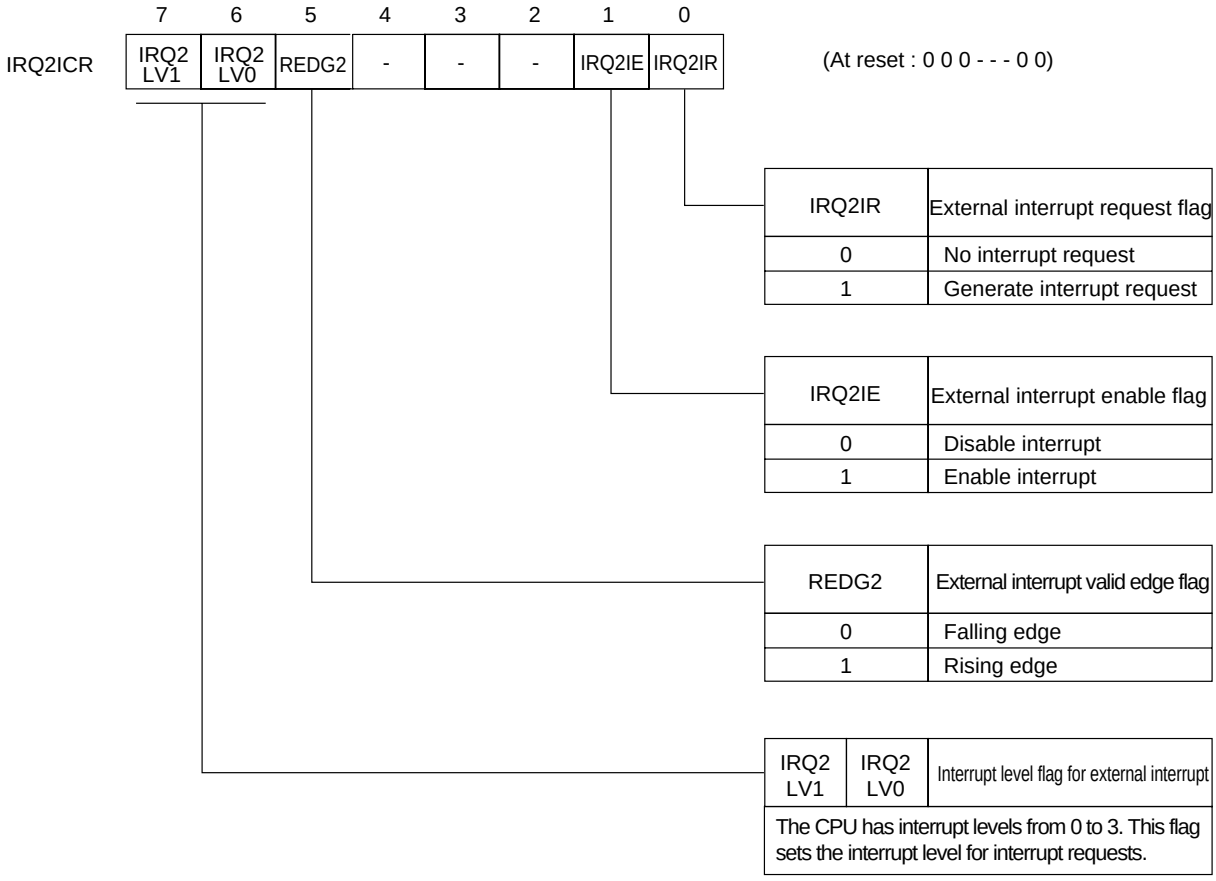


Figure 3-2-4 External Interrupt 2 Control Register (IRQ2ICR : x'03FE4', R/W)

■External Interrupt 3 Control Register (IRQ3ICR)

The external interrupt 3 control register (IRQ3ICR) controls interrupt level of external interrupt 3, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

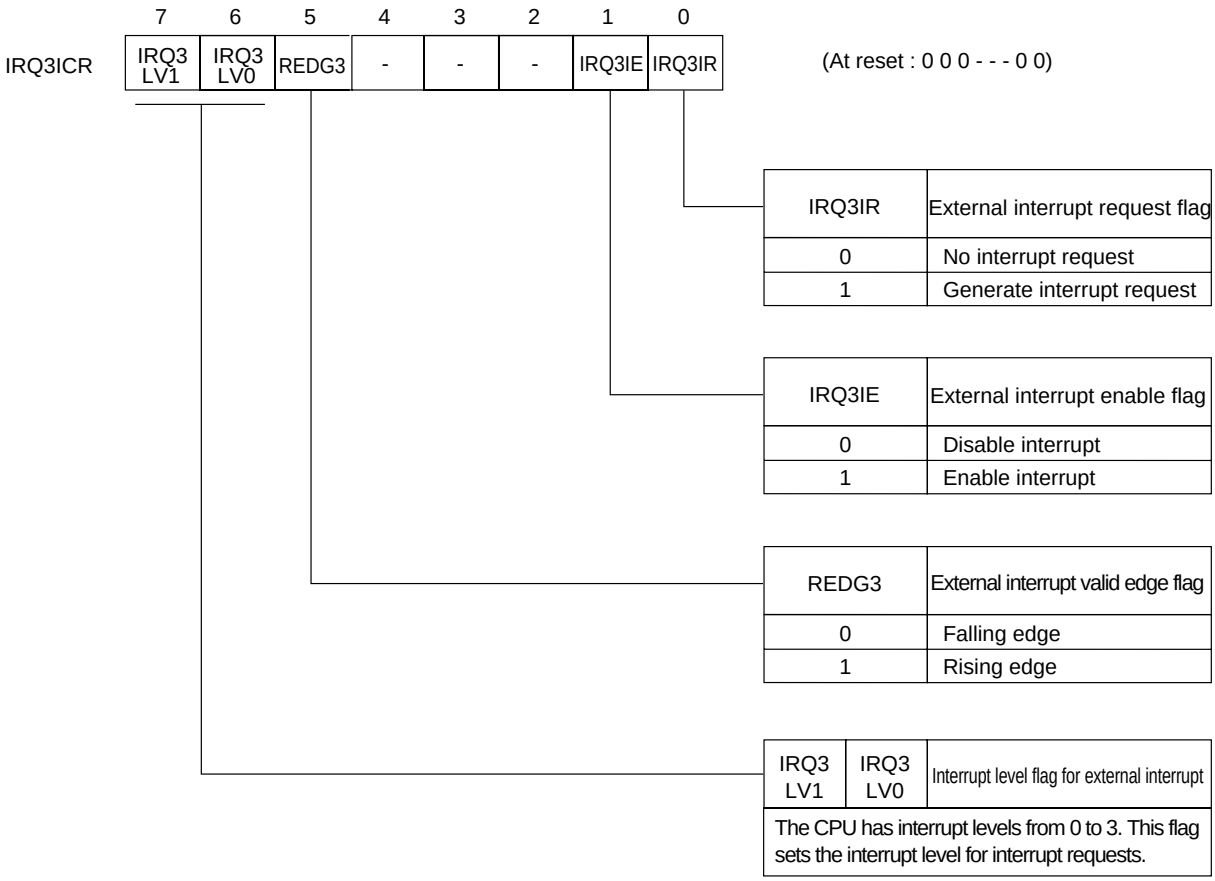


Figure 3-2-5 External Interrupt 3 Control Register (IRQ3ICR : x'03FE5', R/W)

■External Interrupt 4 Control Register (IRQ4ICR)

The external interrupt 4 control register (IRQ4ICR) controls interrupt level of external interrupt 4, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

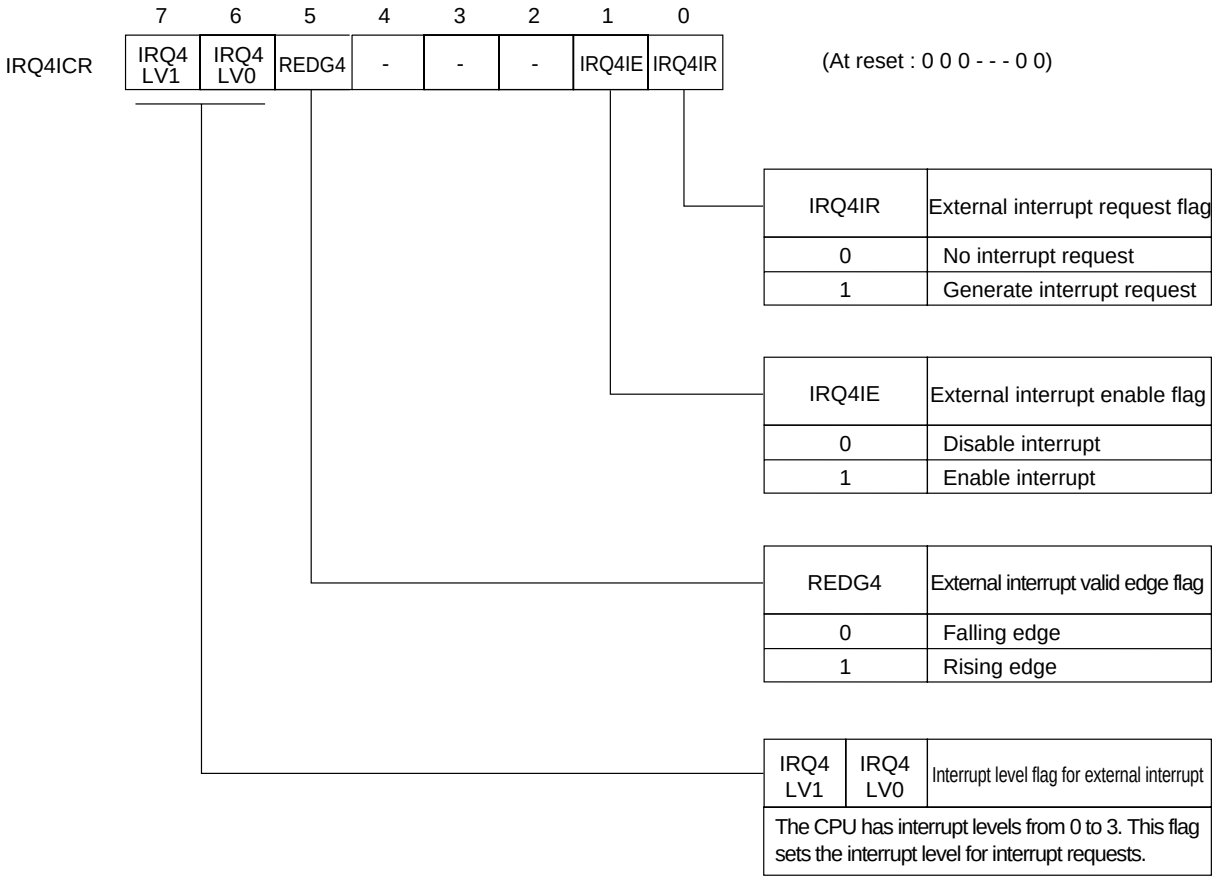


Figure 3-2-6 External Interrupt 4 Control Register (IRQ4ICR : x'03FE6', R/W)

■External Interrupt 5 Control Register (IRQ5ICR)

The external interrupt 5 control register (IRQ5ICR) controls interrupt level of external interrupt 5, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

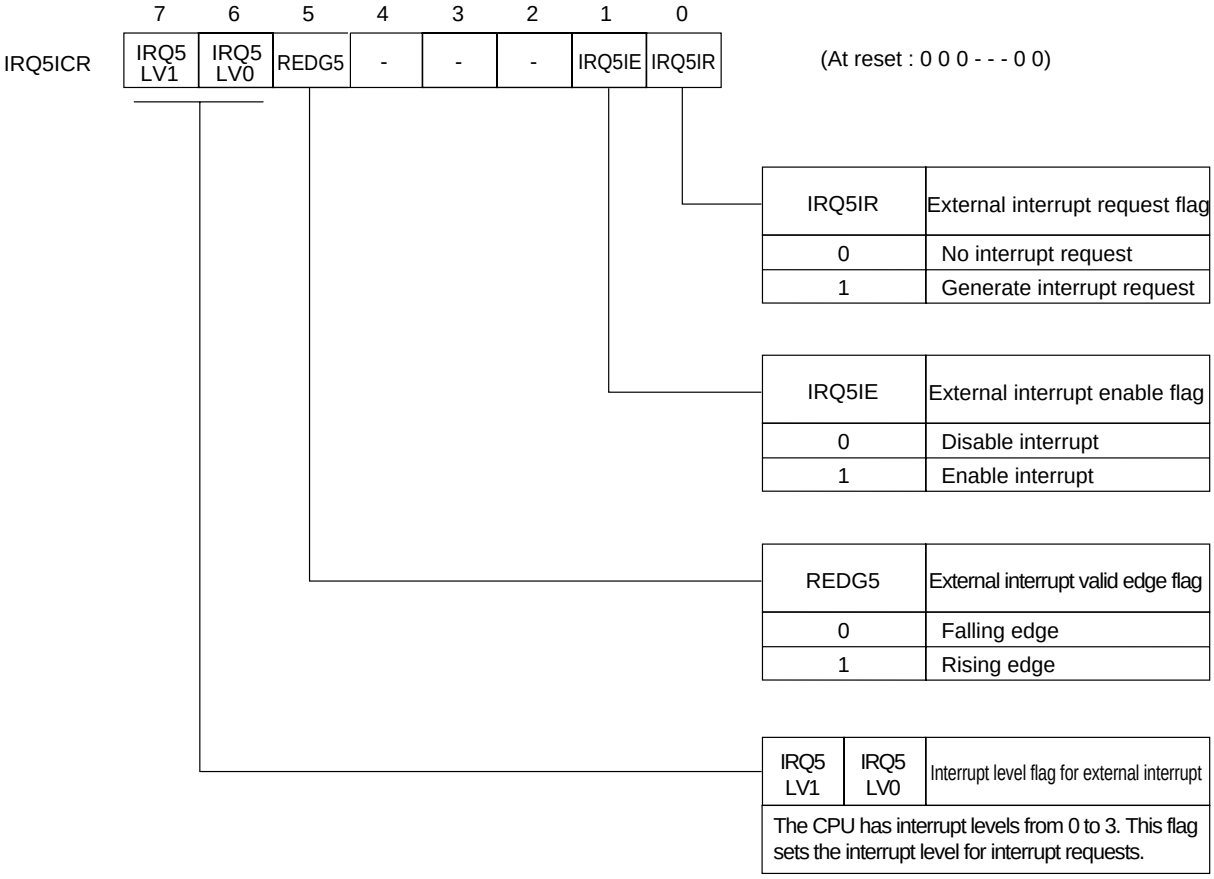


Figure 3-2-7 External Interrupt 5 Control Register (IRQ5ICR : x'03FE7', R/W)

■External Interrupt 6 Control Register (IRQ6ICR)

The external interrupt 6 control register (IRQ6ICR) controls interrupt level of external interrupt 6, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

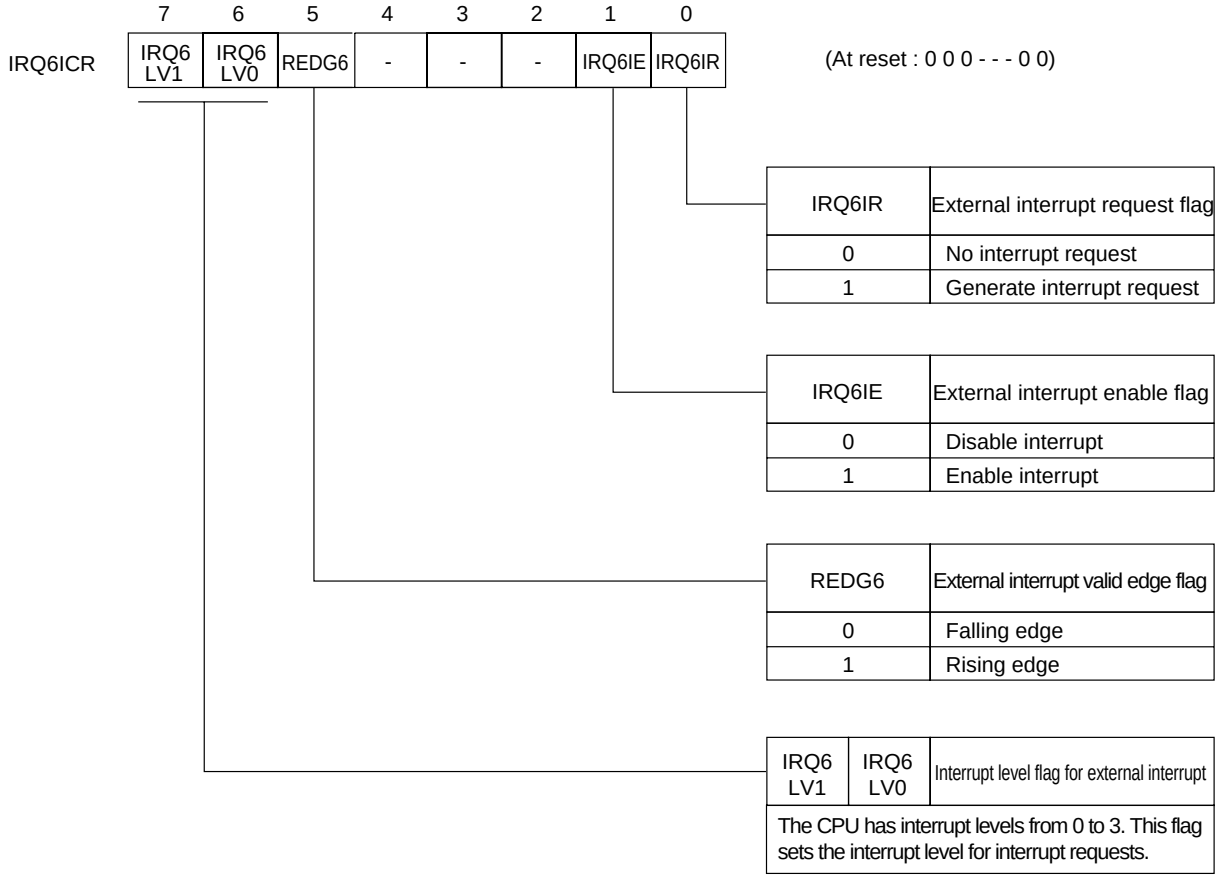


Figure 3-2-8 External Interrupt 6 Control Register (IRQ6ICR : x'03FE8', R/W)

■Timer 0 Interrupt Control Register (TM0ICR)

The timer 0 interrupt control register (TM0ICR) controls interrupt level of timer 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

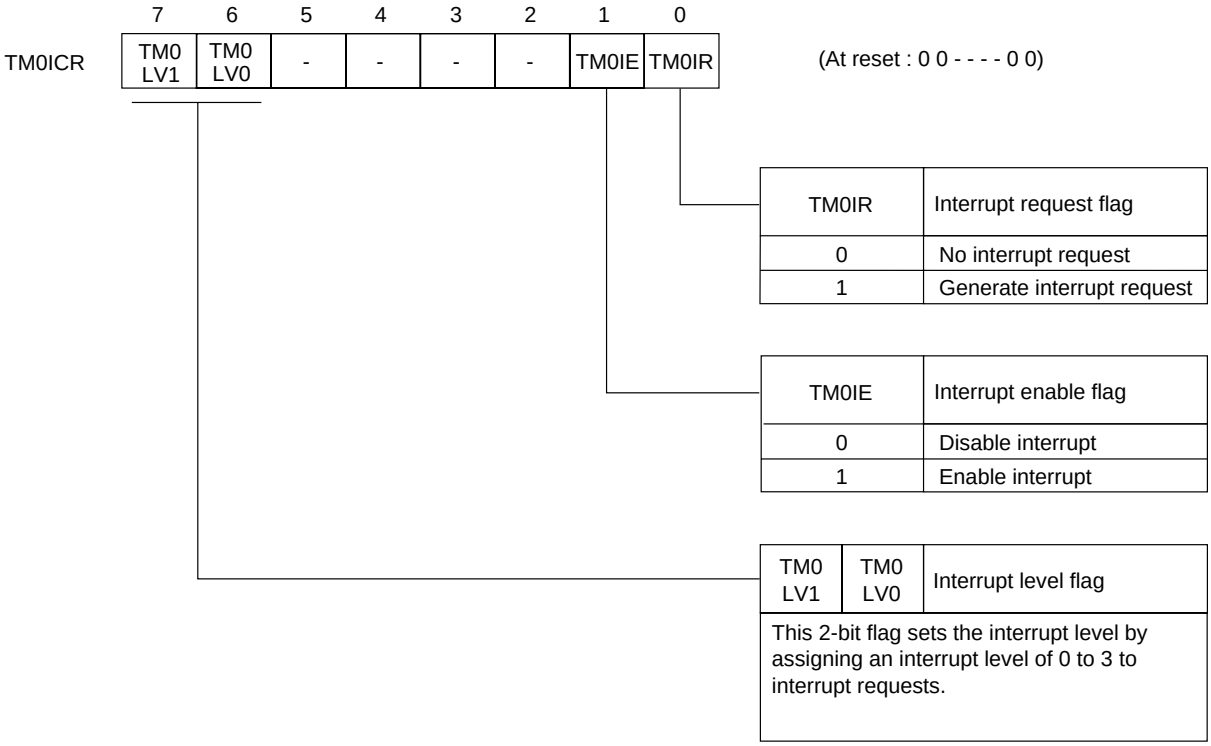


Figure 3-2-9 Timer 0 Interrupt Control Register (TM0ICR : x'03FE9', R/W)

■Timer 1 Interrupt Control Register (TM1ICR)

The timer 1 interrupt control register (TM1ICR) controls interrupt level of timer 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

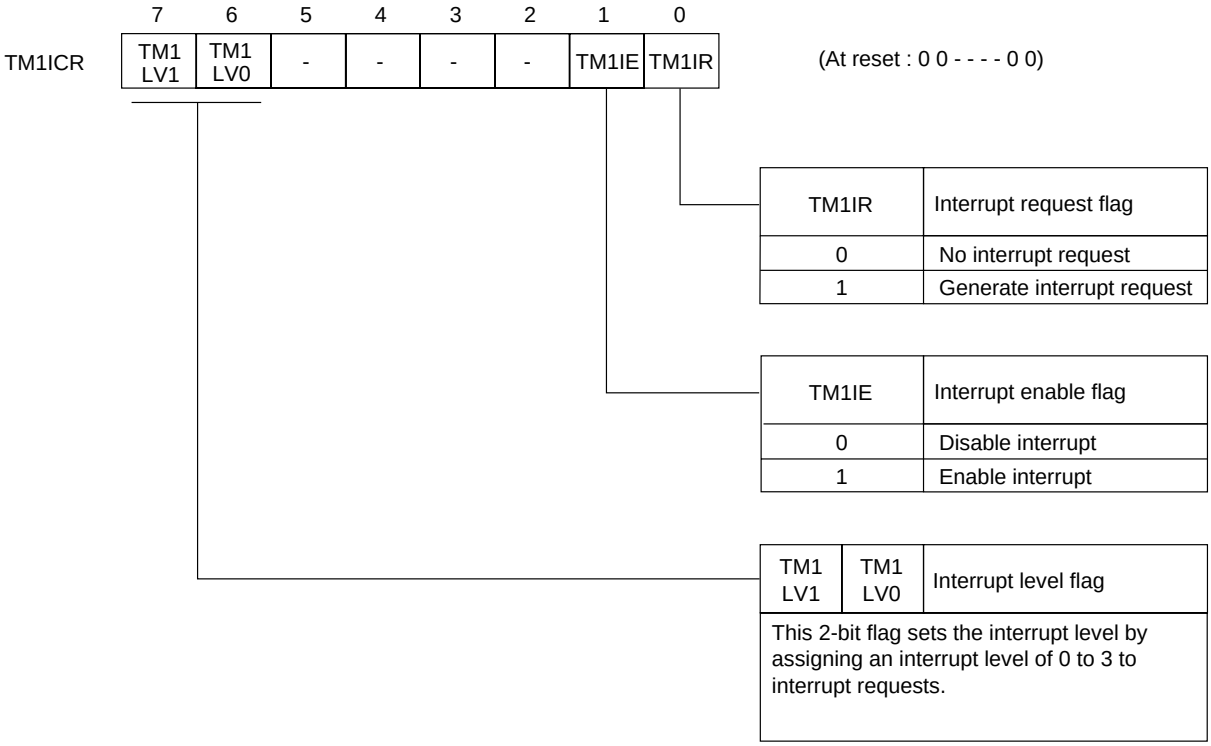


Figure 3-2-10 Timer 1 Interrupt Control Register (TM1ICR : x'03FEA', R/W)

■Timer 2 Interrupt Control Register (TM2ICR)

The timer 2 interrupt control register (TM2ICR) controls interrupt level of timer 2 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

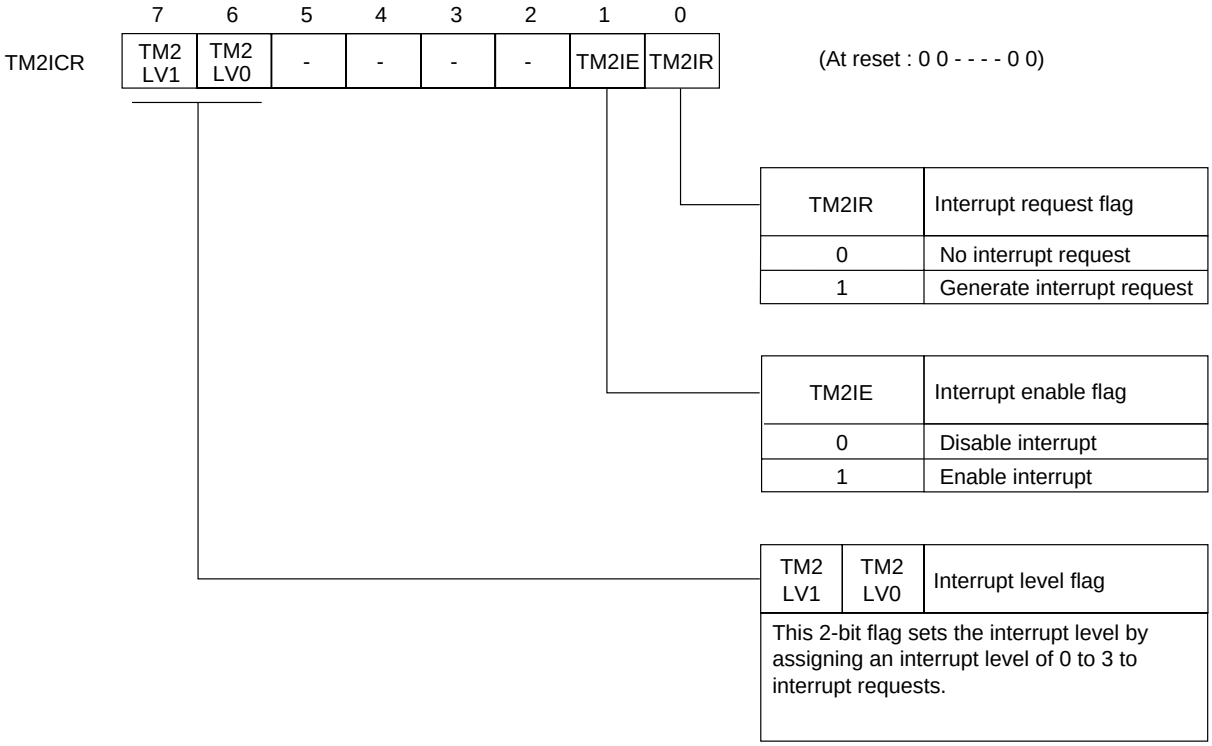


Figure 3-2-11 Timer 2 Interrupt Control Register (TM2ICR : x'03FEB', R/W)

■Timer 3 Interrupt Control Register (TM3ICR)

The timer 3 interrupt control register (TM3ICR) controls interrupt level of timer 3 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

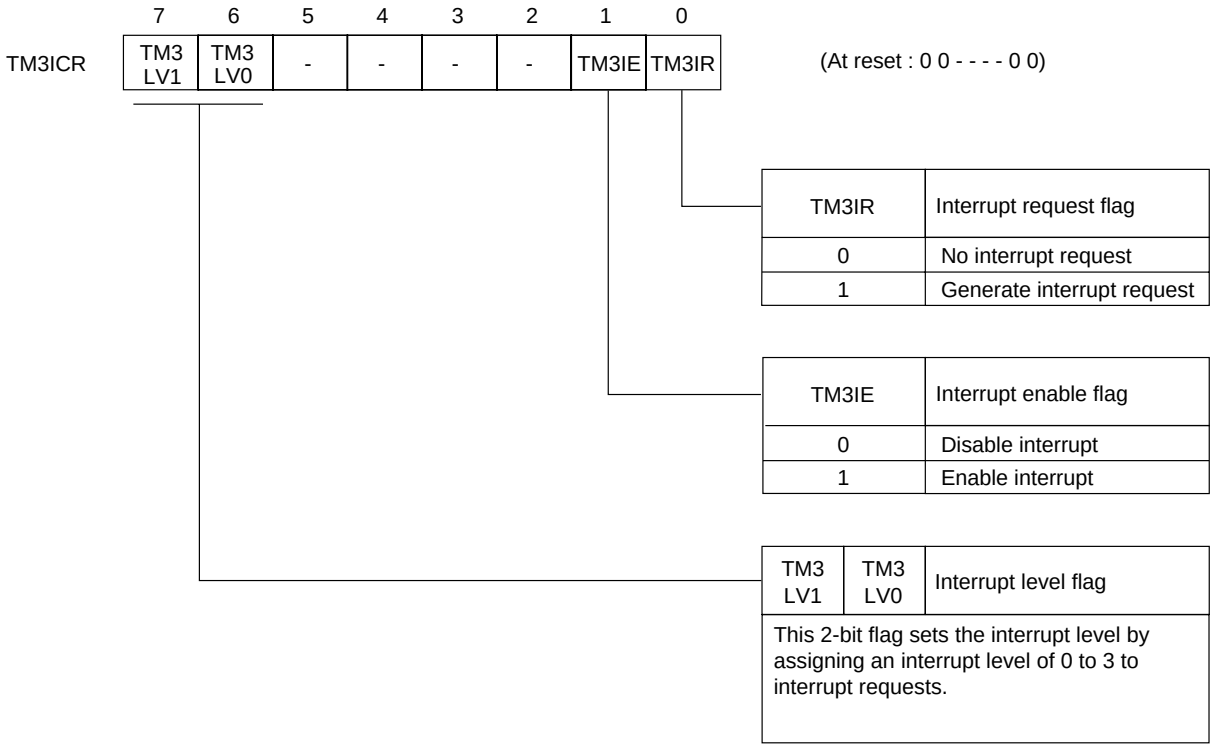


Figure 3-2-12 Timer 3 Interrupt Control Register (TM3ICR : x'03FEC', R/W)

■External Interrupt 7 Control Register (IRQ7ICR)

The external interrupt 7 control register (IRQ7ICR) controls interrupt level of external interrupt 7, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

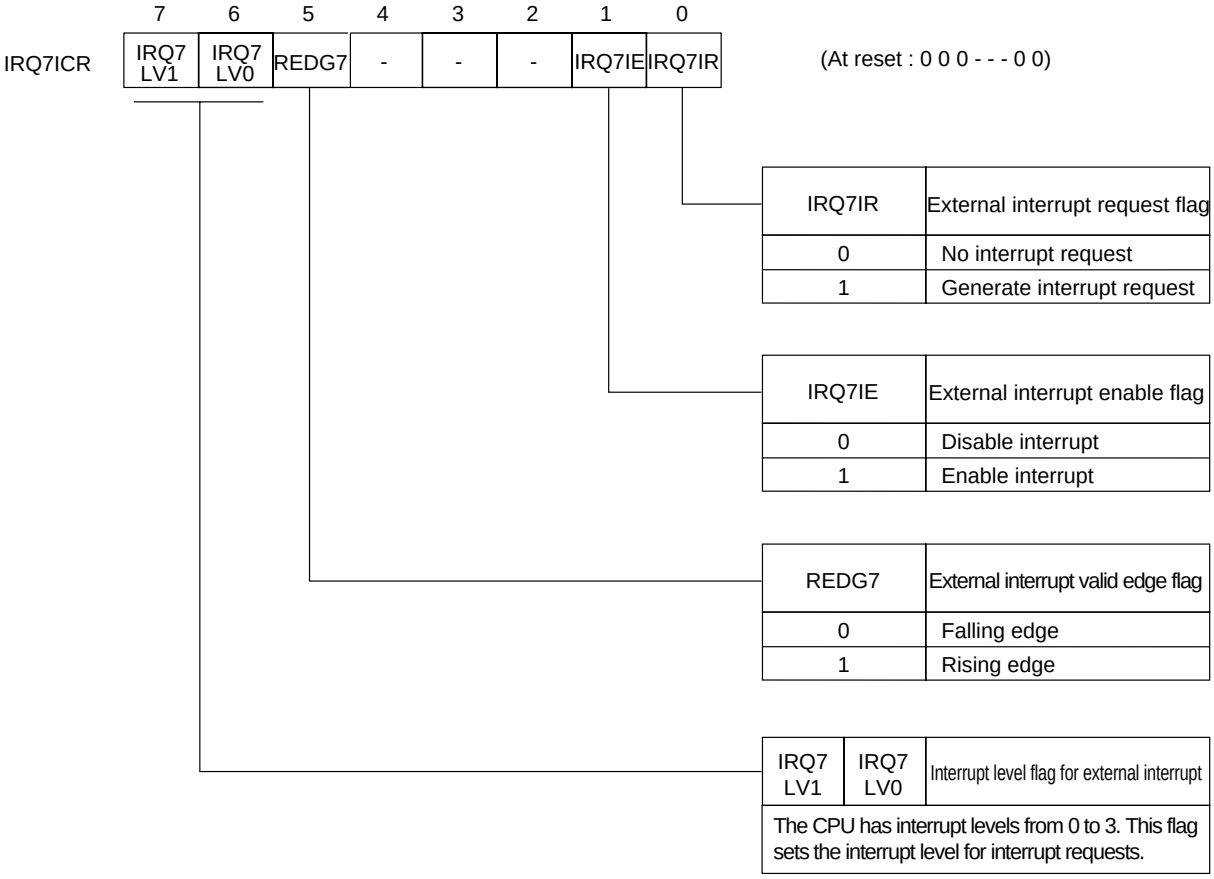


Figure 3-2-13 External Interrupt 7 Control Register (IRQ7ICR : x'03FE9', R/W)

■Remote Control Interrupt Control Register (RMICR)

The remote control interrupt control register (RMICR) controls interrupt level of remote control interrupt, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

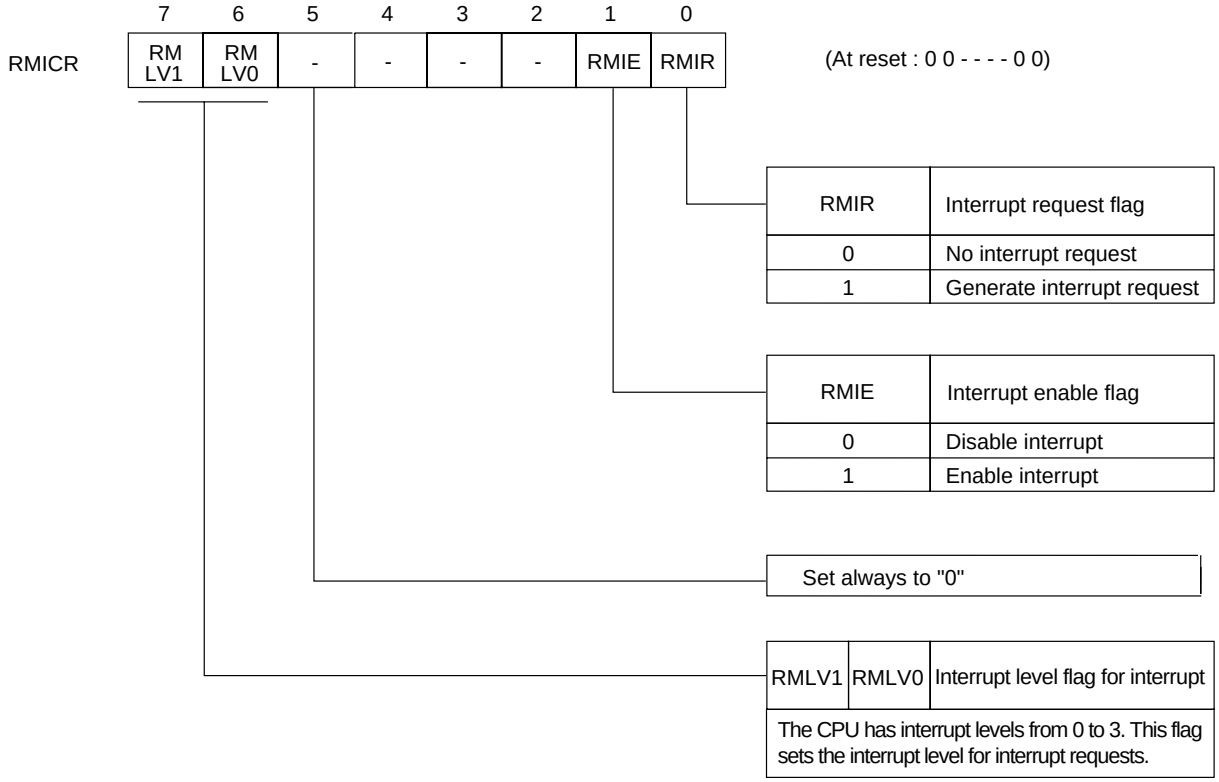


Figure 3-2-14 Remote Control Interrupt Control Register (RMICR : x'03FEE', R/W)

■Timer 6 Interrupt Control Register (TM6ICR)

The timer 6 interrupt control register (TM6ICR) controls interrupt level of timer 6 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

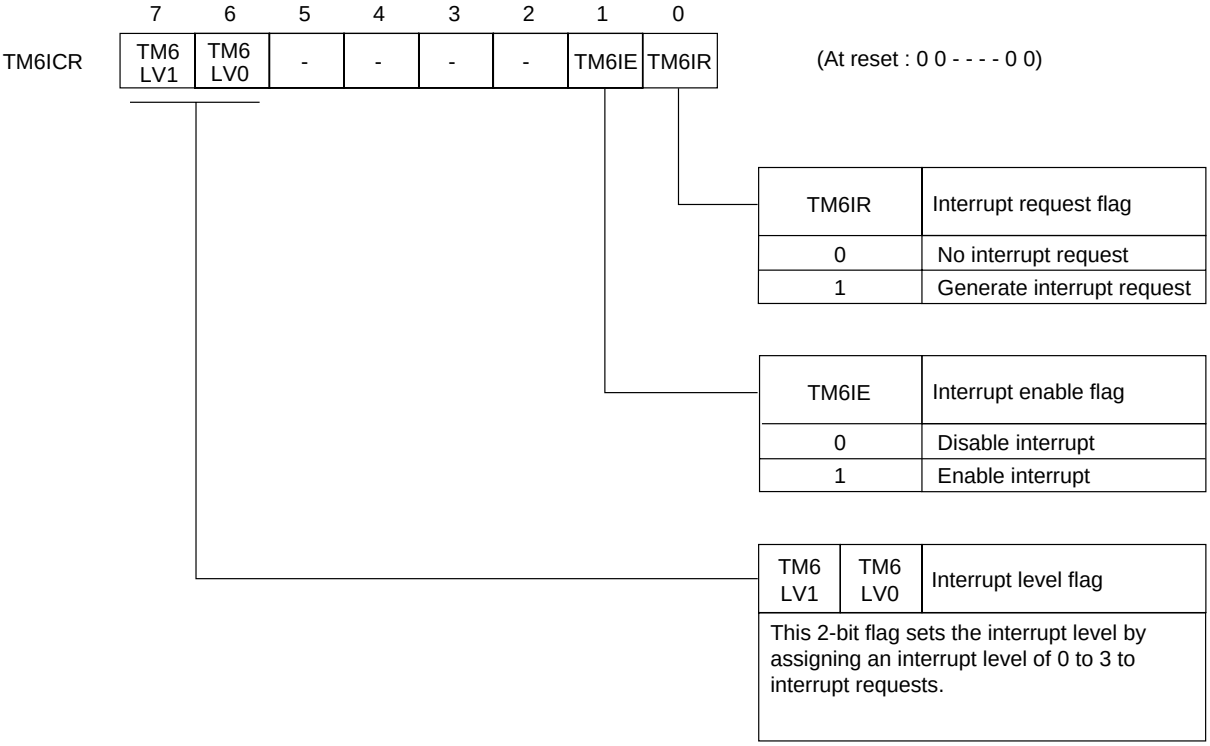


Figure 3-2-15 Timer 6 Interrupt Control Register (TM6ICR : x'03FEF', R/W)

■Time Base Interrupt Control Register (TBICR)

The time base interrupt control register (TBICR) controls interrupt level of time base interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

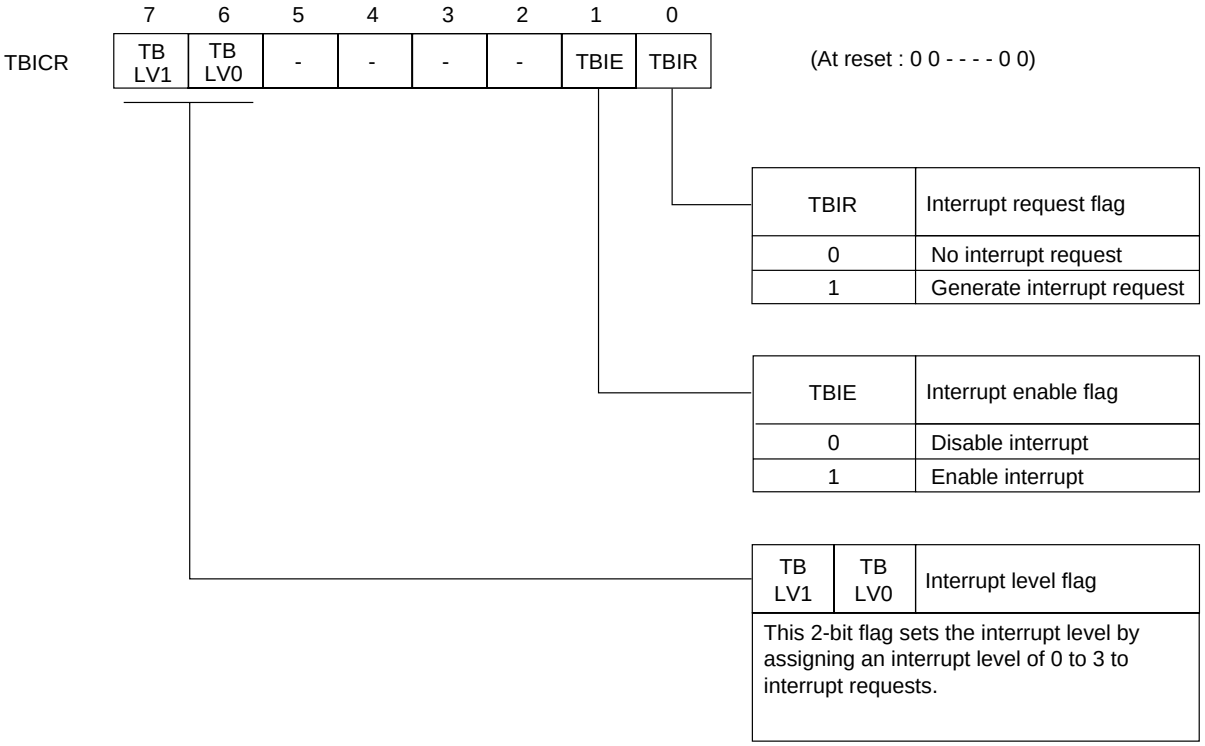


Figure 3-2-16 Time Base Interrupt Control Register (TBICR : x'03FF0', R/W)

■Timer 7 Interrupt Control Register (TM7ICR)

The timer 7 interrupt control register (TM7ICR) controls interrupt level of timer 7 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

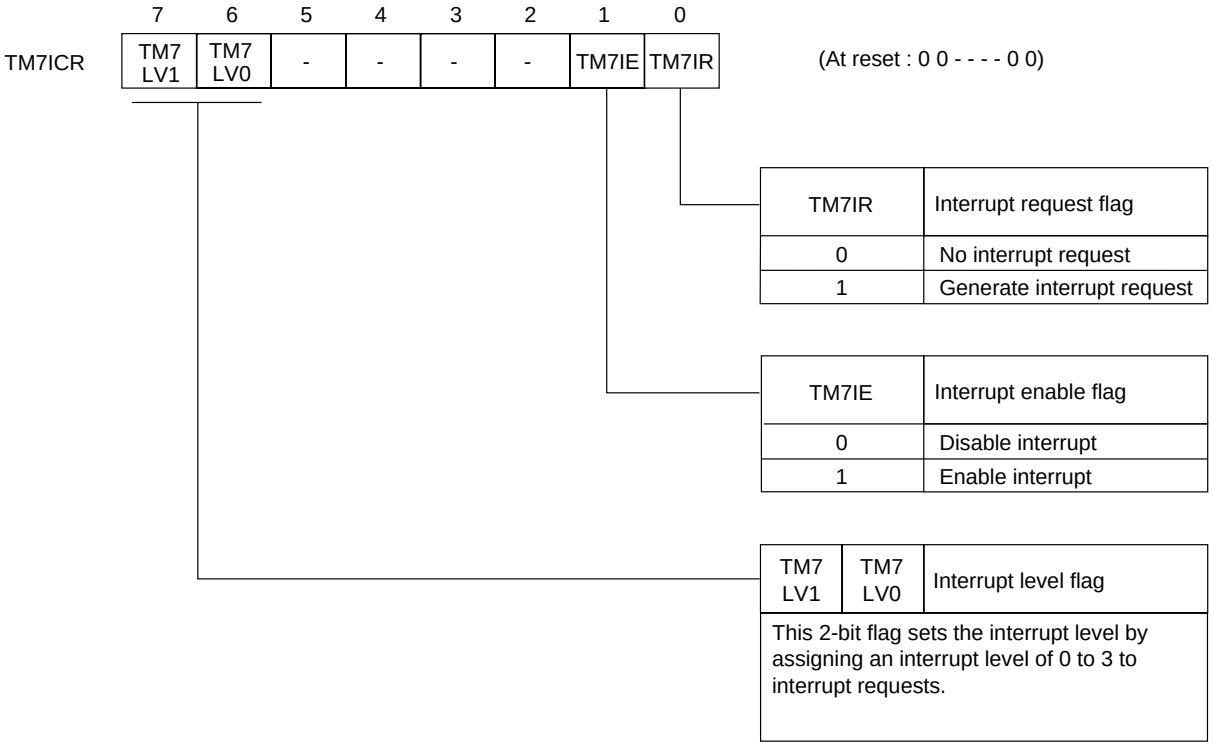


Figure 3-2-17 Timer 7 Interrupt Control Register (TM7ICR : x'03FF1', R/W)

■Timer 7 Compare Register 2-match Interrupt Control Register (T7OC2ICR)

The timer 7 compare register 2-match interrupt control register (T7OC2ICR) controls interrupt level of timer 7 compare register 2-match interrupt , interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

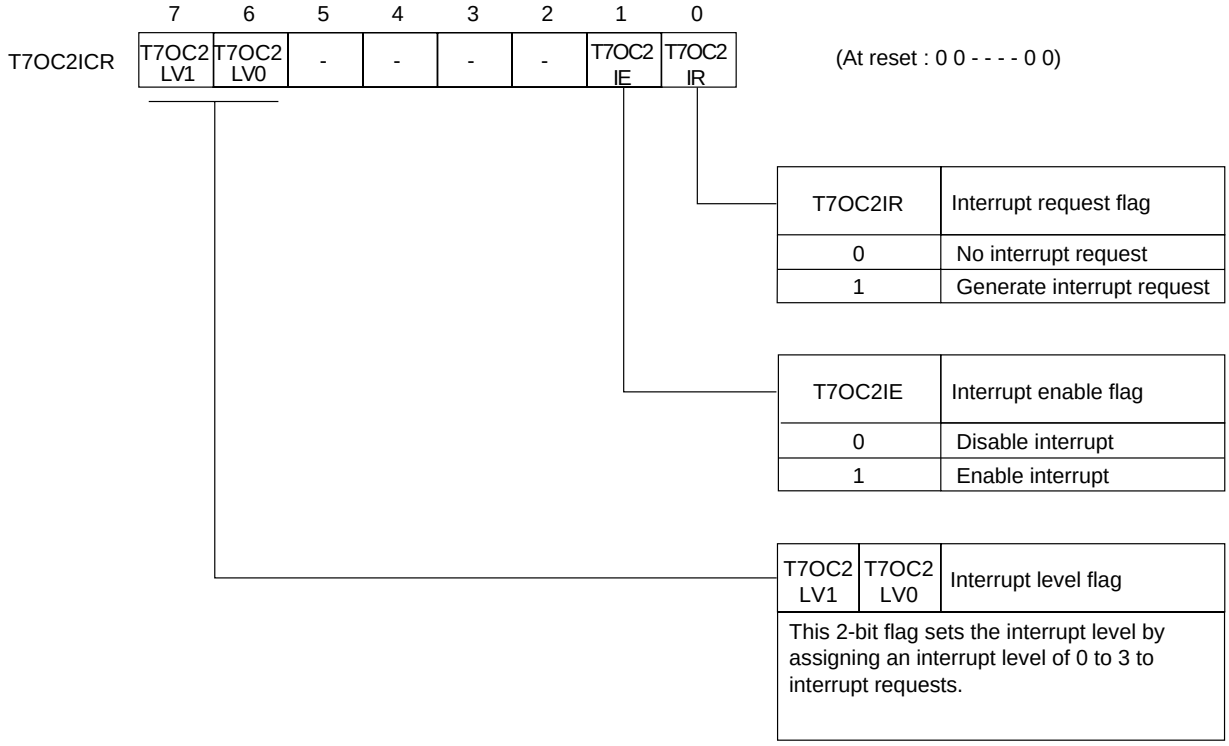


Figure 3-2-18 Timer 7 Compare Register 2-match Interrupt Control Register (T7OC2ICR : x'03FF2', R/W)

■Timer 8 Interrupt Control Register (TM8ICR)

The timer 8 interrupt control register (TM8ICR) controls interrupt level of timer 8 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

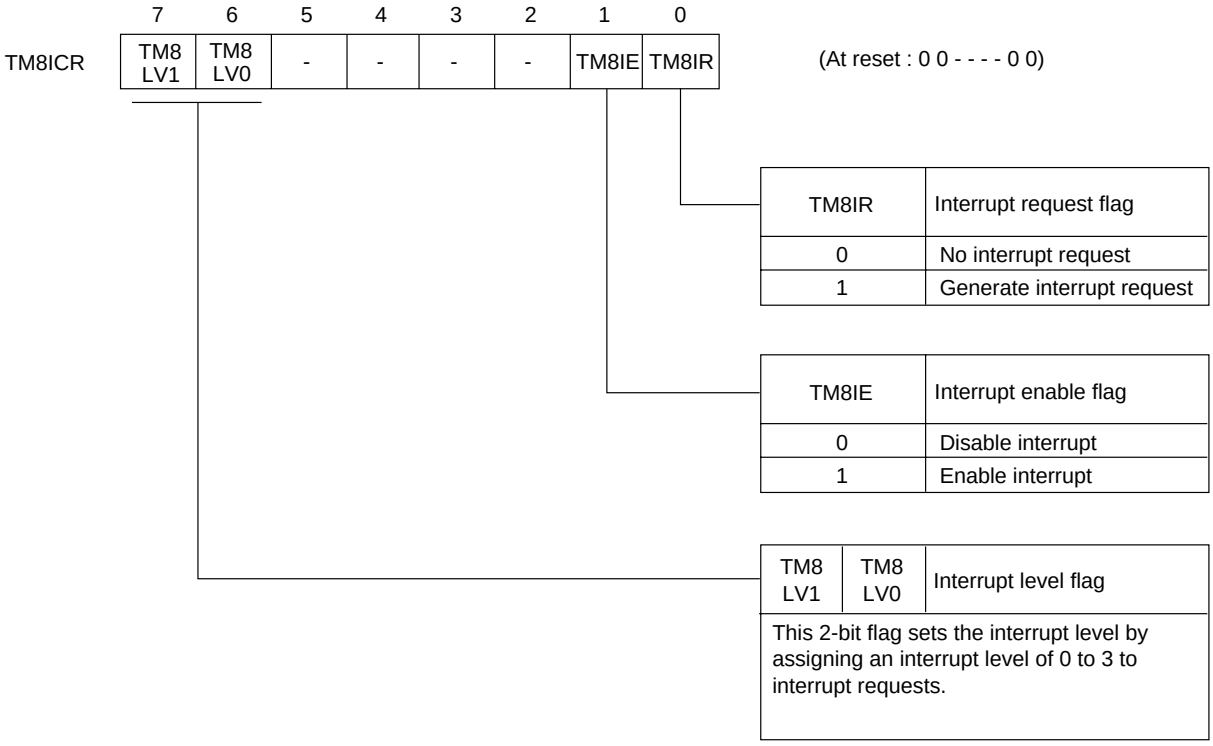


Figure 3-2-19 Timer 8 Interrupt Control Register (TM8ICR : x'03FF3', R/W)

■Timer 8 Compare Register 2-match Interrupt Control Register (T8OC2ICR)

The timer 8 compare register 2-match interrupt control register (T8OC2ICR) controls interrupt level of timer 8 compare register 2-match interrupt , interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

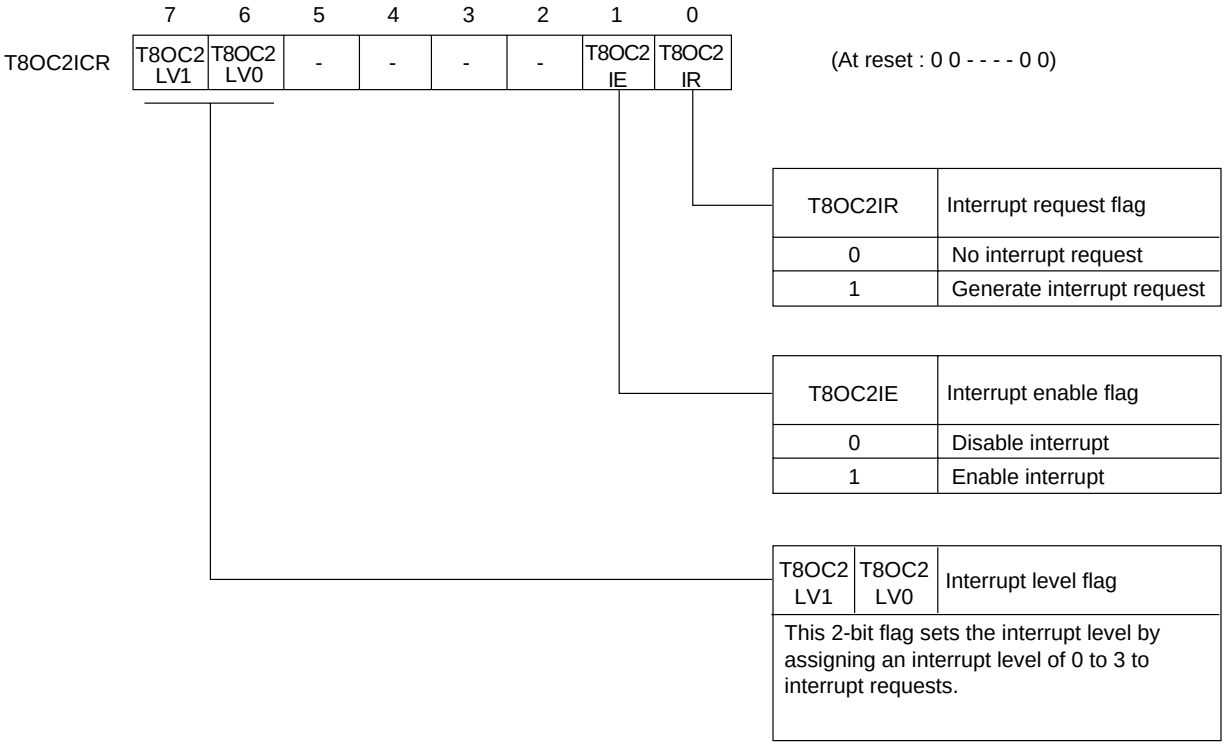


Figure 3-2-20 Timer 8 Compare Register 2-match Interrupt Control Register (T8OC2ICR : x'03FF4', R/W)

■Serial 0 Interrupt Control Register 1 (SC0RICR)

The serial 0 interrupt control register 1 (SC0RICR) controls interrupt level of serial 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

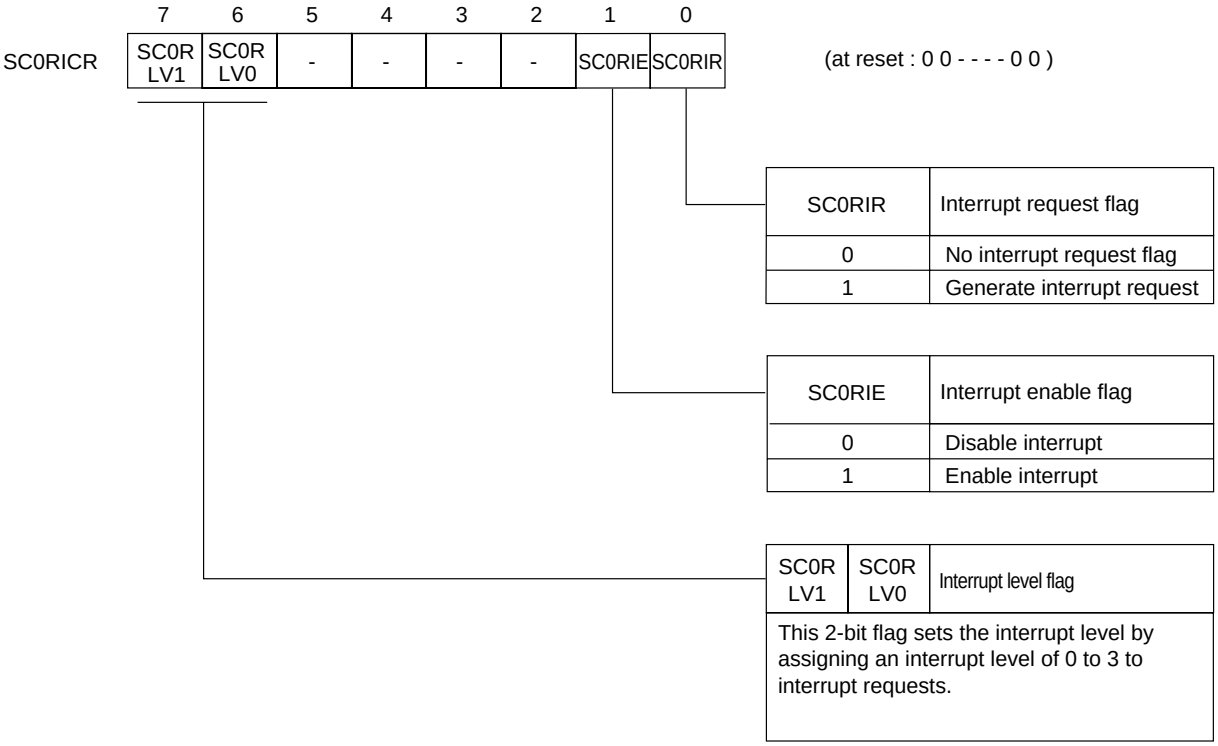


Figure 3-2-21 Serial 0 Interrupt Control Register 1 (SC0RICR : x'03FF5', R/W)

■Serial 0 Interrupt Control Register 2 (SC0TICR)

The serial 0 interrupt control register 2 (SC0TICR) controls interrupt level of serial 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

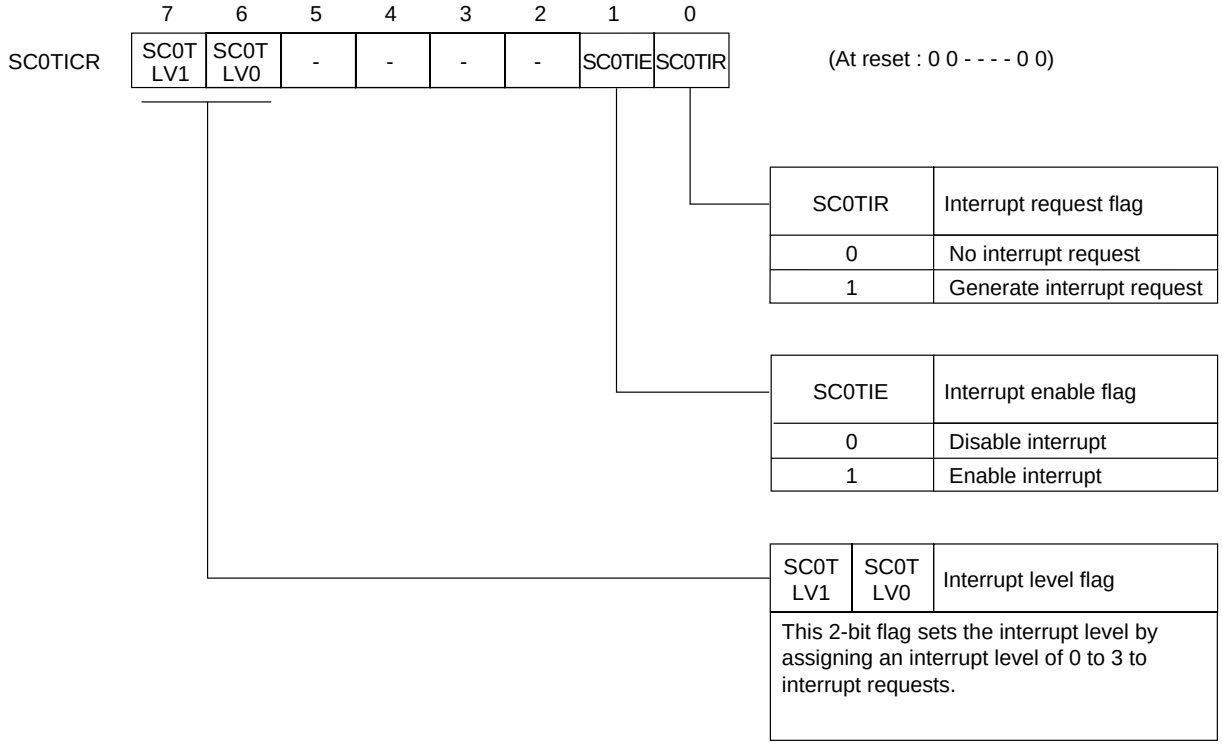


Figure 3-2-22 Serial 0 Interrupt Control Register 2 (SC0TICR : x'03FF6', R/W)

■Serial 2 Interrupt Control Register (SC2ICR)

The serial 2 interrupt control register (SC2ICR) controls interrupt level of serial 2 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

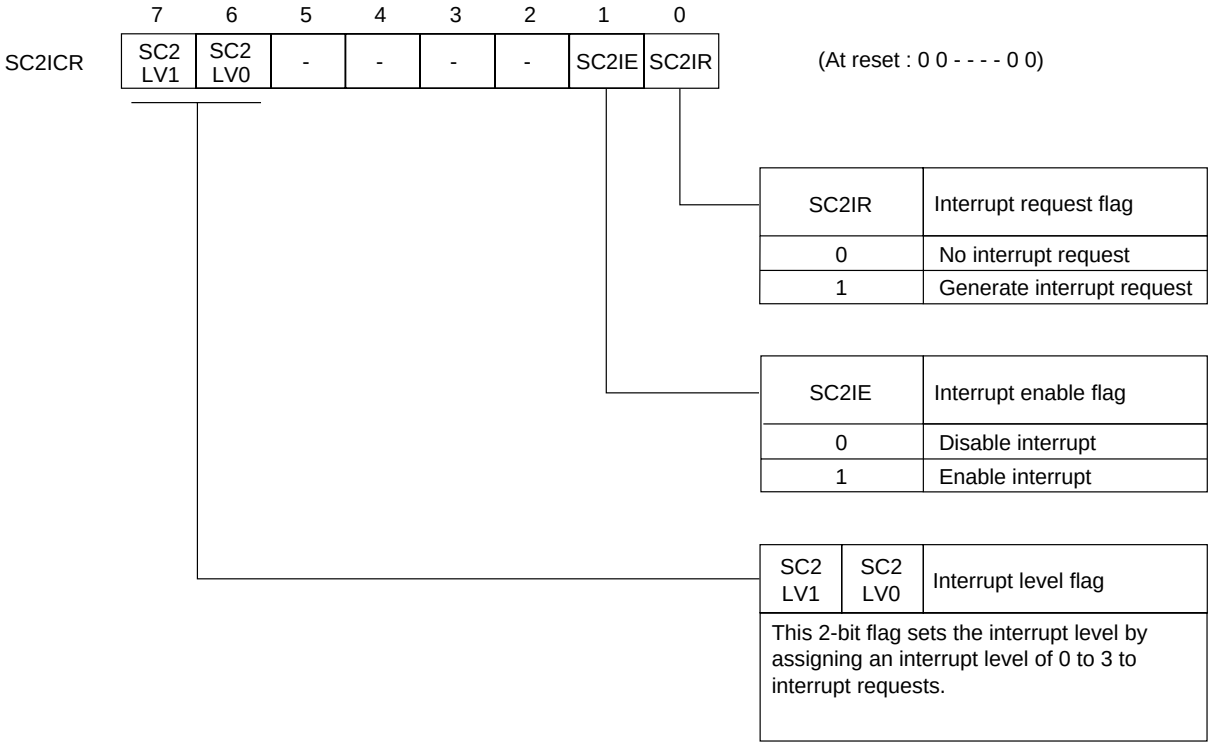


Figure 3-2-23 Serial 2 Interrupt Control Register (SC2ICR : x'03FF8', R/W)

■A/D Conversion Interrupt Control Register (ADICR)

The A/D conversion interrupt control register (ADICR) controls interrupt level of A/D conversion interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

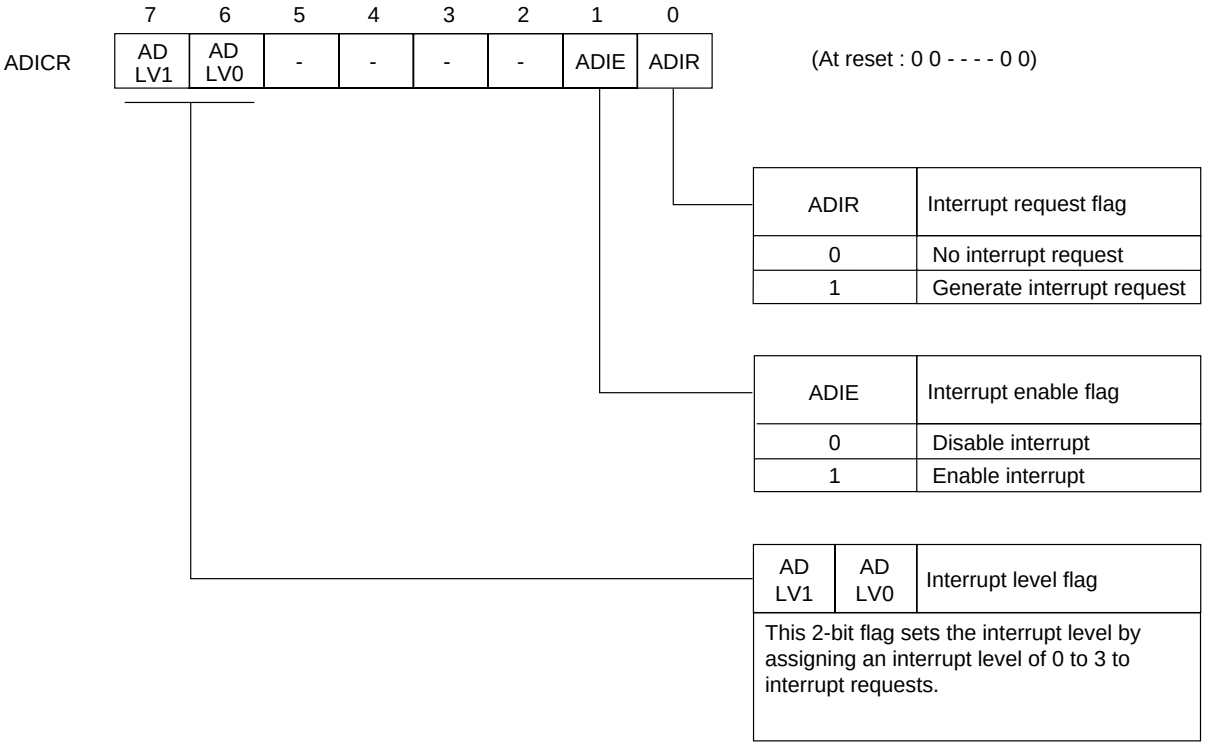


Figure 3-2-24 A/D Conversion Interrupt Control Register (ADICR : x'03FFA', R/W)

3-3 External Interrupts

There are 8 external interrupts in this LSI. The circuit (external interrupt interface), operates the external interrupt input signal, is built-in between the external interrupt input pin and the external interrupt block. This external interrupt interface can manage to do with any kind of external interrupts.

3-3-1 Overview

Table 3-3-1 shows the list of functions which external interrupts 0 to 7 are used.

Table 3-3-1 External Interrupt Functions

	External interrupt 0 (IRQ0)	External interrupt 1 (IRQ1)	External interrupt 2 (IRQ2)	External interrupt 3 (IRQ3)	External interrupt 4 (IRQ4)	External interrupt 5 (IRQ5)	External interrupt 6 (IRQ6)	External interrupt 7 (IRQ7)
External interrupt input pin	P20	P21	P22	P23	P24 (also served as key interrupt)	-	P30	P31
Programmable active edge interrupt	√	√	√	√	√	-	√	√
Both edges interrupt	-	-	√	√	-	√	√	√
Key input interrupt	-	-	-	-	√ (P40-P47)	√ (P00-P05)	-	-
Noise filter built-in	√	√	-	-	-	-	-	-
AC zero cross detection	-	√	-	-	-	-	-	-

3-3-2 Block Diagram

■External Interrupt 0 Interface, External Interrupt 1 Interface, Block Diagram

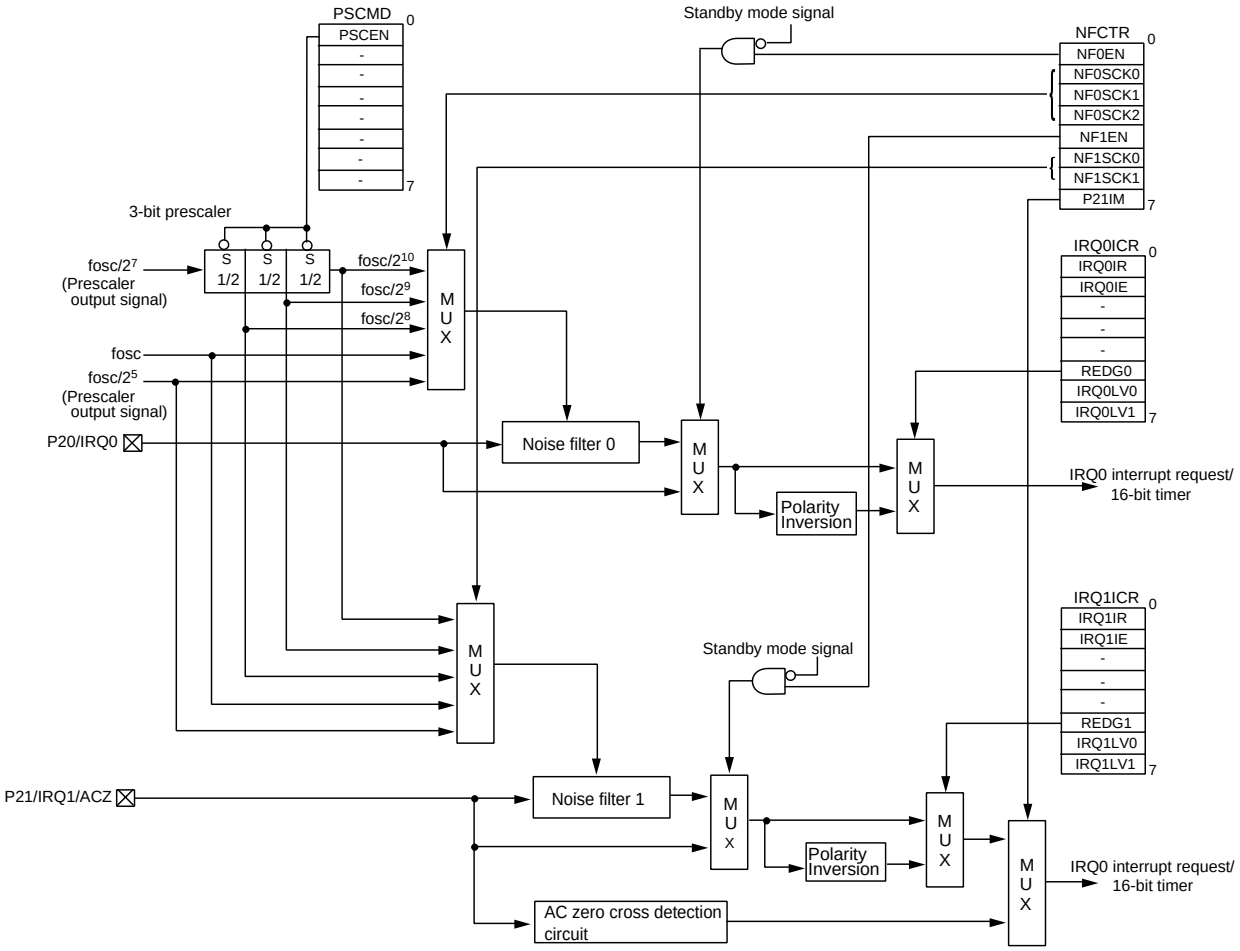


Figure 3-3-1 External Interrupt 0 Interface and External Interrupt 1 Interface, Block Diagram

■External Interrupt 2 Interface, External Interrupt 3 Interface, Block Diagram

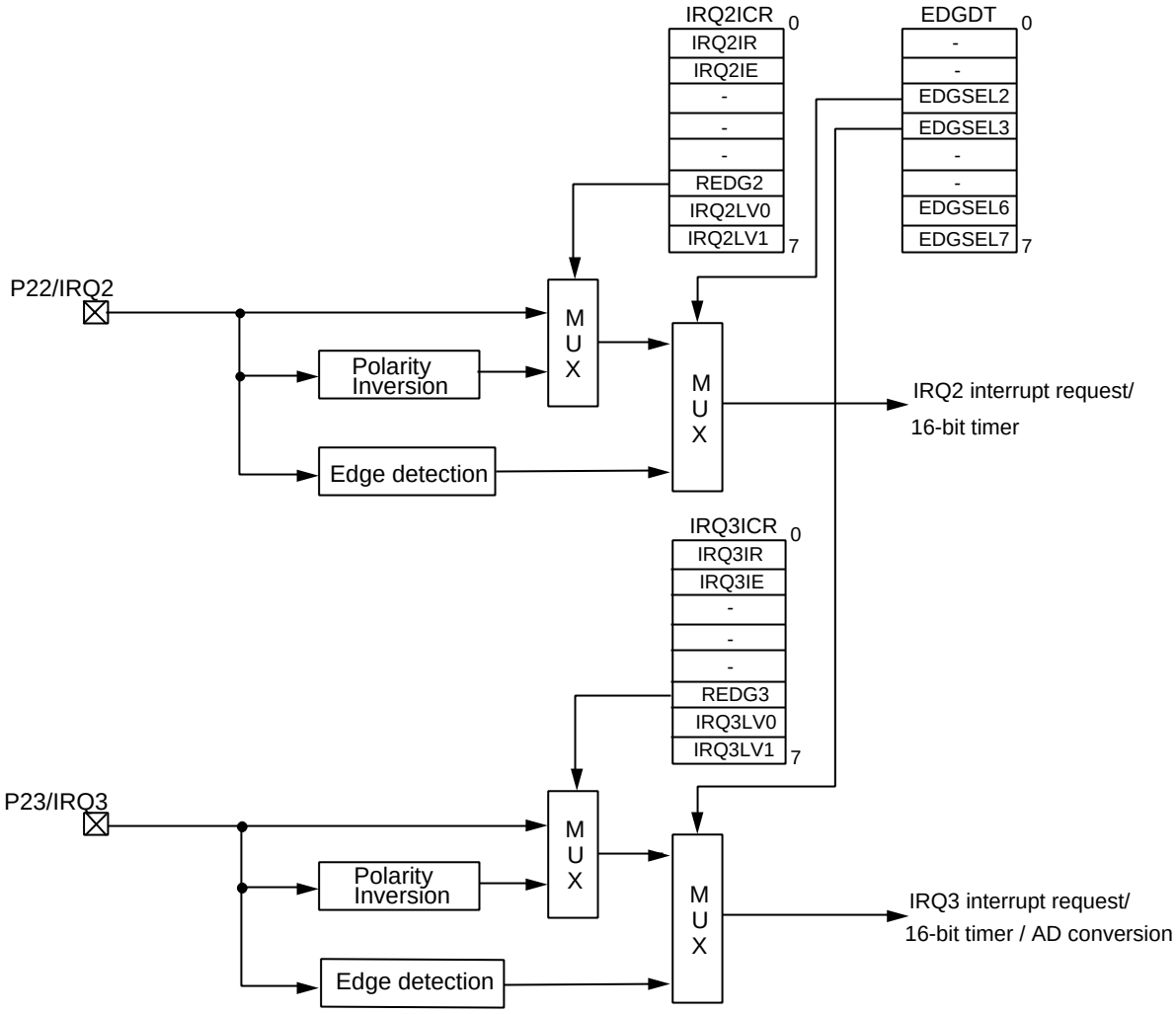


Figure 3-3-2 External Interrupt 2 Interface and External Interrupt 3 Interface, Block Diagram

■External Interrupt 6 Interface, External Interrupt 7 Interface, Block Diagram

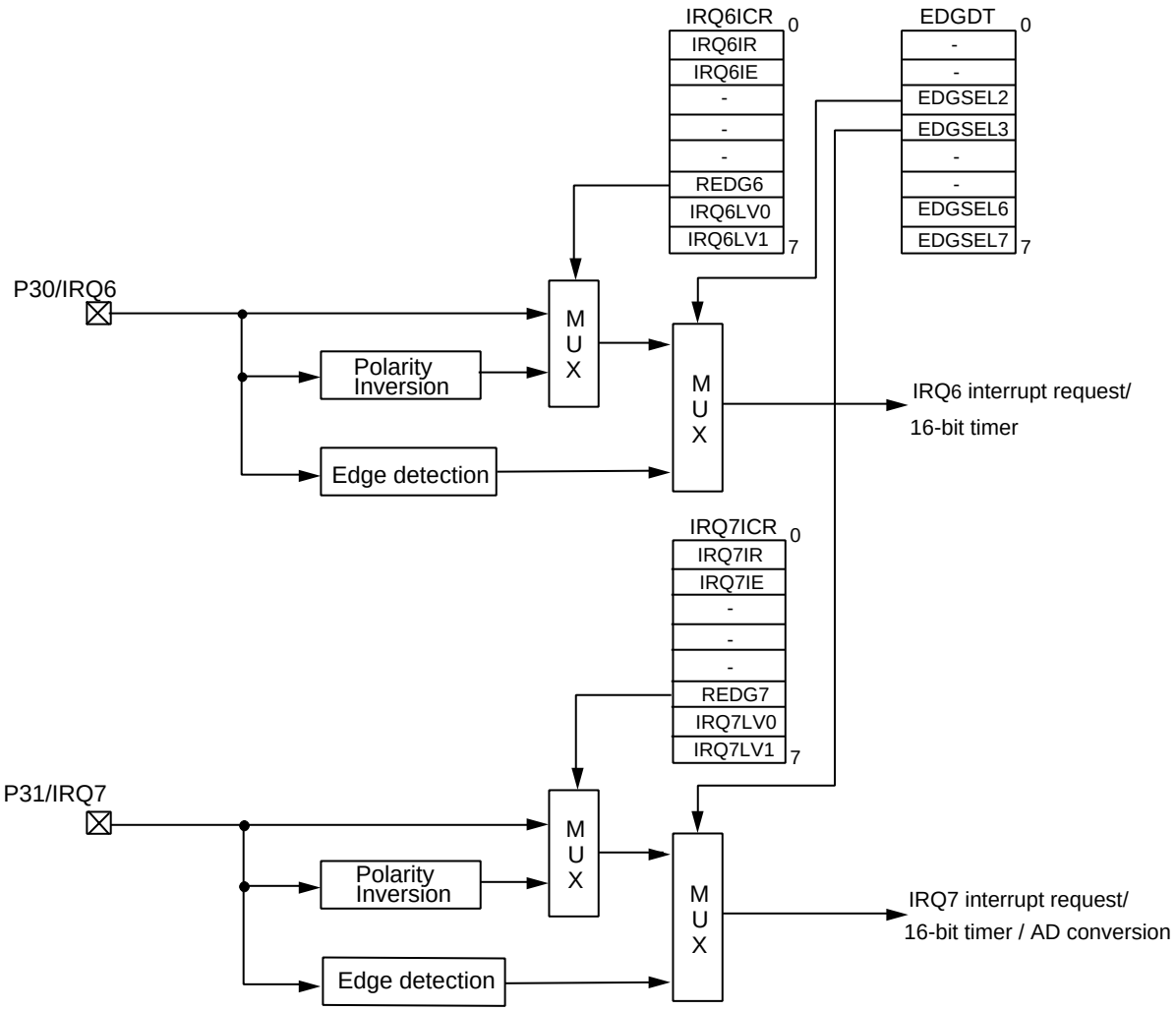


Figure 3-3-3 External Interrupt 6 Interface and External Interrupt 7 Interface, Block Diagram

■External Interrupt 4 Interface, Block Diagram

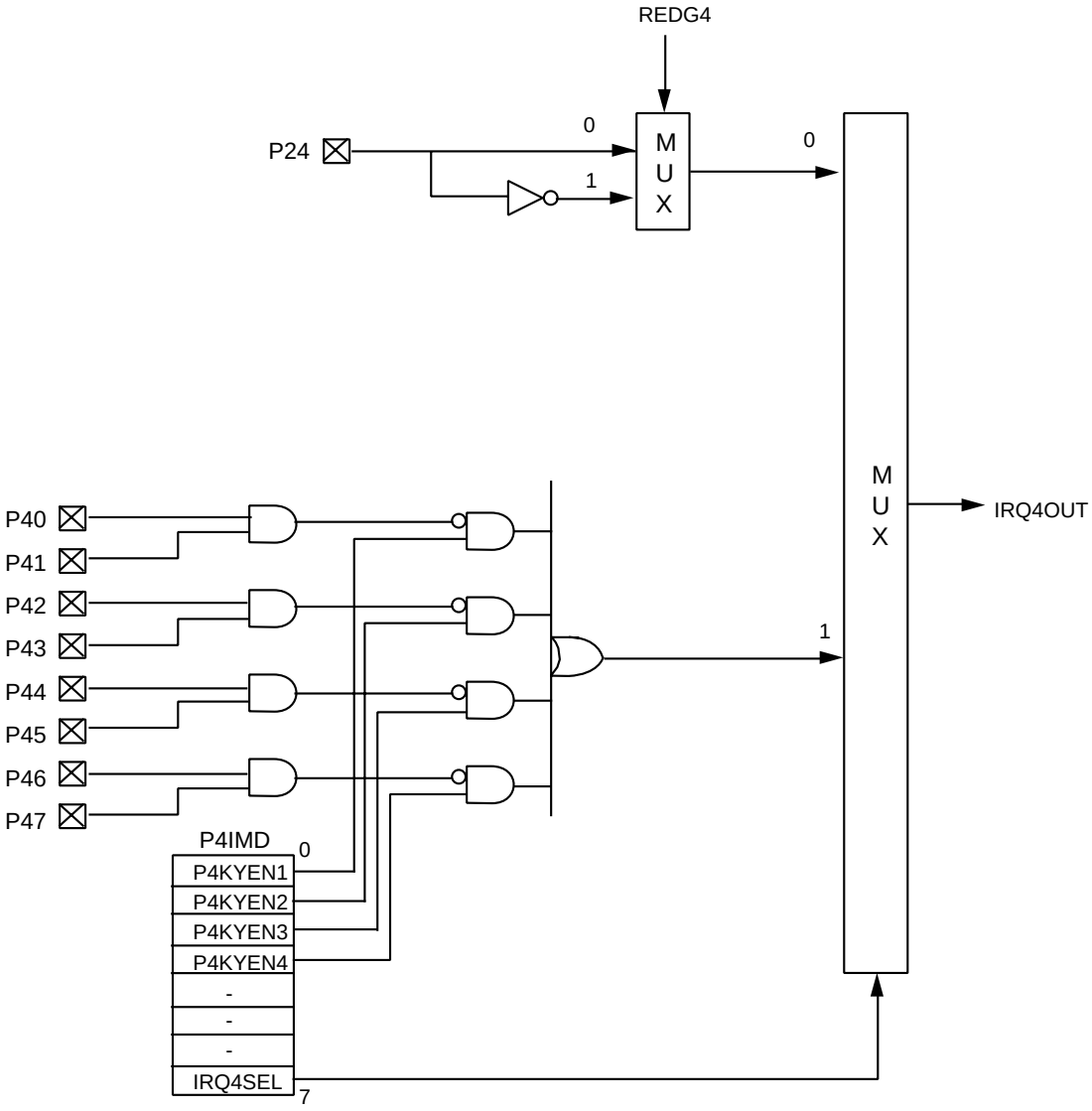


Figure 3-3-4 External Interrupt 4 Interface, Block Diagram

■External Interrupt 5 Interface, Block Diagram

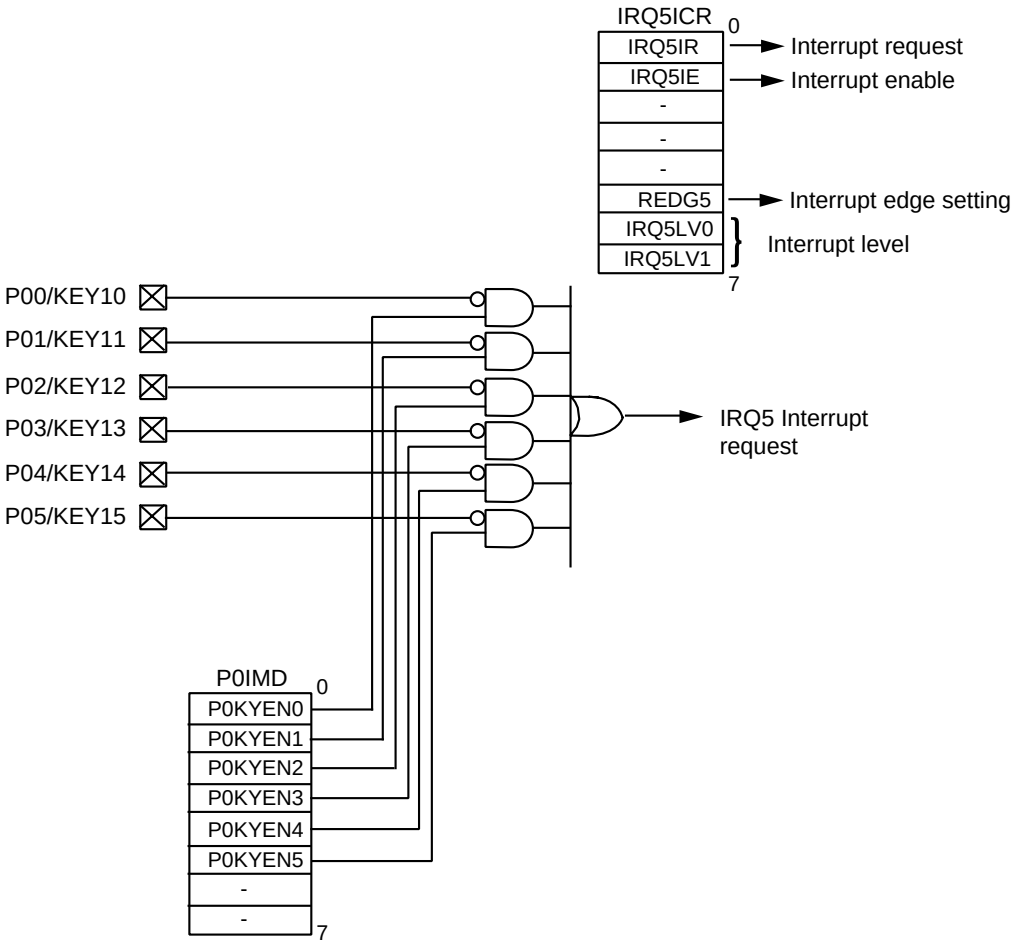


Figure 3-3-5 External Interrupt 5 Interface, Block Diagram

3-3-3 Control Registers

The external Interrupt input signals, which passed through each external interrupt interface 0 to 7 generate interrupt requests.

External interrupt 0 to 7 interface are controlled by the external interrupt control register (IRQnICR). External interrupt interface 0 to 1 are controlled by the noise filter control register (NFCTR), external interrupt interface 2, 3 and 6, 7 are controlled by the both edges interrupt control register (EDGDT), and external interrupt interface 4 is controlled by the port 4 key interrupt control register (P4IMD). External interrupt interface 5 is controlled by the port 0 key interrupt control register (P0IMD).

Table 3-3-2 shows the list of registers, which control external interrupt 0 to 7.

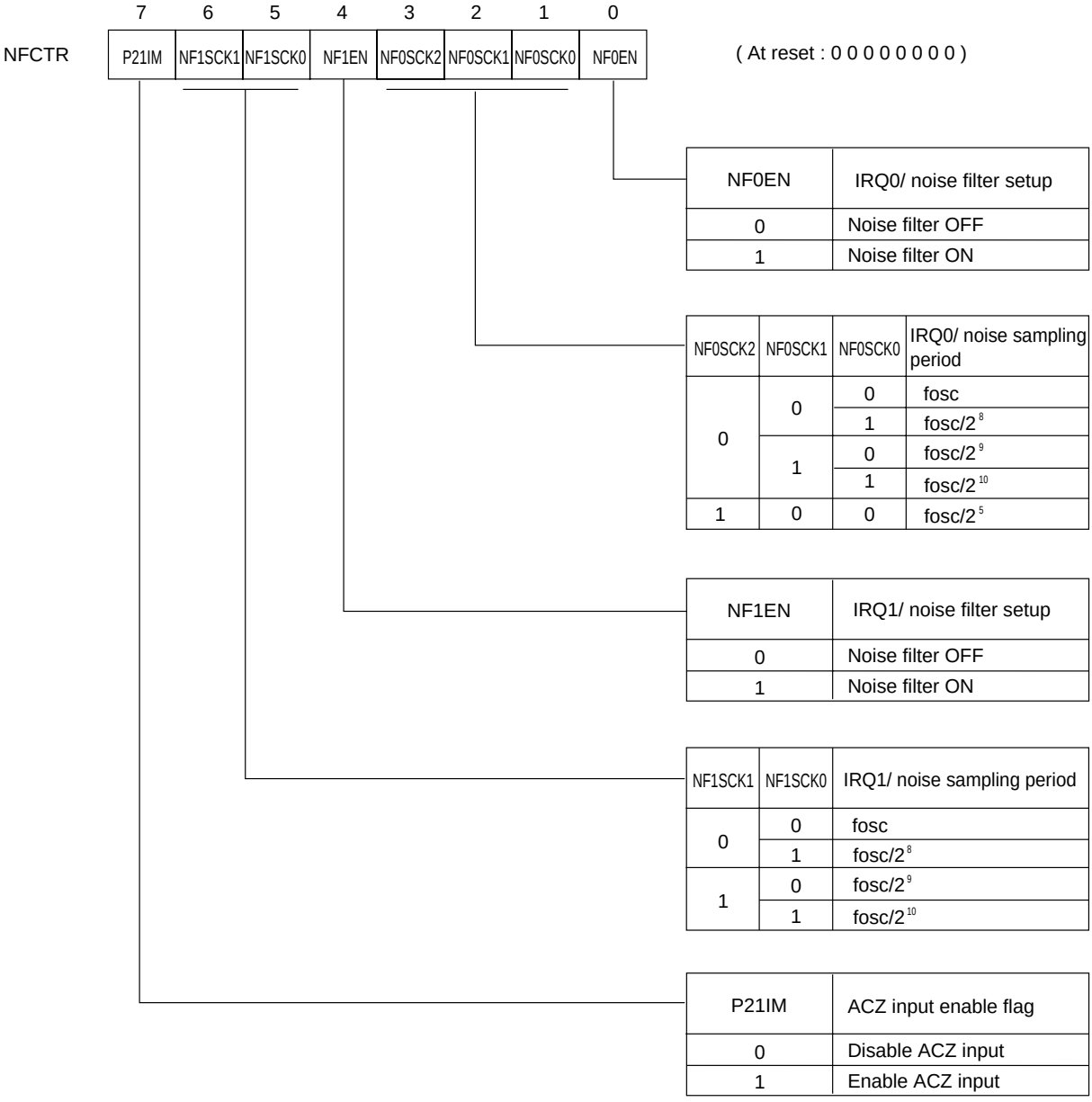
Table 3-3-2 External Interrupt Control Register

External Interrupt	Register	Address	R/W	Function	Page
External interrupt 0	IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III - 17
	NFCTR	x'03F8E'	R/W	Noise filter control register	III - 47
External interrupt 1	IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III - 18
	NFCTR	x'03F8E'	R/W	Noise filter control register	III - 47
External interrupt 2	IRQ2ICR	x'03FE4'	R/W	External interrupt 2 control register	III - 19
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III - 48
External interrupt 3	IRQ3ICR	x'03FE5'	R/W	External interrupt 3 control register	III - 20
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III - 48
External interrupt 4	IRQ4ICR	x'03FE6'	R/W	External interrupt 4 control register	III - 21
	P4IMD	x'03F3E'	R/W	Port 4 key interrupt control register	III - 50
External interrupt 5	IRQ5ICR	X'03FE7'	R/W	External interrupt 5 control register	III - 22
	P0IMD	X'03F4D'	R/W	Port 0 key interrupt control register	III - 49
External interrupt 6	IRQ6ICR	X'03FE8'	R/W	External interrupt 6 control register	III - 23
	EDGDT	X'03F8F'	R/W	Both edges interrupt control register	III - 48
External interrupt 7	IRQ7ICR	X'03FED'	R/W	External interrupt 7 control register	III - 28
	EDGDT	X'03F8F'	R/W	Both edges interrupt control register	III - 48

R/W : Readable / Writable.

■Noise Filter Control Register (NFCTR)

The noise filter control register (NFCTR) set the noise remove function to IQR0 and IRQ1 and also selects the sampling cycle of noise remove function. And this register also set the AC zero cross detection function to IRQ1.



NF0EN	IRQ0/ noise filter setup
0	Noise filter OFF
1	Noise filter ON

NF0SCK2	NF0SCK1	NF0SCK0	IRQ0/ noise sampling period
0	0	0	fosc
		1	fosc/2^8
	1	0	fosc/2^9
		1	fosc/2^{10}
1	0	0	fosc/2^5

NF1EN	IRQ1/ noise filter setup
0	Noise filter OFF
1	Noise filter ON

NF1SCK1	NF1SCK0	IRQ1/ noise sampling period
0	0	fosc
	1	fosc/2^8
1	0	fosc/2^9
	1	fosc/2^{10}

P21IM	ACZ input enable flag
0	Disable ACZ input
1	Enable ACZ input

Figure 3-3-6 Noise Filter Control Register (NFCTR : x'03F8E', R/W)

■Both Edges Interrupt Control Register (EDGDT)

The both edges interrupt control register (EDGDT) selects interrupt edges of IRQ2, IRQ3 and IRQ6, IRQ7. Interrupts are generated at both edges, or at single edge. The external interrupt control register (IRQ2ICR, IRQ3ICR,IRQ6ICR, IRQ7ICR) specifies whether interrupts are generated.

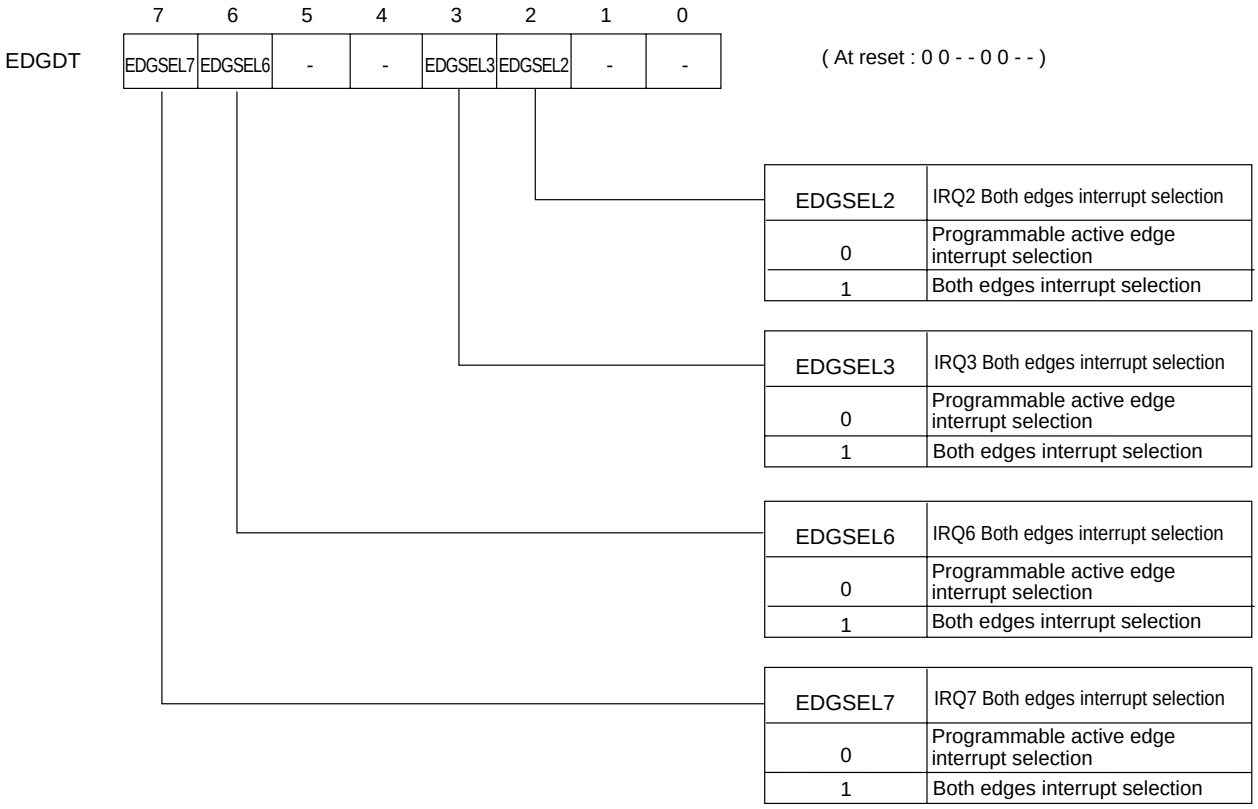

7 6 5 4 3 2 1 0
EDGDT
EDGSEL7 EDGSEL6 - - EDGSEL3 EDGSEL2 - -
(At reset : 0 0 - - 0 0 - -)
EDGSEL2 IRQ2 Both edges interrupt selection
0 Programmable active edge interrupt selection
1 Both edges interrupt selection
EDGSEL3 IRQ3 Both edges interrupt selection
0 Programmable active edge interrupt selection
1 Both edges interrupt selection
EDGSEL6 IRQ6 Both edges interrupt selection
0 Programmable active edge interrupt selection
1 Both edges interrupt selection
EDGSEL7 IRQ7 Both edges interrupt selection
0 Programmable active edge interrupt selection
1 Both edges interrupt selection

Figure 3-3-7 Both Edges Interrupt Control Register (EDGDT : x'03F8F', R/W)

■Port 0 Key Interrupt Control Register (P0IMD)

The port 0 key interrupt control register (P0IMD) selects if key interrupt is accepted. Also, this register assigns port0 pin to key interrupt in 1-bit unit.

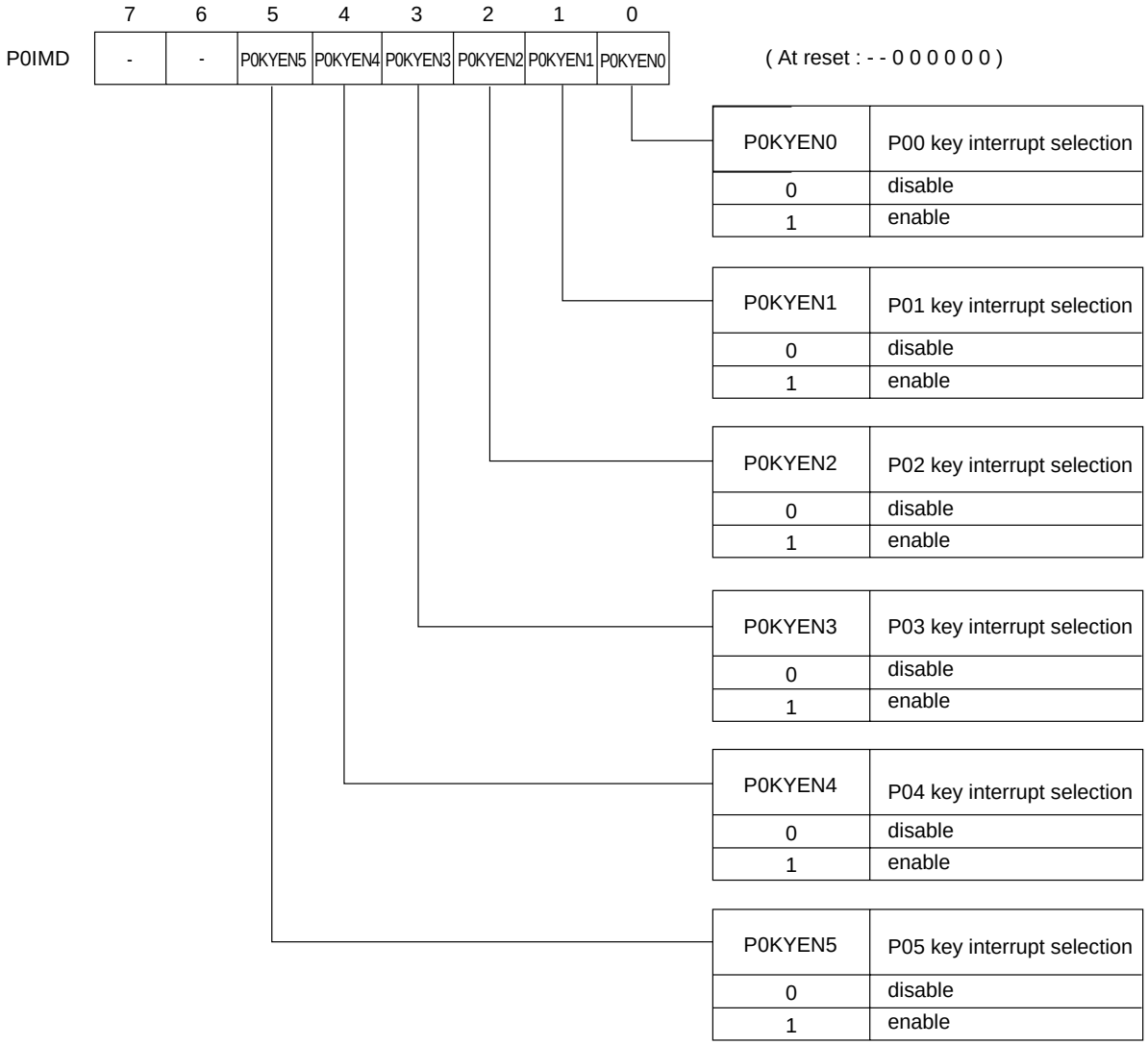


Figure 3-3-8 Port 0 Key Interrupt Control Register (P0IMD : x'03F4D', R/W)

■Port 4 Key Interrupt Control Register (P4IMD)

The port 4 key interrupt control register (P4IMD) selects if key interrupt is accepted, and if external interrupt IRQ4 is accepted. Also, this register assigns port4 pin to key interrupt in 1-bit unit.

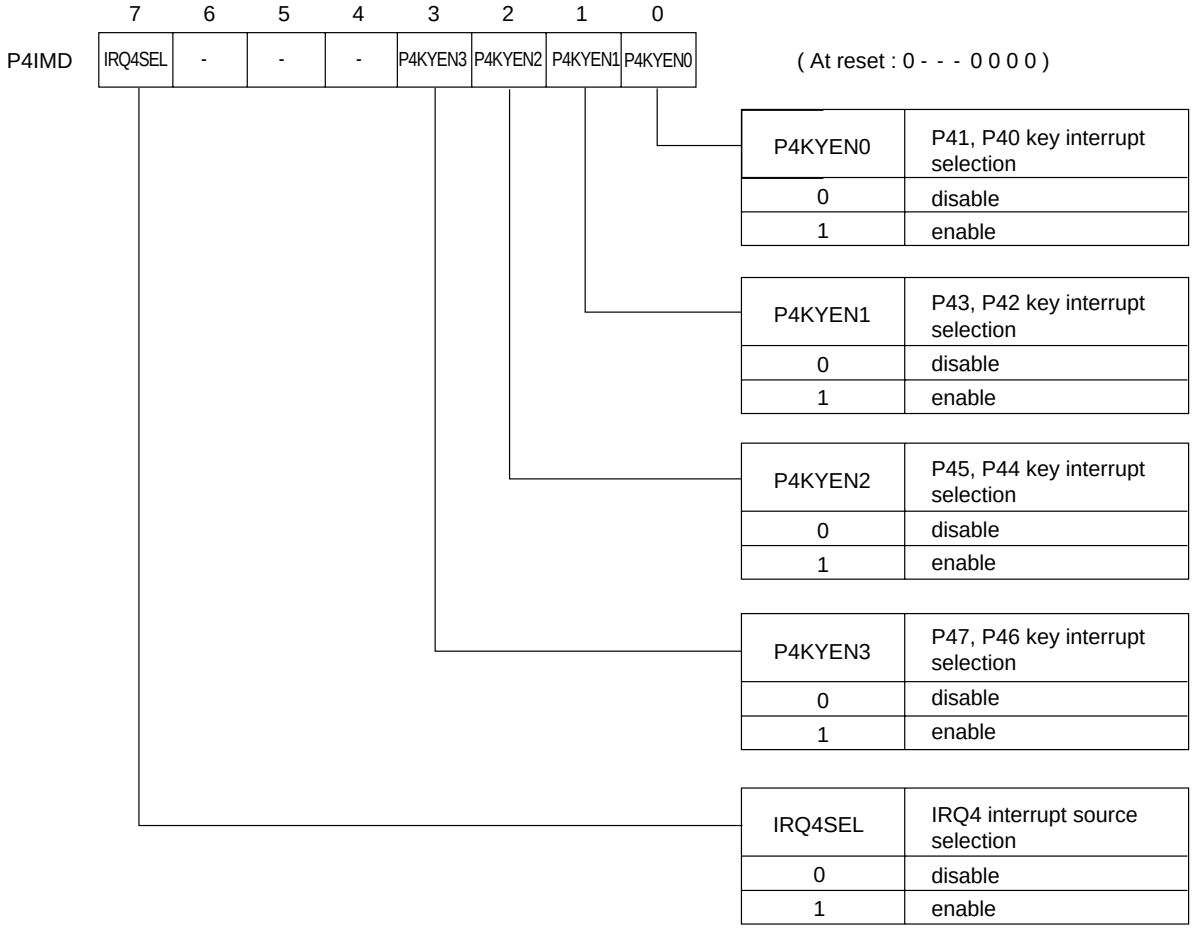

7 6 5 4 3 2 1 0
P4IMD
IRQ4SEL - - - P4KYEN3 P4KYEN2 P4KYEN1 P4KYEN0
(At reset : 0 - - - 0 0 0 0)
P4KYEN0 P41, P40 key interrupt selection
0 disable
1 enable
P4KYEN1 P43, P42 key interrupt selection
0 disable
1 enable
P4KYEN2 P45, P44 key interrupt selection
0 disable
1 enable
P4KYEN3 P47, P46 key interrupt selection
0 disable
1 enable
IRQ4SEL IRQ4 interrupt source selection
0 disable
1 enable

Figure 3-3-7 Port 4 Key Interrupt Control Register (P4IMD : x'03F3E', R/W)

3-3-4 Programmable Active Edge Interrupt

■Programmable Active Edge Interrupts (External interrupts 0 to 7)
Through register settings, external interrupts 0 to 7 are generated at either the rising or falling edge of the IRQ input signal. And this function can generate interrupt at the selected edge.

■Programmable Active Edge Interrupt Setup Example (External interrupt 0 to 7)
External interrupt 0 (IRQ0) is generated at the rising edge of the input signal from P20.
The table below provides a setup example for IRQ0.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(1) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the rising edge as the active edge for interrupts.
(2) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(2) Set the interrupt priority level in the IRQ0LV1-0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [☞ Chapter 3. 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(3) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

External interrupt 0 is generated at the rising edge of the input signal from P20.

The Interrupt request flag can be set at switching the interrupt edge, so specify the interrupt valid edge before the interrupt permission.

The external interrupt pin is recommended to be pull-up in advance.

When the programmable active edge interrupt is specified for external interrupt 2, 3, 6, 7 (IRQ2, IRQ3, IRQ6, IRQ7), set the EDGSELn flag of the both edge interrupt control register (EDGDT) to "0".

3-3-5 Both Edges Interrupt

■Both Edges Interrupt (External interrupts 2, 3, 6 and 7)
Both edges interrupt can generate interrupt at both the falling edge and the rising edge by the input signal from external input pins. CPU also can be returned from standby mode.

■Both Edges Interrupt Setup Example (External interrupts 2, 3, 6 and 7)
External interrupt 2 (IRQ2) is generated at the both edges of the input signal from P22 pin.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the both edges interrupt. EDGDT (x'3F8F') bp2 : EDGSEL2 = 1	(1) Set the EDGSEL2 flag of the both edges interrupt control register (EDGDT) to "1" to select the both edges interrupt.
(2) Set the interrupt level. IRQ2ICR (x'3FE4') bp7-6 : IRQ2LV1- 0 = 10	(2) Set the interrupt level by the IRQ2LV1-0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR). [☞ Chapter 3 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ2ICR (x'3FE4') bp1 : IRQ2IE = 1	(3) Set the IRQ2IE flag of the IRQ2ICR register to "1" to enable the interrupt.

At the both edge of the input signal from P22 pin, an external interrupt 2 is generated .

When the both edge interrupt is selected, the interrupt request is generated at the both edge, regardless of the REDGn flag of the external interrupt control register (IRQnICR).

The interrupt request flag may be set at switching the interrupt edge. So, clear the interrupt request flag before the interrupt acceptance. Also, select the both edge interrupt before the interrupt acceptance.

The external interrupt pin is recommended to be pull-up, in advance.

3-3-6 Key Input Interrupt

■Key Input Interrupt (External interrupt 4, 5)

This LSI can set port 4 (P40 to P47) pin by 2 bit, and set port 0 (P00 to P05) pin by 1 bit to key input pin. Port 4 key input interrupt can generate an interrupt at the falling edge, if at least 1 key input pin outputs low level. Port 0 key input interrupt can generate an interrupt at the rising edge or the falling edge, if at least 1 key input pin outputs high level or low level.

Port 4 key input pin should be pull-up in advance.
Port 0 key input pin should be pull-up in advance when falling edge is selected and be pull-down when rising edge is selected.

■Key Input Interrupt Setup Example (External interrupt 4, 5)

After P40 to P47 of port 4 are set to key input pins and key is input (low level), the external interrupt 4 (IRQ4) is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the key input pin to input. P4DIR (x'3F34') bp7-0 : P4DIR7-0 = 0000	(1) Set the P4DIR7-0 flag of the port 4 direction control register (P4DIR) to "0000" to set P40 to P47 pins to input pins.
(2) Set the pull-up resistance. P4PLU (x'3F44') bp7-0 : P4PLU7-0 = 1111	(2) Set the P4PLU7-0 flag of the port 4 pull-up resistance control register (P4PLU) to "1111" to add the pull-up resistors to P40 to P47 pins.
(3) Select the key input pin. P4IMD (x'3F3E') bp3-0 : P4KYEN3-0= 1111 bp7-4 : P4KYEN7-4= 1000	(3) Set the P4KYEN3-0 flag of the port 4 key interrupt control register (P4IMD) to "1111" to set P40 to P47 pins to key input pins. Set "1000" to the P4KYEN7-4 flag to set P4 key interrupt.
(4) Set the interrupt level. IRQ4ICR (x'3FE6') bp7-6 : IRQ4LV1-0= 10	(4) Set the interrupt level by the IRQ4LV1-0 flag of the IRQ4ICR register. If the interrupt request flag has been already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ4ICR (x'3FE6') bp1 : IRQ4IE = 1	(5) Set the IRQ4IE flag of the IRQ4ICR register to "1" to enable the interrupt.

If there is at least one input signal, from the P40 to P47 pins, shows low level, the external interrupt 4 is generated at the falling edge.

The key input should be setup before the interrupt is accepted.

3-3-7 Noise Filter

■Noise Filter (External interrupts 0 and 1)

Noise filter reduce noise by sampling the input waveform from the external interrupt pins (IRQ0, IRQ1). Its sampling cycle can be selected from 5 types (fosc, fosc/2^5, fosc/2^8, fosc/2^9, fosc/2^{10}).

■Noise Remove Selection (External interrupts 0 and 1)

Noise remove function can be selected by setting the NFnEN flag of the noise filter control register (NFCTR) to "1".

Table 3-3-3 Addition of Noise Remove Function

NFnEN	IRQ0 input (P20)	IRQ1 input (P21)
0	IRQ0 Noise filter OFF	IRQ1 Noise filter OFF
1	IRQ0 Noise filter ON	IRQ1 Noise filter ON

■Sampling Cycle Setup (External interrupts 0 and 1)

The sampling cycle of noise remove function can be set by the NFnSCK 2- 0 flag of the NFCTR register.

Table 3-3-4 Sampling Cycle / Time of Noise Remove Function

NFnCKS2	NFnCKS1	NFnCKS0	Sampling cycle	High-frequency oscillation			
				fosc=20 MHz		fosc=8 MHz	
0	0	0	fosc	20 MHz	50 ns	8 MHz	125 ns
		1	fosc/2^8	78.13 kHz	12.80 µs	31.25 kHz	32 µs
	1	0	fosc/2^9	39.06 kHz	25.60 µs	15.62 kHz	64 µs
		1	fosc/2^{10}	19.53 kHz	51.20 µs	7.81 kHz	128 µs
1	0	0	fosc/2^5	625 kHz	1.60 µs	250 kHz	4 µs

■Noise Remove Function Operation (External interrupts 0 and 1)

After sampling the input signal to the external interrupt pins (IRQ0, IRQ1) with the set sampling time, if the same level comes continuously three times, that level is sent to the inside of LSI. If the same level does not come continuously three times, the previous level is sent. It means that only the signal with the amplitude of longer than " Sampling time X 3 sampling clock " can pass through the noise filter, and other signals with amplitude shorter than this are removed, because those are regarded as noise.

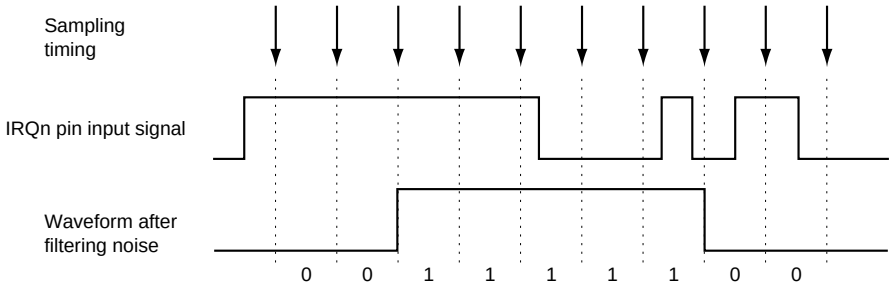


Figure 3-3-10 Noise Remove Function Operation

Noise filter can not be used at STOP mode, HALT mode and SLOW mode.

■Noise Filter Setup Example (External interrupt 0 and 1)

Noise remove function is added to the input signal from P20 pin to generate the external interrupt 0 (IRQ0) at the rising edge. The sampling clock is set to fosc, and the operation state is fosc = 20 MHz. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(1) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the interrupt active edge to the rising edge.
(2) Select the sampling clock. NFCTR (x'3F8E') bp2-1 : NF0SCK2-0 = 000	(2) Select the sampling clock to fosc by the NF0SCK 2-0 flag of the noise filter control register (NFCTR).
(3) Set the noise filter operation. NFCTR (x'3F8E') bp0 : NF0EN = 1	(3) Set the NF0EN flag of the NFCTR register to "1" to add the noise filter operation.
(4) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(4) Set the interrupt level by the IRQ0LV 1- 0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [☞Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(5) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

Note : The above (2) and (3) are set at the same time.

The input signal from the P20 pin generates the external interrupt 0 at the rising edge of the signal, after passing through the noise filter.

The setup of the noise filter should be done before the interrupt is enabled.

The external interrupt pins are recommended to be pull-up in advance.

3-3-8 AC Zero-Cross Detector

This LSI has AC zero-cross detector circuit. The P21 / ACZ pin is the input pin of AC zero-cross detector circuit. AC zero-cross detector circuit output the high level when the input level is at the middle, and outputs the low level at other level.

■AC Zero-Cross Detector (External interrupt 1)
AC zero-cross detector set the IRQ1 pin to the high level when the input signal (P21/ACZ pin) is at intermediate range by AC zero cross detector circuit. At the other level, IRQ1 pin is set to the low level. AC zero-cross detector is set by setting the P21IM flag of the noise filter control register (NFCTR) to "1".

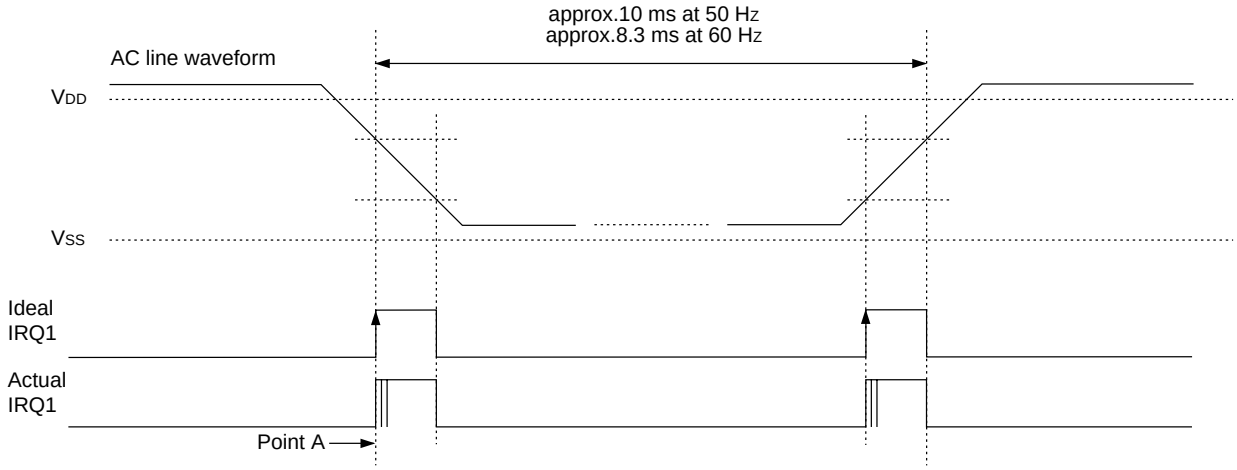


Figure 3-3-11 AC Line Waveform and IRQ1 Generation Timing

Actual IRQ1 interrupt request is generated several times at crossing the 1/2 V_{DD} of AC line waveform. So, the filtering operation by the program is needed.

The interrupt request is generated at the rising edge of the AC zero-cross detector signal.

■AC Zero-Cross Detector Setup Example (External interrupt 1)

AC zero-cross detector generates the external interrupt 1 (IRQ1) by using P21/ACZ pin.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the AC zero-cross detector signal. NFCTR (x'3F8E') bp7 : P21IM = 1	(1) Set the P21IM flag of the noise filter control register (NFCTR) to "1" to select the AC zero-cross detector signal as the external interrupt 1 generation factor.
(2) Set the interrupt level. IRQ1ICR (x'3FE3') bp7-6 : IRQ1LV1-0= 10	(2) Set the interrupt level by the IRQ1LV 1-0 flag of the IRQ1ICR register. If the interrupt request flag has been already set, clear the interrupt flag. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(3) Enable the interrupt. IRQ1ICR (x'3FE3') bp1 : IRQ1IE = 1	(3) Set the IRQ1IE flag of the IRQ1ICR register to "1" to enable the interrupt.

When the input level of the input signal from P21/ACZ pin cross 1/2V_{DD}, the external interrupt 1 is generated.

Chapter 4 I/O Ports

4

4-1 Overview

4-1-1 I/O Port Diagram

A total of 83 pins on this LSI, including those shared with special function pins, are allocated for the 12 I/O ports of port 0 to port 9, port A and port B. Each I/O port is assigned to its corresponding special function register area in memory. I/O ports are operated in byte or bit units in the same way as RAM.

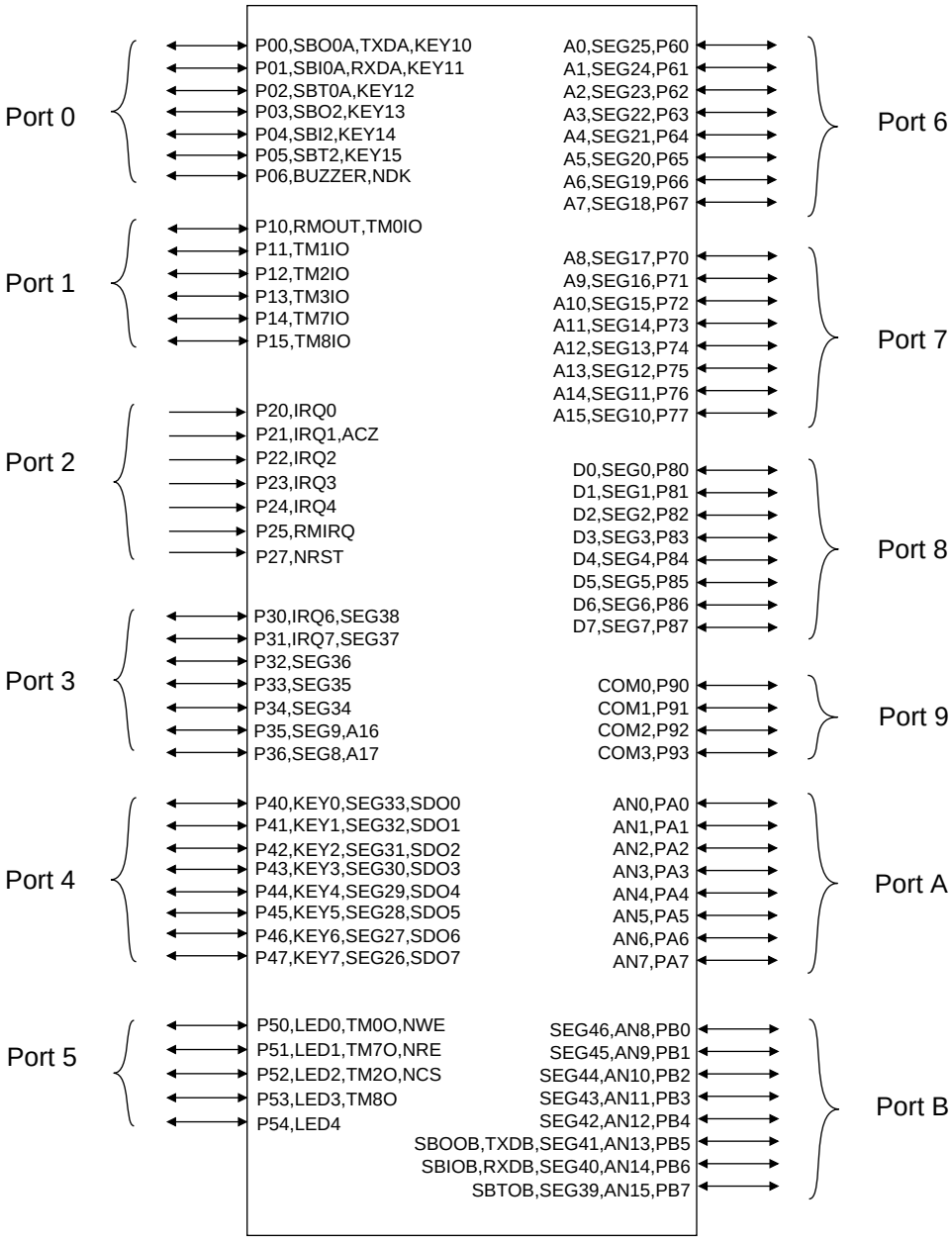


Figure 4-1-1 I/O Port Functions

4-1-2 I/O Port Status at Reset

Table 4-1-1 I/O Port Status at Reset (Single chip mode)

Port Name	I/O mode	Pull-up / Pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up / pull-down resistor	I/O port
Port 1	Input mode	No pull-up / pull-down resistor	I/O port
Port 2	Input mode	P27 : Pull-up resistor Others : No pull-up resistor	I/O port
Port 3	Input mode	No pull-up resistor	I/O port
Port 4	Input mode	No pull-up resistor	I/O port
Port 5	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up resistor	I/O port
Port 7	Input mode	No pull-up resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port 9	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up / pull-down resistor	I/O port
Port	Input mode	No pull-up resistor	I/O port

The values of pull-up/pull-down resistors should be caluculated in following ways based on the electrical characteristics in LSI User's Manual of each model.

How to determine pull-up resistor value

ex) When pins maintain the low level guaranteed performance as specified in the electrical characteristics (V_{IN} is not 0 V),
and at V_{DD} = 5 V, V_{IN} = 1.5 V,
input current is min. = - 30 μA, typ = - 100 μA, max. = - 300 μA.
(- means current passing from microcontroller.)
When convert above values to resistor value, typ = 35 kΩ.
Note that this value varies wildely depending on the temperature.
In temperature variation from - 40 °C to 85 °C, the resistor value varies from min. = 11.7 kΩ to max. = 117 kΩ.

How to determine pull-down resistor value

ex) When pins maintain the high level guaranteed performance as specified in the electrical characteristics (V_{IN} is not V_{DD}),
and at V_{DD} = 5 V, V_{IN} = 3.5 V,
input current is min. = - 30 μA, typ = - 100 μA, max. = - 300 μA.
When convert these values to resistance value, typ = 35 kΩ.
Note that this value varies wildely depending on the temperature.
In temperature variation from - 40 °C to 85 °C, the resistor value varies from min. = 11.7 kΩ to max. = 117 kΩ.

4-1-3 Control Registers

Ports 0 to 9, port A and B are controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU) or the pull-up / pull-down resistor control resister (PnPLUD) and registers that control special function pin (P0IMD, P1OMD, P4SYO, P4MMD, P5OMD, P5LED, PAIMD, PBIMD, FLOAT, LCCTR1, LCCTR2, LCCTR3, LCCTR4).

Table 4-1-2 shows the registers to control ports 0 to 9, and port A and B ;

Table 4-1-2 I/O Port Control Registers List (1/2)

	Register	Address	R/W	Function	Page
Port 0	P0OUT	x'03F10'	R/W	Port 0 output register	Ⅳ-7
	P0IN	x'03F20'	R	Port 0 input register	Ⅳ-7
	P0DIR	x'03F30'	R/W	Port 0 direction control register	Ⅳ-7
	P0PLUD	x'03F40'	R/W	Port 0 pull-up / pull-down resistor control register	Ⅳ-7
	P0IMD	x'03F4D'	R/W	Port 0 key interrupt control register	Ⅲ-49
Port 1	P1OUT	x'03F11'	R/W	Port 1 output register	Ⅳ-14
	P1IN	x'03F21'	R	Port 1 input register	Ⅳ-14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	Ⅳ-14
	P1PLUD	x'03F41'	R/W	Port 1 pull-up / pull-down resistor control register	Ⅳ-14
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	Ⅳ-15
Port 2	P2OUT	x'03F12'	R/W	Port 2 output register	Ⅳ-19
	P2IN	x'03F22'	R	Port 2 input register	Ⅳ-19
	P2PLU	x'03F42'	R/W	Port 2 pull-up resistor control register	Ⅳ-19
Port 3	P3OUT	x'03F13'	R/W	Port 3 output register	Ⅳ-22
	P3IN	x'03F23'	R	Port 3 input register	Ⅳ-22
	P3DIR	x'03F33'	R/W	Port 3 direction control register	Ⅳ-22
	P3PLU	x'03F43'	R/W	Port 3 pull-up resistor control register	Ⅳ-22
Port 4	P4OUT	x'03F14'	R/W	Port 4 output register	Ⅳ-30
	P4IN	x'03F24'	R	Port 4 input register	Ⅳ-30
	P4DIR	x'03F34'	R/W	Port 4 direction control register	Ⅳ-30
	P4PLU	x'03F44'	R/W	Port 4 pull-up resistor control register	Ⅳ-30
	P4SYO	x'03F1E'	R/W	Port 4 synchronous output control register	Ⅳ-31
	P4IMD	x'03F3E'	R/W	Port 4 key input interrupt control register	Ⅲ-50

Table 4-1-3 I/O Port Control Registers List (2/2)

	Register	Address	R/W	Function	Page
Port 5	P5OUT	x'03F15'	R/W	Port 5 output register	Ⅳ-35
	P5IN	x'03F25'	R	Port 5 input register	Ⅳ-35
	P5DIR	x'03F35'	R/W	Port 5 direction control register	Ⅳ-35
	P5PLU	x'03F45'	R/W	Port 5 pull-up resistor control register	Ⅳ-35
	P5OMD	x'03F3F'	R/W	Port 5 output mode register	Ⅳ-36
	P5LED	x'03F4F'	R/W	Port 5 large current drive control register	Ⅳ-37
Port 6	P6OUT	x'03F16'	R/W	Port 6 output register	Ⅳ-41
	P6IN	x'03F26'	R	Port 6 input register	Ⅳ-41
	P6DIR	x'03F36'	R/W	Port 6 direction control register	Ⅳ-41
	P6PLU	x'03F46'	R/W	Port 6 pull-up resistor control register	Ⅳ-41
Port 7	P7OUT	x'03F17'	R/W	Port 7 output register	Ⅳ-45
	P7IN	x'03F27'	R	Port 7 input register	Ⅳ-45
	P7DIR	x'03F37'	R/W	Port 7 direction control register	Ⅳ-45
	P7PLU	x'03F47'	R/W	Port 7 pull-up resistor control register	Ⅳ-45
Port 8	P8OUT	x'03F18'	R/W	Port 8 output register	Ⅳ-50
	P8IN	x'03F28'	R	Port 8 input register	Ⅳ-50
	P8DIR	x'03F38'	R/W	Port 8 direction control register	Ⅳ-50
	P8PLU	x'03F48'	R/W	Port 8 pull-up resistor control register	Ⅳ-50
Port 9	P9OUT	x'03F19'	R/W	Port 9 output register	Ⅳ-54
	P9IN	x'03F29'	R	Port 9 input register	Ⅳ-54
	P9DIR	x'03F39'	R/W	Port 9 direction control register	Ⅳ-54
	P9PLU	x'03F49'	R/W	Port 9 pull-up resistor control register	Ⅳ-54
Port A	PAOUT	x'03F1A'	R/W	Port A output register	Ⅳ-58
	PAIN	x'03F2A'	R	Port A input register	Ⅳ-58
	PADIR	x'03F3A'	R/W	Port A direction control register	Ⅳ-58
	PAIMD	x'03F3C'	R/W	Port A input mode register	Ⅳ-58
	PAPLUD	x'03F4A'	R/W	Port A pull-up / pull-down resistor control register	Ⅳ-58
Port B	PBOUT	x'03F1B'	R/W	Port B output register	Ⅳ-62
	PBIN	x'03F2B'	R	Port B input register	Ⅳ-62
	PBDIR	x'03F3B'	R/W	Port B direction control register	Ⅳ-62
	PBIMD	x'03F3D'	R/W	Port B input mode register	Ⅳ-62
	PBPLU	x'03F4B'	R/W	Port B pull-up resistor control register	Ⅳ-62
Pin control	FLOAT	x'03F2E'	R/W	Pull-up / Pull-down resistor selection, pin control register	Ⅳ-8,16,31,59, Ⅺ-8
LCD control	LCCTR1	x'03FDB'	R/W	LCD output control register 1	Ⅳ-23,51,55 XIV-9
	LCCTR2	x'03FDC'	R/W	LCD output control register 2	Ⅳ-42, 46, XIV-10
	LCCTR3	x'03FDD'	R/W	LCD output control register 3	Ⅳ-24,32, XIV-11
	LCCTR4	x'03FDE'	R/W	LCD output control register 4	Ⅳ-63 XIV-12
Serial control	SC0MD1	x'03F91'	R/W	Serial interface 0 mode register	Ⅺ-7
	SC2MD1	x'03FA1'	R/W	Serial interface 2 mode register	Ⅻ-7
Buzzer control	DLYCTR	x'03F03'	R/W	Oscillation stabilization wait counter control register	Ⅱ-33 X-3

R/W : Readable/Writable

R : Readable only

4-2 Port 0

4-2-1 Description

■General Port Setup
Each bit can be set individually as either an input or output by the port 0 control I/O direction register (P0DIR). The control flag of the port 0 direction control register (P0DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 0 direction control register (P0DIR) to "0" and read the value of the port 0 input register (P0IN).

To output data to pin, set the control flag of the port 0 direction control register (P0DIR) to "1" and write the data to the port 0 output register (P0OUT).

Each bit can be set individually if pull-up or pull-down resistor is added or not, by the port 0 pull-up / pull-down resistor control register (P0PLUD). Set the control flag of the port 0 pull-up / pull-down resistor control register (P0PLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) selects if pull-up resistor or pull-down resistor is added. The bp4 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

■Special Function Pin Setup
P00 to P05 are used as input pin of key interrupt, as well.

[☞ Chapter 3 3-3-6. Key input interrupt]

[☞ Chapter 3 3-3-3. Control registers]

P00 to P05 are used as I/O pin for serial 0, 2, as well. P00 and P03 are output pins of the serial 0, 2 transmission data. When the SC0SBOS, SC2SBOS flag of the serial interface 0, 2 mode register 1 (SC0MD1, SC2MD1) is "1", P00 and P03 are serial data output pins. P01 and P04 are the input pins of the serial 0, 2 reception data. P02 and P05 are I/O pins of the serial 0, 2 clock. When the SC0SBTS, SC2SBTS flag of serial interface 0, 2 mode register 1 (SC0MD1, SC2MD1) is "1", P02 and P05 are serial clock output pins.
P00, P01, P02 and P05 can be selected as either an push-pull output or Nch open-drain output by the serial interface 0, 2 port control registers (SC0ODC, SC2ODC).
I/O pins of serial interface 0 can be assigned to be any pins among P00 to P02, or PB05 to PB07 by the SC0SEL flag of the pin control register (FLOAT).

[☞ Chapter 11 11-2. Control registers]

[☞ Chapter 12 12-2. Control registers]

P06 is used as a buzzer output pin, as well. When the bp7 of the oscillation stabilization control register (DLYCTR) is "1", buzzer output is enabled.

4-2-2 Registers

	7	6	5	4	3	2	1	0	
P0OUT	—	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0	(At reset : - X X X X X X X)

P0OUT	Output data
0	L(V_{SS} level) is output.
1	H(V_{DD} level) is output.

Port 0 output register (P0OUT : x'03F10', R/W)

	7	6	5	4	3	2	1	0	
P0IN	—	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0	(At reset : - X X X X X X X)

P0IN	Input data
0	Pin is low(V_{SS} level).
1	Pin is high(V_{DD} level).

Port 0 input register (P0IN : x'03F20', R)

	7	6	5	4	3	2	1	0	
P0DIR	—	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0	(At reset : - 0 0 0 0 0 0 0)

P0DIR	I/O mode selection
0	Input mode
1	Output mode

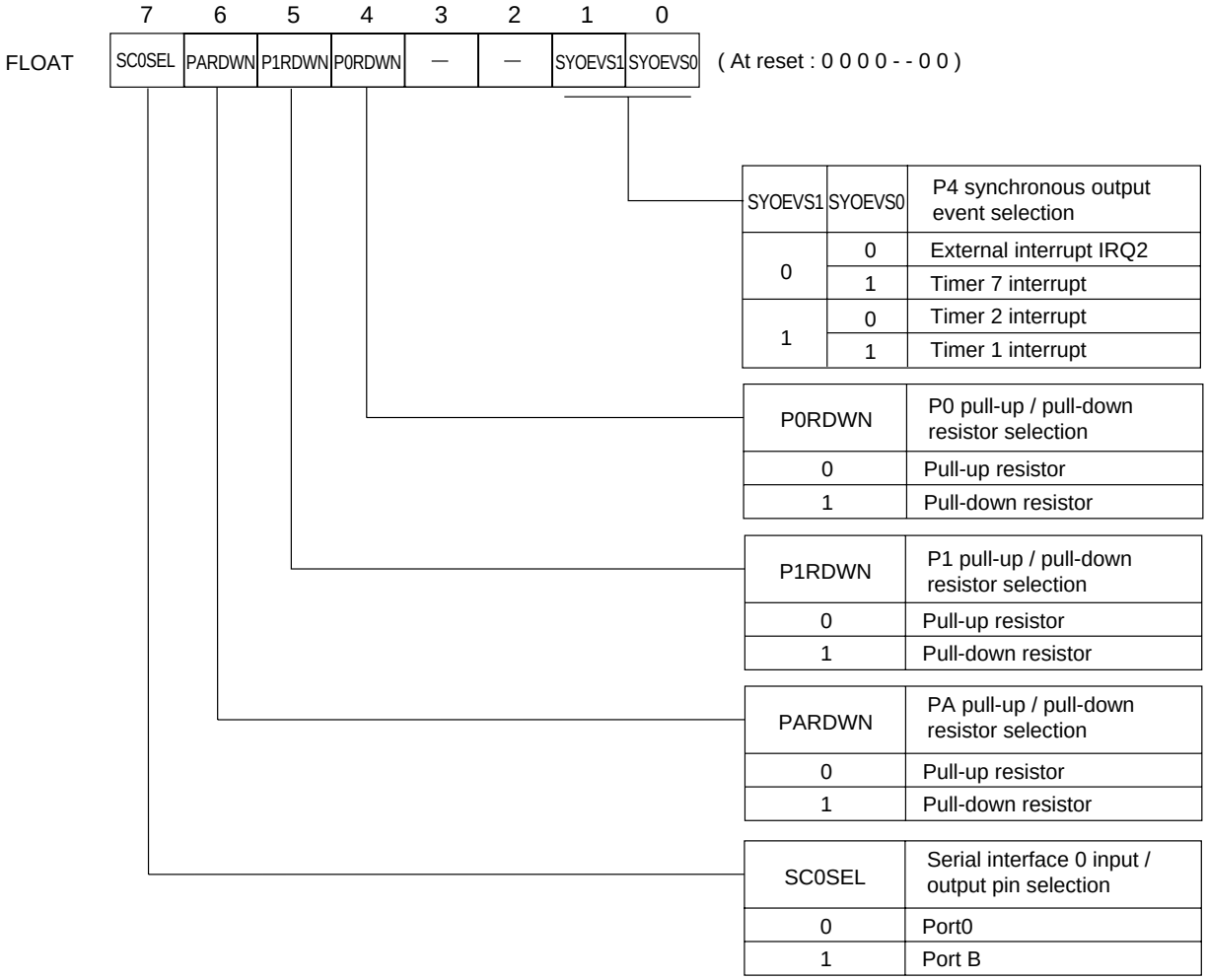
Port 0 direction control register (P0DIR : x'03F30', R/W)

	7	6	5	4	3	2	1	0	
P0PLUD	—	P0PLUD6	P0PLUD5	P0PLUD4	P0PLUD3	P0PLUD2	P0PLUD1	P0PLUD0	(At reset : - 0 0 0 0 0 0 0)

P0PLU	Pull-up / pull-down resistor selection
0	No pull-up / pull-down resistor
1	Pull-up / pull-down resistor

Port 0 pull-up / pull-down resistor control register (P0PLU : x'03F40', R/W)

Figure 4-2-1 Port 0 Registers (1/2)


7 6 5 4 3 2 1 0
FLOAT
SC0SEL PARDWN P1RDWN P0RDWN — — SYOEVS1 SYOEVS0
(At reset : 0 0 0 0 - - 0 0)
SYOEVS1 SYOEVS0 P4 synchronous output event selection
0 0 External interrupt IRQ2
1 Timer 7 interrupt
1 0 Timer 2 interrupt
1 Timer 1 interrupt
P0RDWN P0 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
P1RDWN P1 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
PARDWN PA pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
SC0SEL Serial interface 0 input / output pin selection
0 Port0
1 Port B

Pull-up / Pull-down resistor selection, Pin control register (FLOAT : x'03F2E', R/W)

Figure 4-2-2 Port 0 Registers (2/2)

4-2-3 Block Diagram

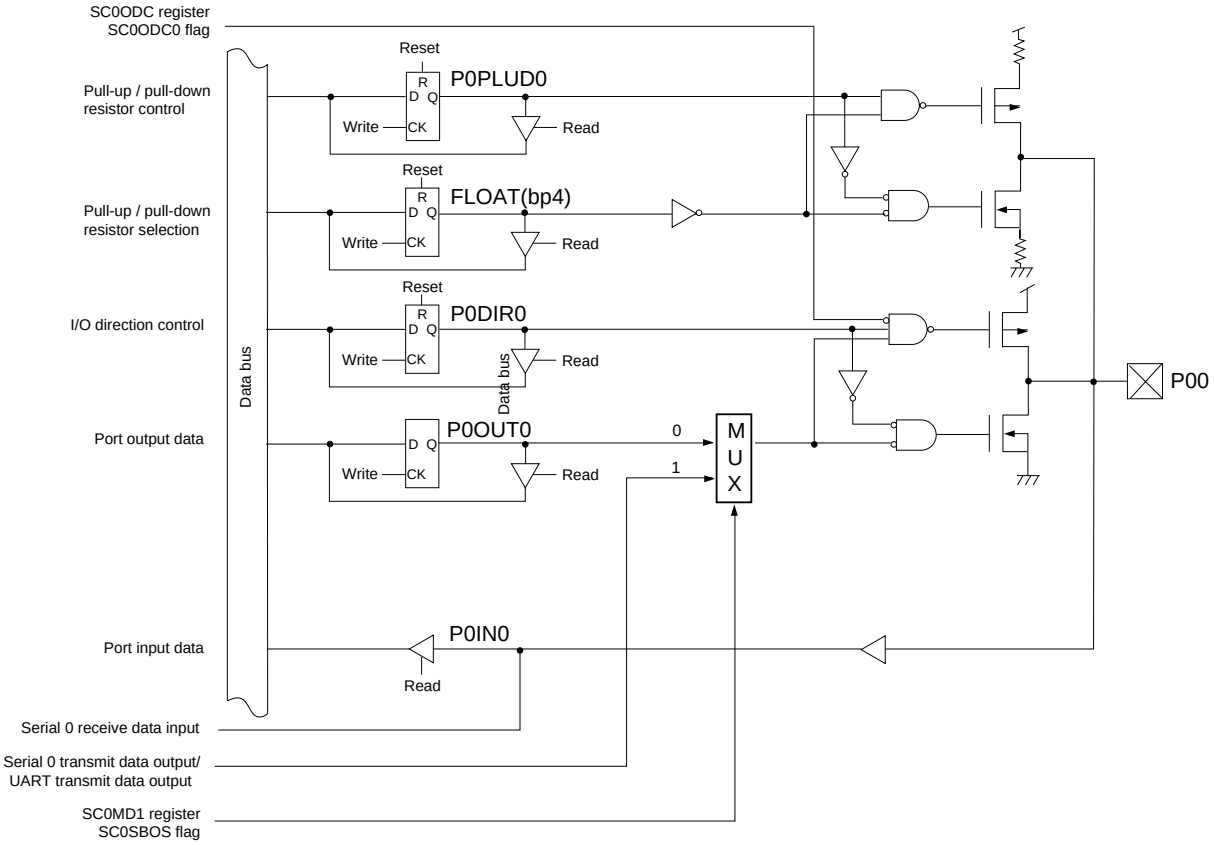


Figure 4-2-3 Block diagram (P00)

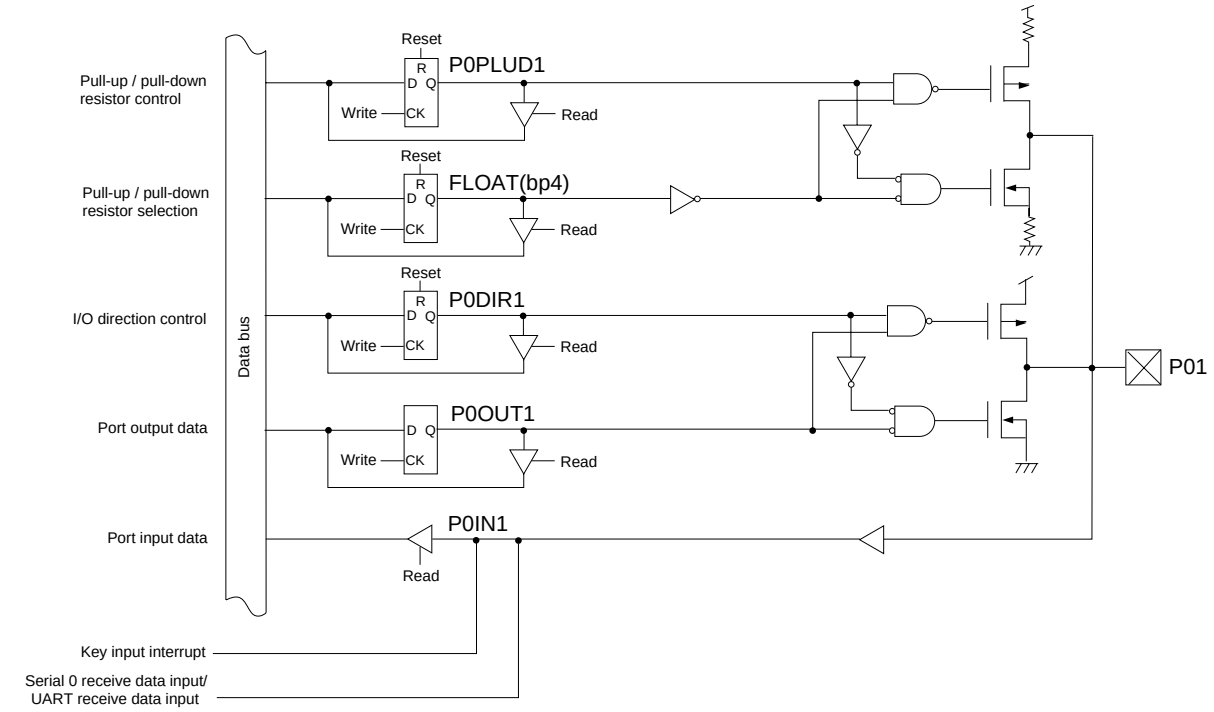


Figure 4-2-4 Block diagram (P01)

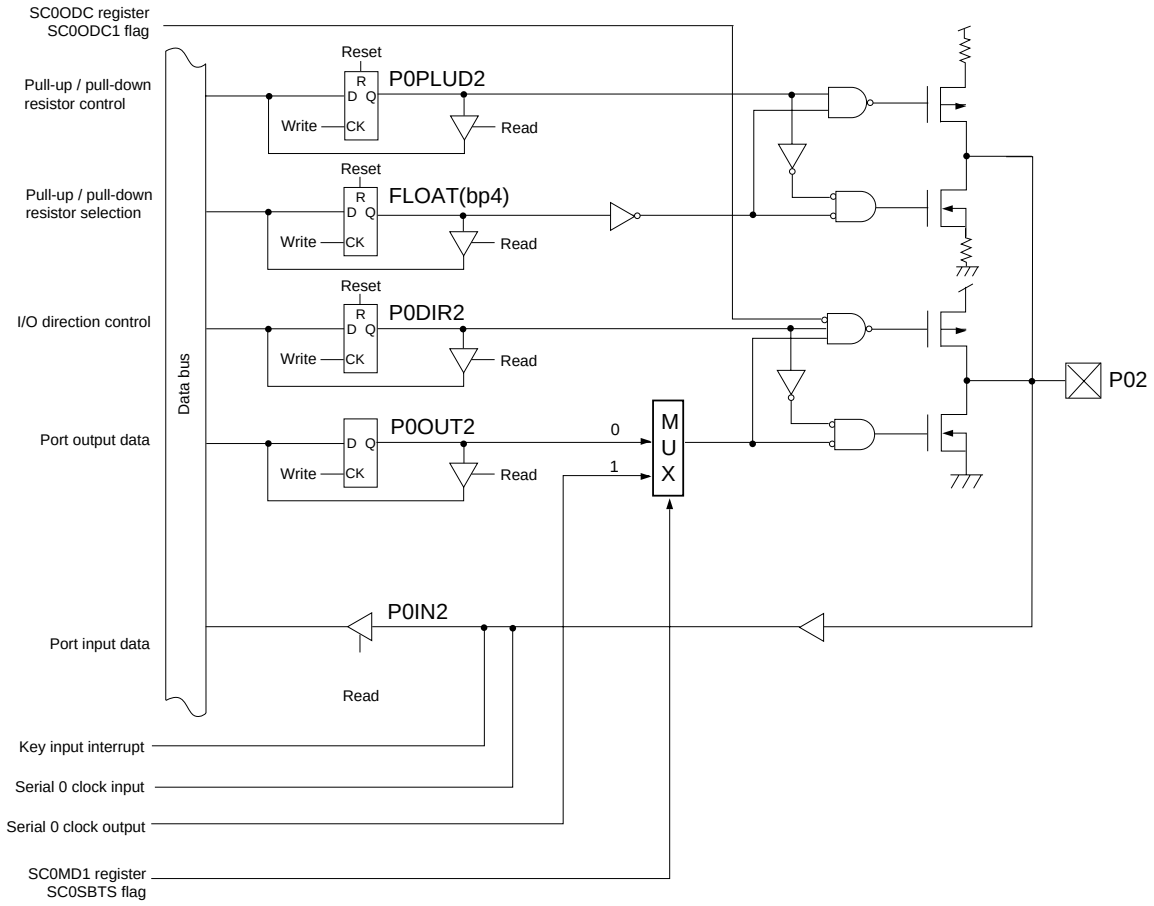


Figure 4-2-5 Block diagram (P02)

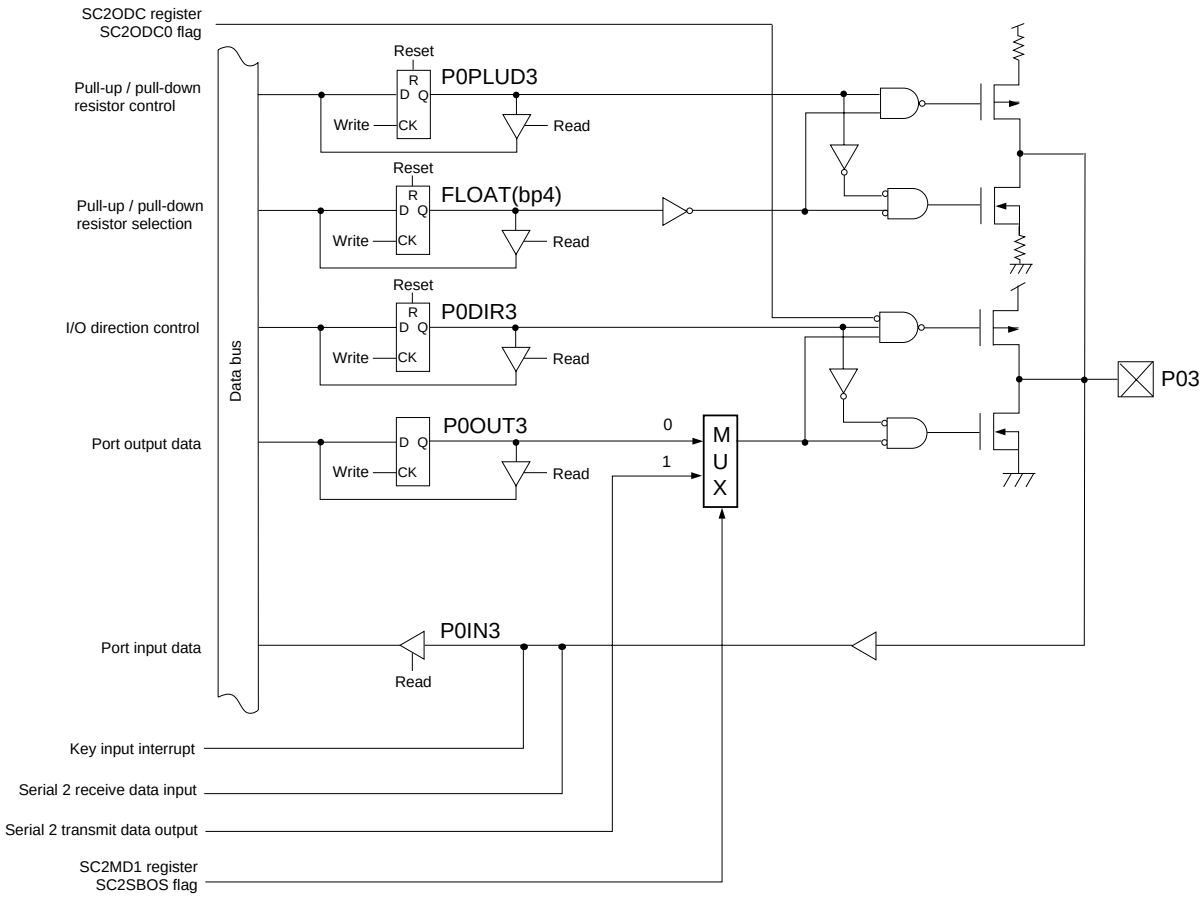


Figure 4-2-6 Block diagram (P03)

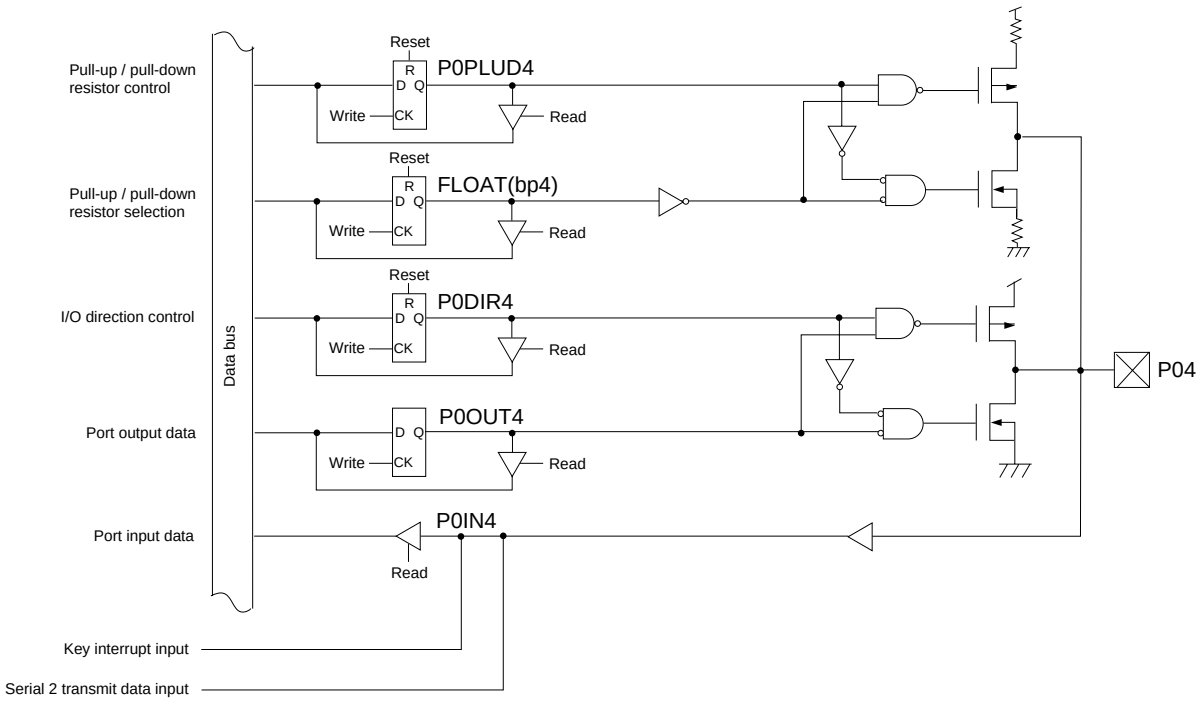


Figure 4-2-7 Block Diagram (P04)

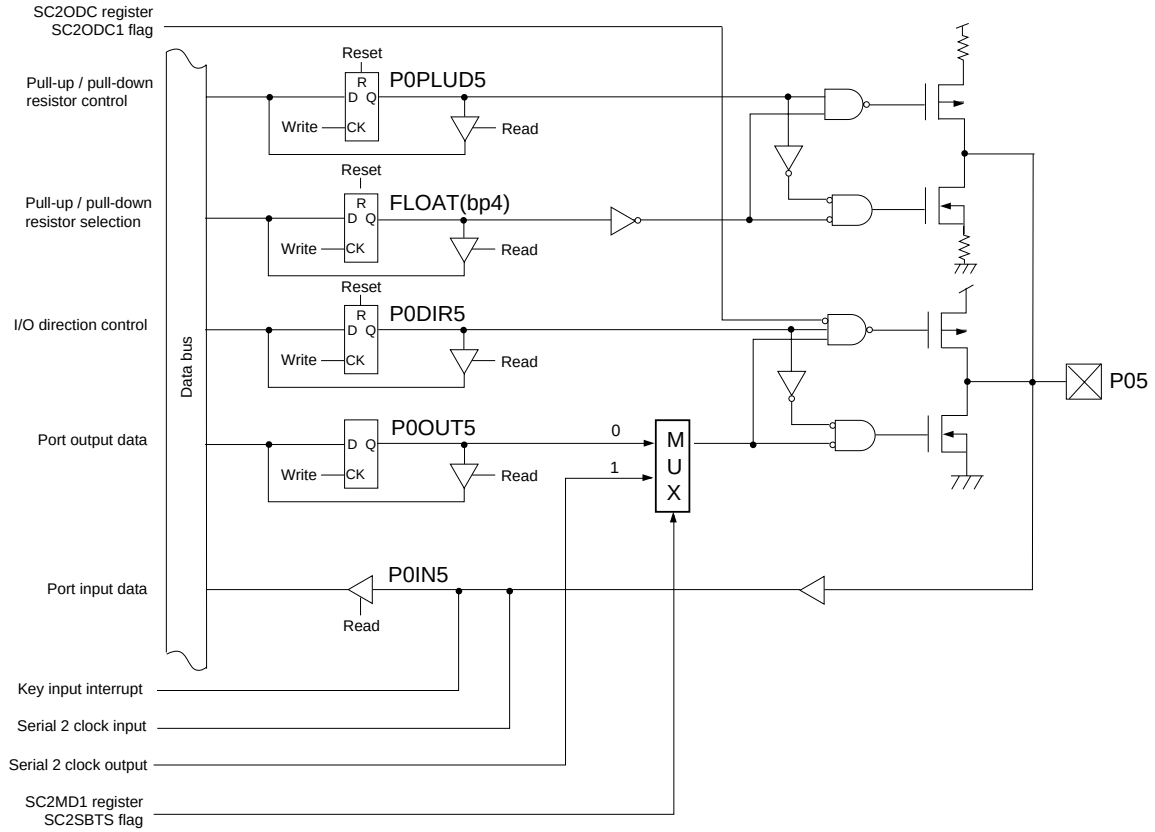


Figure 4-2-8 Block Diagram (P05)

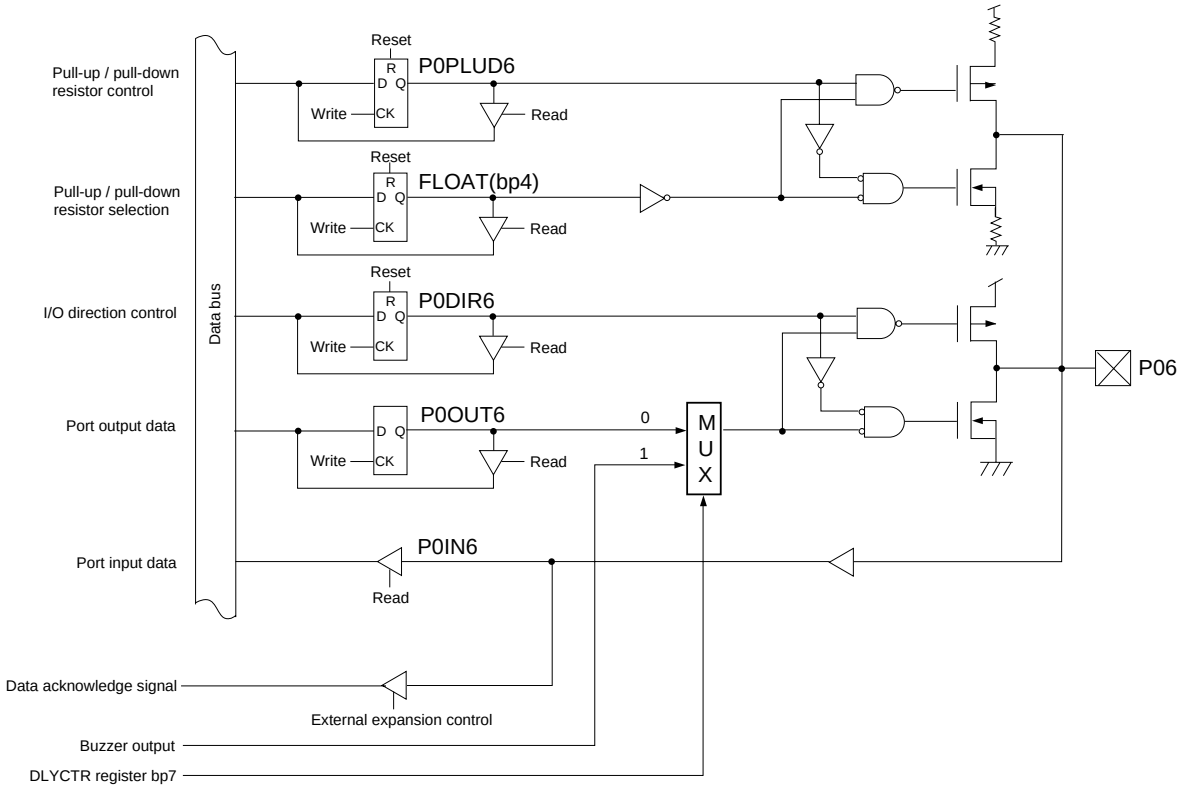


Figure 4-2-9 Block Diagram (P06)

4-3 Port 1

4-3-1 Description

■General Port Setup
Each bit can be set individually as either an input or output by the port 1 I/O direction control register (P1DIR). The control flag of the port 1 direction control register (P1DIR) is set to "1" for output mode, and "0" for input mode.

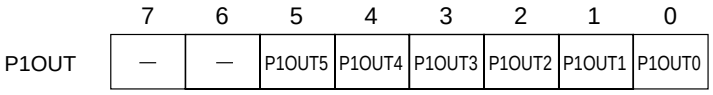
To read input data of pin, set the control flag of the port 1 direction control register (P1DIR) to "0" and read the value of the port 1 input register (P1IN).

To output data to pin, set the control flag of the port 1 direction control register (P1DIR) to "1" and write the value of the port 1 output register (P1OUT).

Each bit can be set individually if pull-up or pull-down resistor is added or not, by the port 1 pull-up / pull-down resistor control register (P1PLUD). Set the control flag of the port 1 pull-up / pull-down resistor control register (P1PLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp5 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

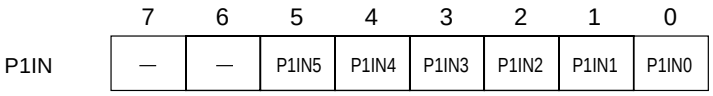
■Special Function Pin Setup
P10 to P15 are used as timer I/O pin, as well. P10 is used as remote control carrier output pin, as well. The port 1 output mode register (P1OMD) can select P10 to P15 output mode by each bit. When the port 1 output mode register (P1OMD) is "1", special function data is output, and when it is "0", they are used as general port.

4-3-2 Registers



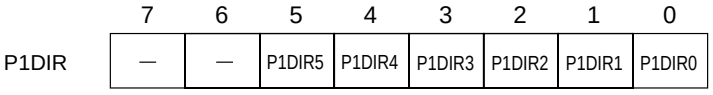
P1OUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port 1 output register (P1OUT : x'03F11', R/W)



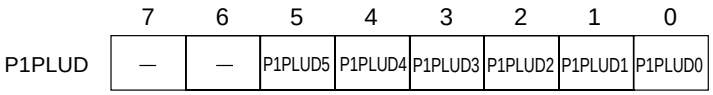
P1IN	Input data
0	Pin is low(VSS level).
1	Pin is high(VDD level).

Port 1 input register (P1IN : x'03F21', R)



P1DIR	I/O mode selection
0	Input mode
1	Output mode

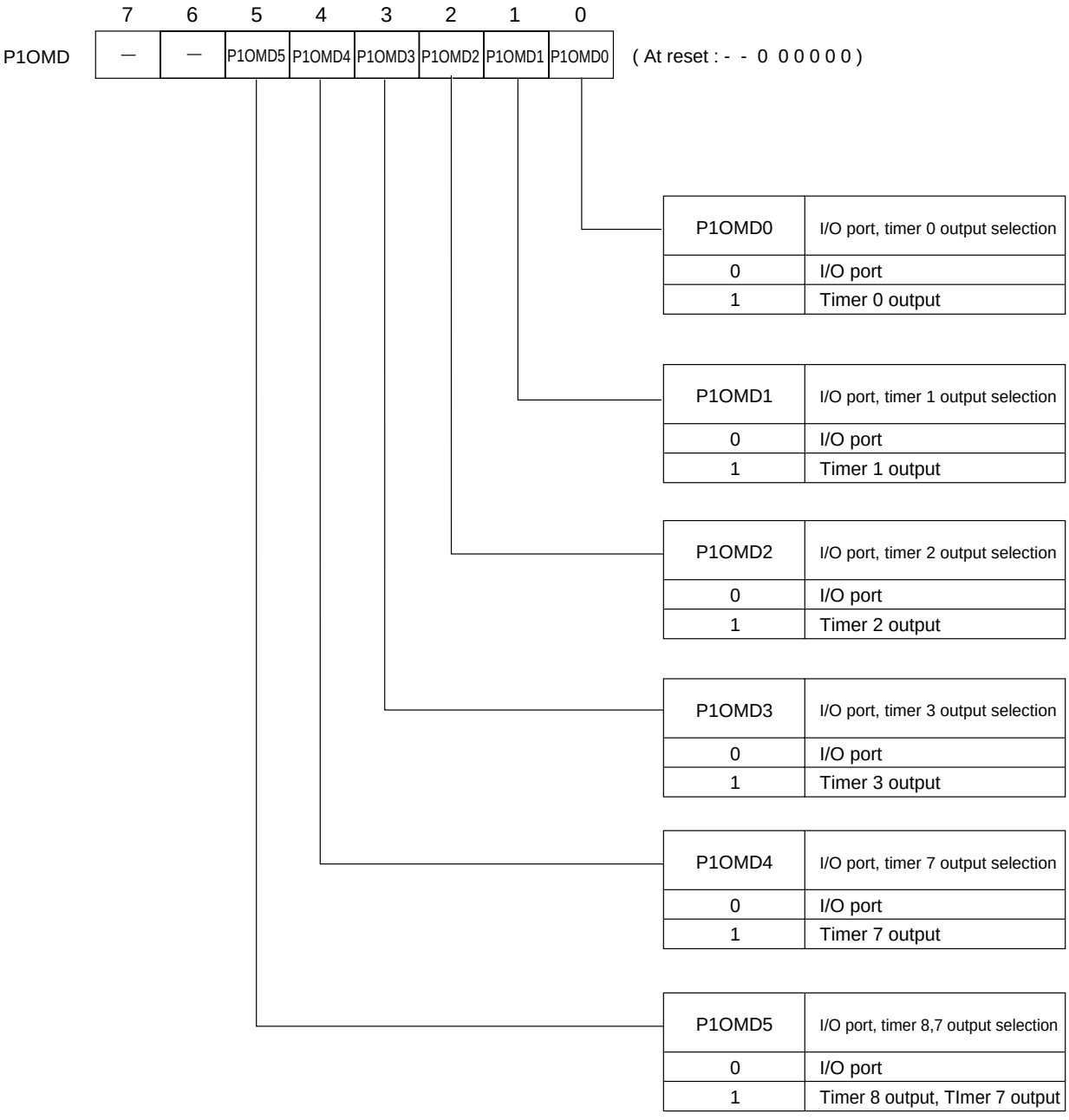
Port 1 direction control register (P1DIR : x'03F31', R/W)



P1PLUD	Pull-up / pull-down resistor selection
0	No pull-up / pull-down resistor
1	Pull-up / pull-down resistor

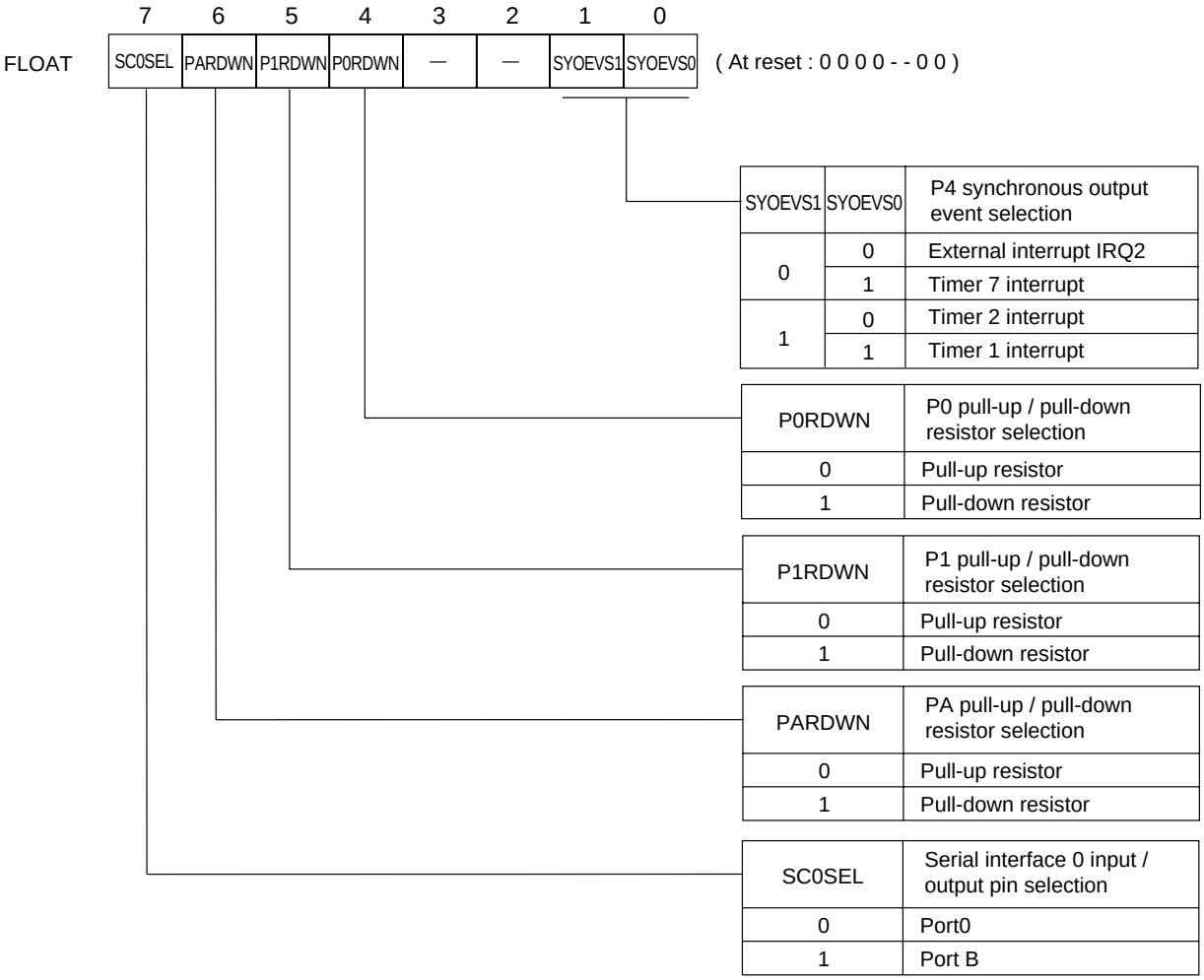
Port 1 pull-up / pull-down resistor control register (P1PLUD : x'03F41', R/W)

Figure 4-3-1 Port 1 Registers (1/3)


7 6 5 4 3 2 1 0
P1OMD
—
—
P1OMD5
P1OMD4
P1OMD3
P1OMD2
P1OMD1
P1OMD0
(At reset : - - 0 0 0 0 0 0)
P1OMD0 I/O port, timer 0 output selection
0 I/O port
1 Timer 0 output
P1OMD1 I/O port, timer 1 output selection
0 I/O port
1 Timer 1 output
P1OMD2 I/O port, timer 2 output selection
0 I/O port
1 Timer 2 output
P1OMD3 I/O port, timer 3 output selection
0 I/O port
1 Timer 3 output
P1OMD4 I/O port, timer 7 output selection
0 I/O port
1 Timer 7 output
P1OMD5 I/O port, timer 8,7 output selection
0 I/O port
1 Timer 8 output, TImer 7 output

Port 1 output mode register (P1OMD : x'03F2F', R/W)

Figure 4-3-2 Port 1 Registers (2/3)


7 6 5 4 3 2 1 0
FLOAT
SC0SEL PARDWN P1RDWN P0RDWN — — SYOEVS1 SYOEVS0
(At reset : 0 0 0 0 - - 0 0)
SYOEVS1 SYOEVS0 P4 synchronous output event selection
0 0 External interrupt IRQ2
1 Timer 7 interrupt
1 0 Timer 2 interrupt
1 Timer 1 interrupt
P0RDWN P0 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
P1RDWN P1 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
PARDWN PA pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
SC0SEL Serial interface 0 input / output pin selection
0 Port0
1 Port B

Pull-up / Pull-down resistor selection, Pin control register (FLOAT : x'03F2E', R/W)

Figure 4-3-3 Port 1 Registers (3/3)

4-3-3 Block Diagram

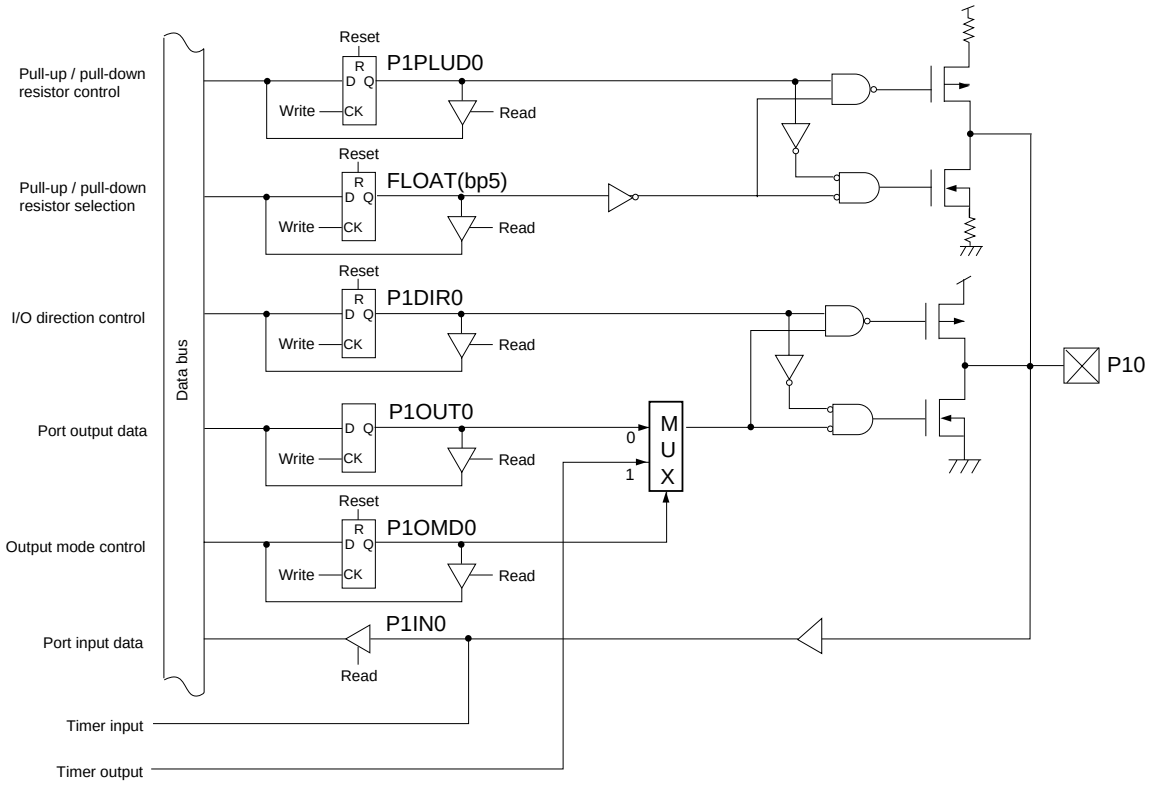


Figure 4-3-4 Block Diagram (P10)

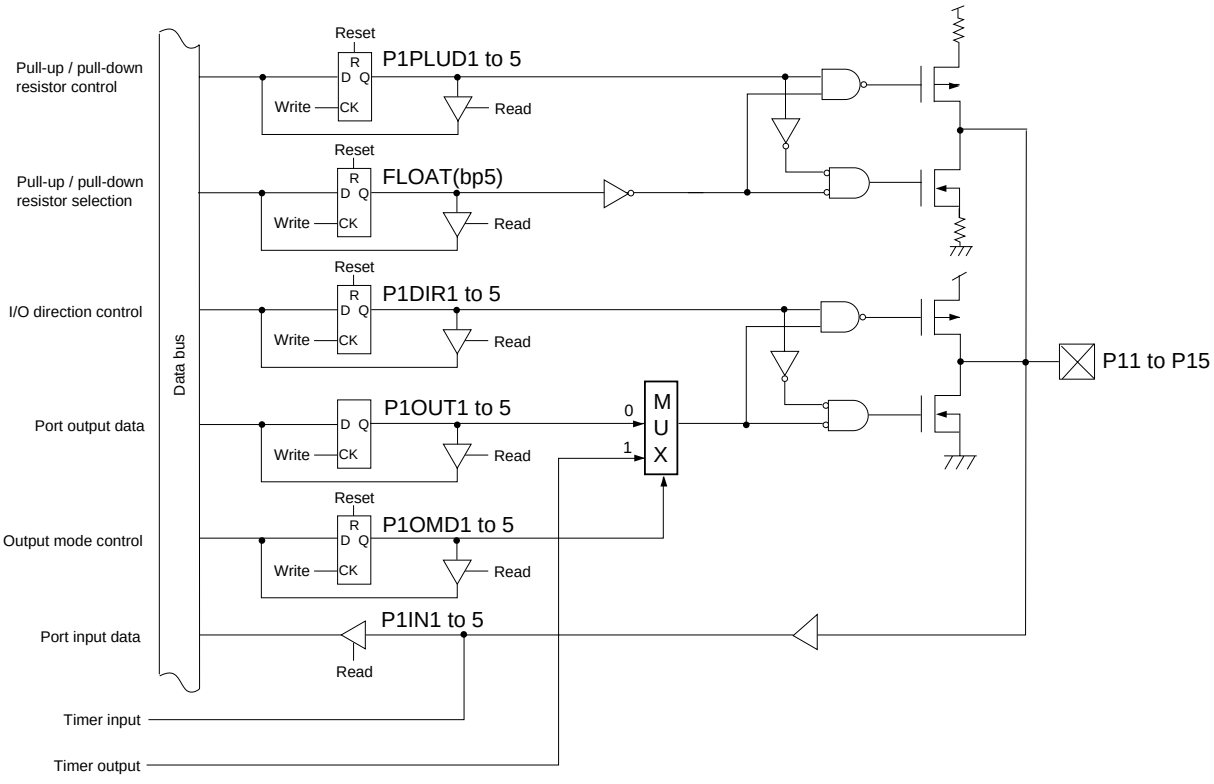


Figure 4-3-5 Block Diagram (P11 to P15)

4-4 Port 2

4-4-1 Description

■General Port Setup
Port 2 is input port, except P27. To read input data of pin, read out the value of the port 2 input register (P2IN).

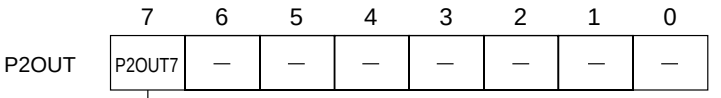
P27 is reset pin. When the software is reset, write "0" to the bp7 of the port 2 output register (P2OUT).

The port 2 pull-up resistor control register (P2PLU) can select if port 2 is added pull-up resistor or not, by 1 bit. When the control flag of the port 2 pull-up resistor control register (P2PLU) is set to "1", pull-up resistor is added. P27 is always added pull-up resistor.

■Special Function Pin Setup
P20, P22, P23 and P24 are used as external interrupt pins, and P25 is used as remote control pin, as well.

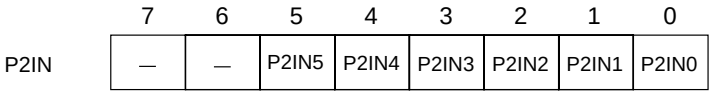
P21 is used as an input pin for external interrupt and AC zero-cross. To read data of AC zero-cross, set "1" to the bp7 of the noise filter control register (NFCTR) and read the value of the port 2 input register (P2IN).

4-4-2 Registers



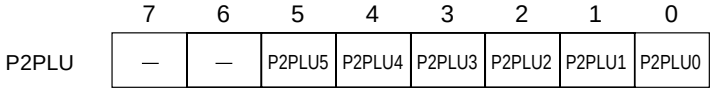
P2OUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port 2 output register(P2OUT : x'03F12', R/W)



P2IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 2 input register(P2IN : x'03F22', R)



P2PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 2 pull-up resistor control register(P2PLU : x'03F42', R/W)

Figure 4-4-1 Port 2 Registers

4-4-3 Block Diagram

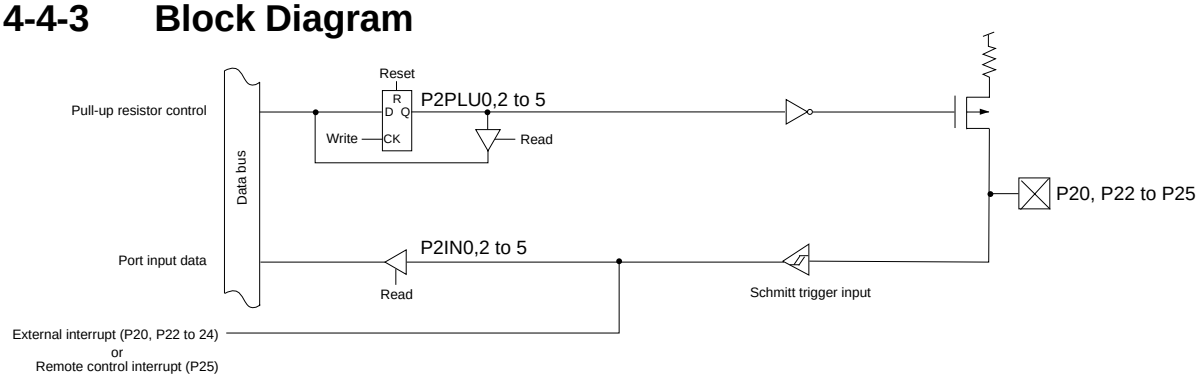


Figure 4-4-2 Block Diagram (P20, P22 to P25)

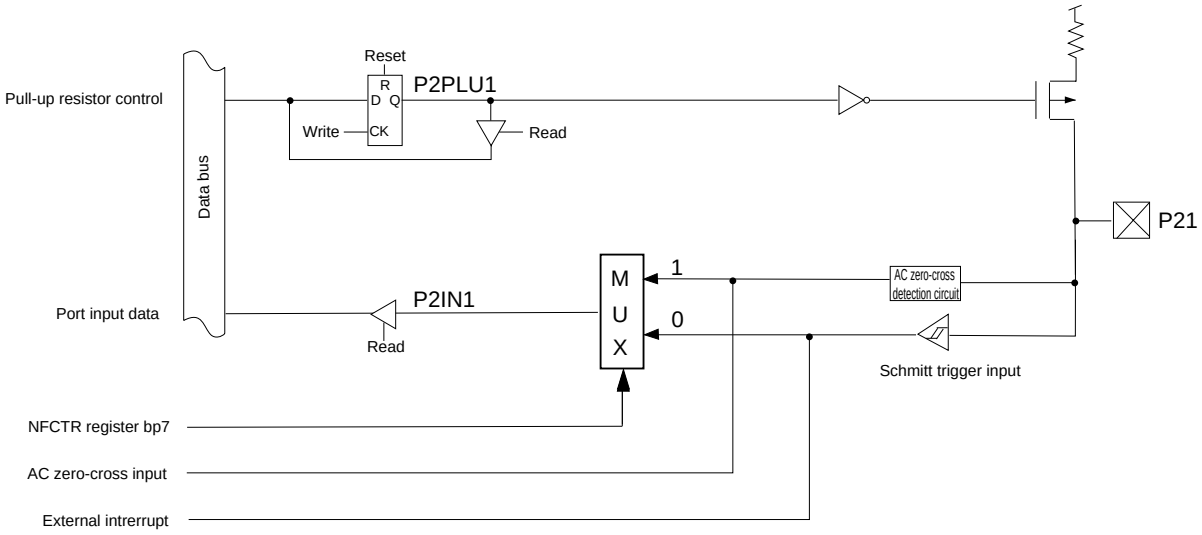


Figure 4-4-3 Block Diagram (P21)

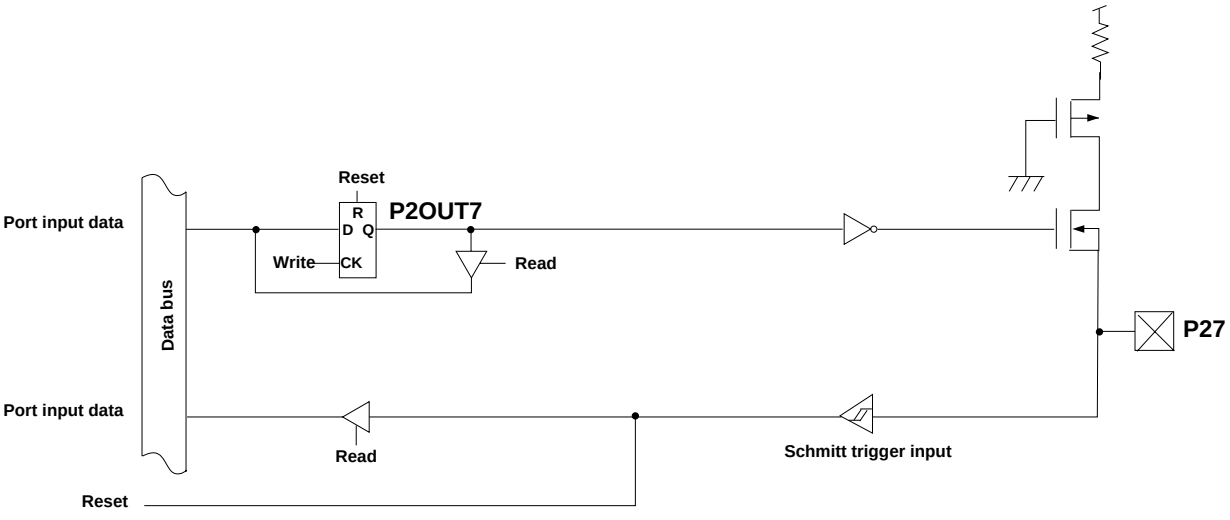


Figure 4-4-4 Block Diagram (P27)

4-5 Port 3

4-5-1 Description

■General Port Setup

Each bit can be set individually as either an input or output by the port 3 I/O direction control register (P3DIR). The control flag of the port 3 direction control register (P3DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 3 direction control register (P3DIR) to "0" and read the value of the port 3 input register (P3IN).

To output data to pin, set the control flag of the port 3 direction control register (P3DIR) to "1" and write data to the port 3 output register (P3OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 3 pull-up resistor control register (P3PLU). Set the control flag of the port 3 pull-up resistor control register (P3PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup

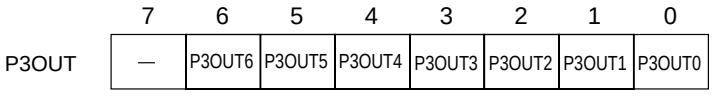
P30 to P37 can be used as the LCD Segment output pins (SEG38 to 34 and SEG9 to 8). Set "1" to bit 4 to 6 (LC3SL4 to 6) of the LCD output control register 3 (LCCTR3) to use SEG 38 to 34. Set "1" to bit 0 (LC1SL0) of the LCD output control register 1 (LCCTR1) to use SEG 9 to 8.
SEG 35 to 38 and SEG 9 to 8 can be set by 2-bits, and SEG 34 can be selected by 1-bit. When segment output is selected, input mode is set and the pull-up resistors are set off automatically.
In memory expansion mode P35 to 36 can be used as address output pins of the external expansion memory . Whether they are used as an address output pins or general I/O pins can be selected with bp7 of the address output control register (EXADV).

Table 4-5-1 P35 to P36 external expansion pins

Pin	In Memory expansion mode *
P35	A16 (external memory address bp16)
P36	A17 (external memory address bp17)

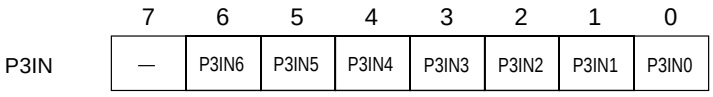
*P35 to 36 do not output address without setting bp7 of the EXADV register to "1".

4-5-2 Registers



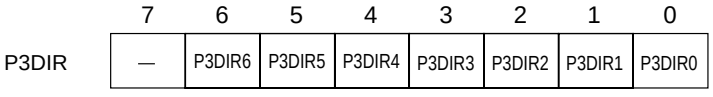
P3OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 3 output register (P3OUT : x'03F13', R/W)



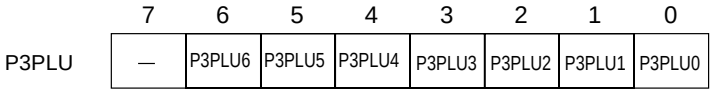
P3IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 3 input register (P3IN : x'03F23', R)



P3DIR	I/O mode selection
0	Input mode
1	Output mode

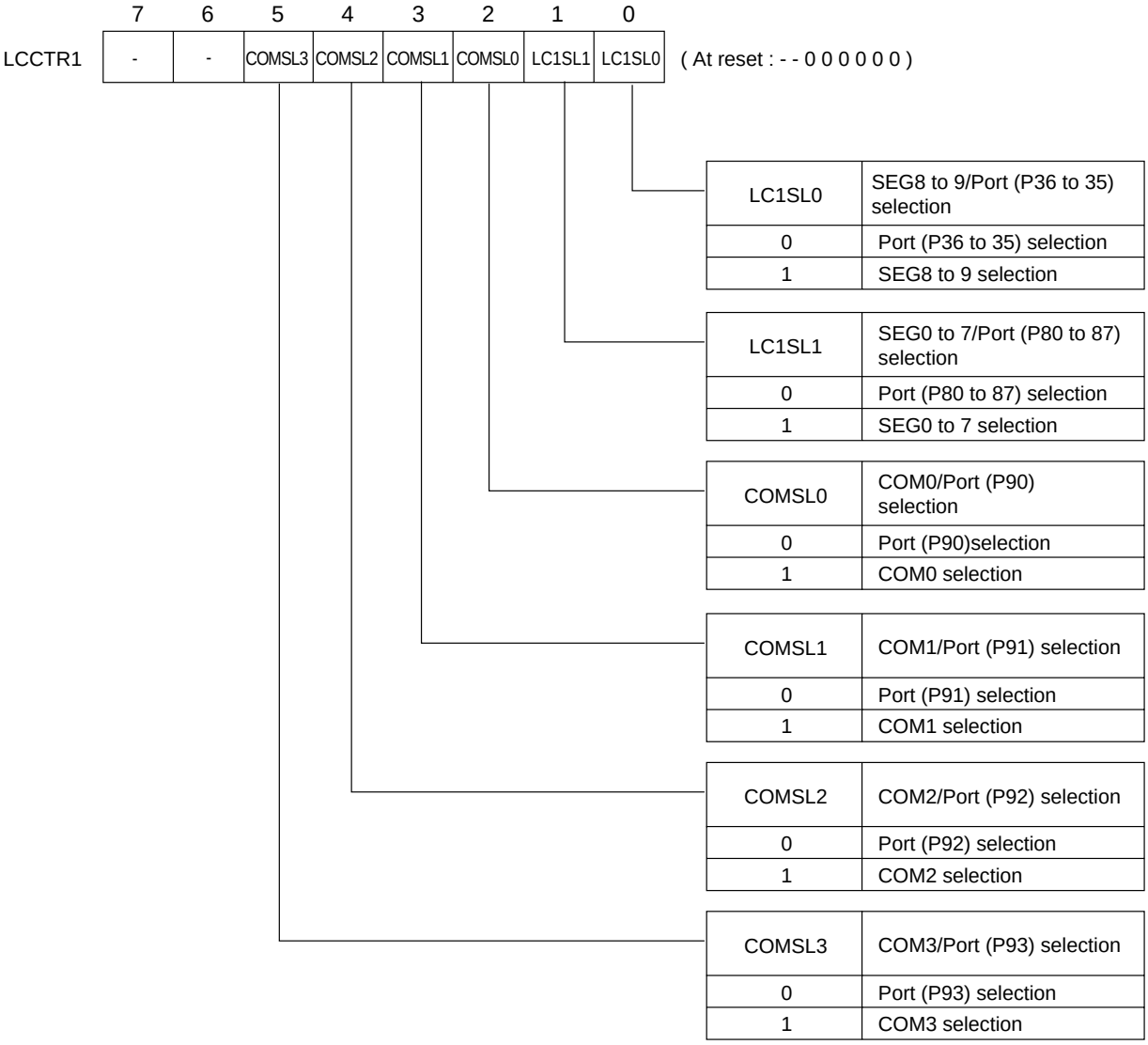
Port 3 direction control register (P3DIR : x'03F33', R/W)



P3PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

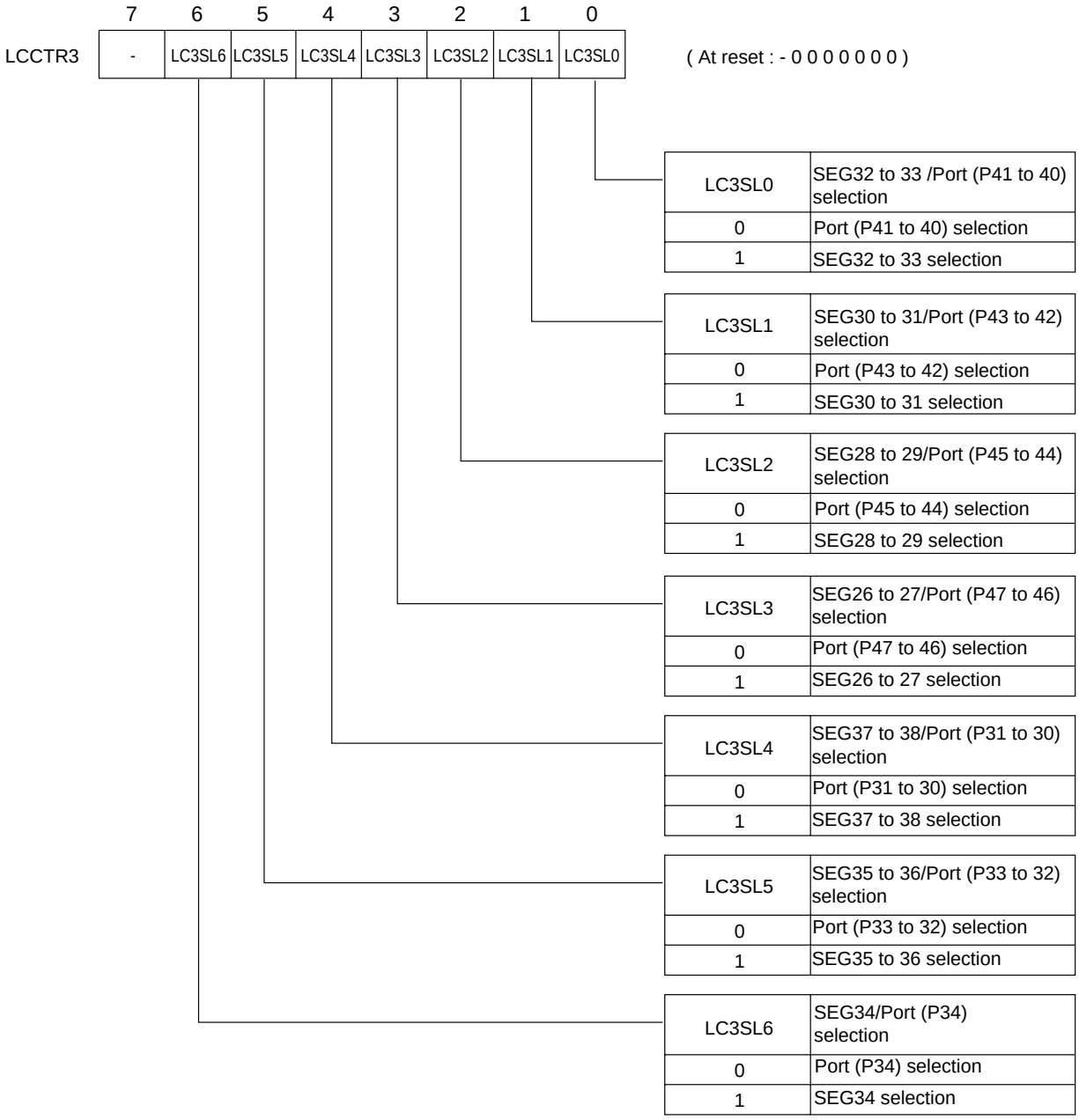
Port 3 pull-up resistor control register (P3PLU : x'03F43', R/W)

Figure 4-5-1 Port 3 Registers (1/3)


7 6 5 4 3 2 1 0
LCCTR1
- - COMSL3 COMSL2 COMSL1 COMSL0 LC1SL1 LC1SL0
(At reset : - - 0 0 0 0 0 0)
LC1SL0 | SEG8 to 9/Port (P36 to 35) selection
0 | Port (P36 to 35) selection
1 | SEG8 to 9 selection
LC1SL1 | SEG0 to 7/Port (P80 to 87) selection
0 | Port (P80 to 87) selection
1 | SEG0 to 7 selection
COMSL0 | COM0/Port (P90) selection
0 | Port (P90)selection
1 | COM0 selection
COMSL1 | COM1/Port (P91) selection
0 | Port (P91) selection
1 | COM1 selection
COMSL2 | COM2/Port (P92) selection
0 | Port (P92) selection
1 | COM2 selection
COMSL3 | COM3/Port (P93) selection
0 | Port (P93) selection
1 | COM3 selection

LCD Control Register1 (LCCTR1 : X'03FDB', R/W)

Figure 4-5-2 Port 3 Registers (2/3)


7 6 5 4 3 2 1 0
LCCTR3
- LC3SL6 LC3SL5 LC3SL4 LC3SL3 LC3SL2 LC3SL1 LC3SL0
(At reset : - 0 0 0 0 0 0 0)
LC3SL0 SEG32 to 33 /Port (P41 to 40) selection
0 Port (P41 to 40) selection
1 SEG32 to 33 selection
LC3SL1 SEG30 to 31/Port (P43 to 42) selection
0 Port (P43 to 42) selection
1 SEG30 to 31 selection
LC3SL2 SEG28 to 29/Port (P45 to 44) selection
0 Port (P45 to 44) selection
1 SEG28 to 29 selection
LC3SL3 SEG26 to 27/Port (P47 to 46) selection
0 Port (P47 to 46) selection
1 SEG26 to 27 selection
LC3SL4 SEG37 to 38/Port (P31 to 30) selection
0 Port (P31 to 30) selection
1 SEG37 to 38 selection
LC3SL5 SEG35 to 36/Port (P33 to 32) selection
0 Port (P33 to 32) selection
1 SEG35 to 36 selection
LC3SL6 SEG34/Port (P34) selection
0 Port (P34) selection
1 SEG34 selection

LCD Control Register 3 (LCCTR3 : X'03FDD', R/W)

Figure 4-5-3 Port 3 Registers (3/3)

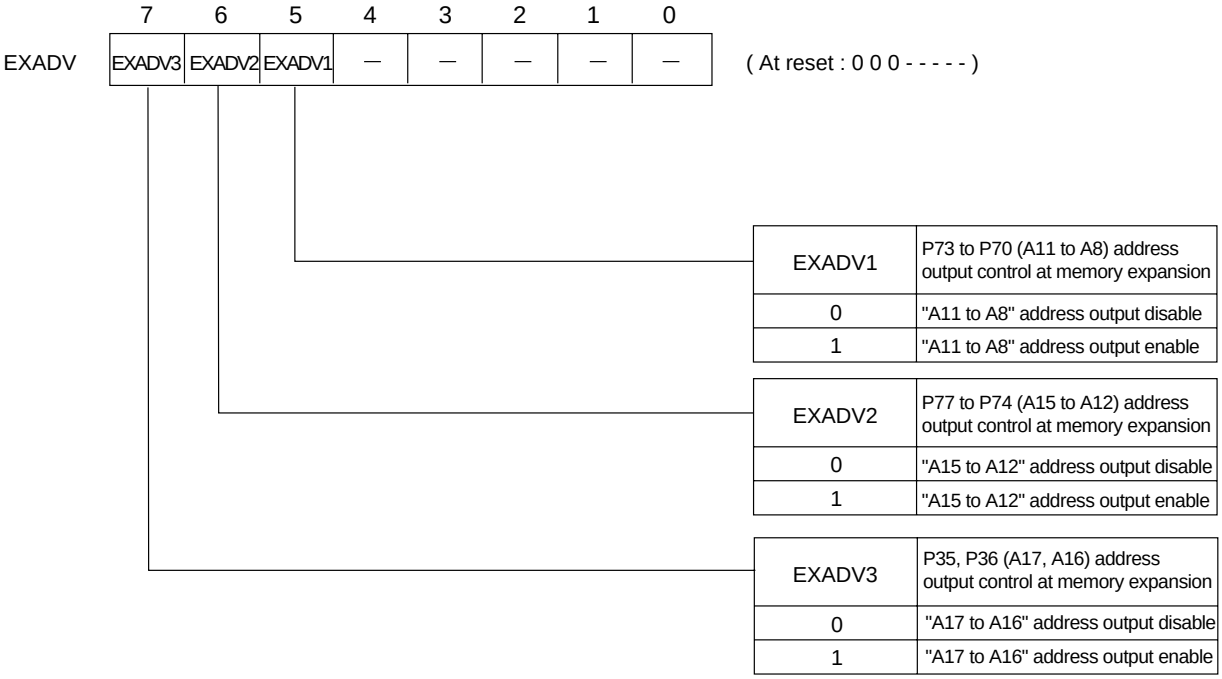
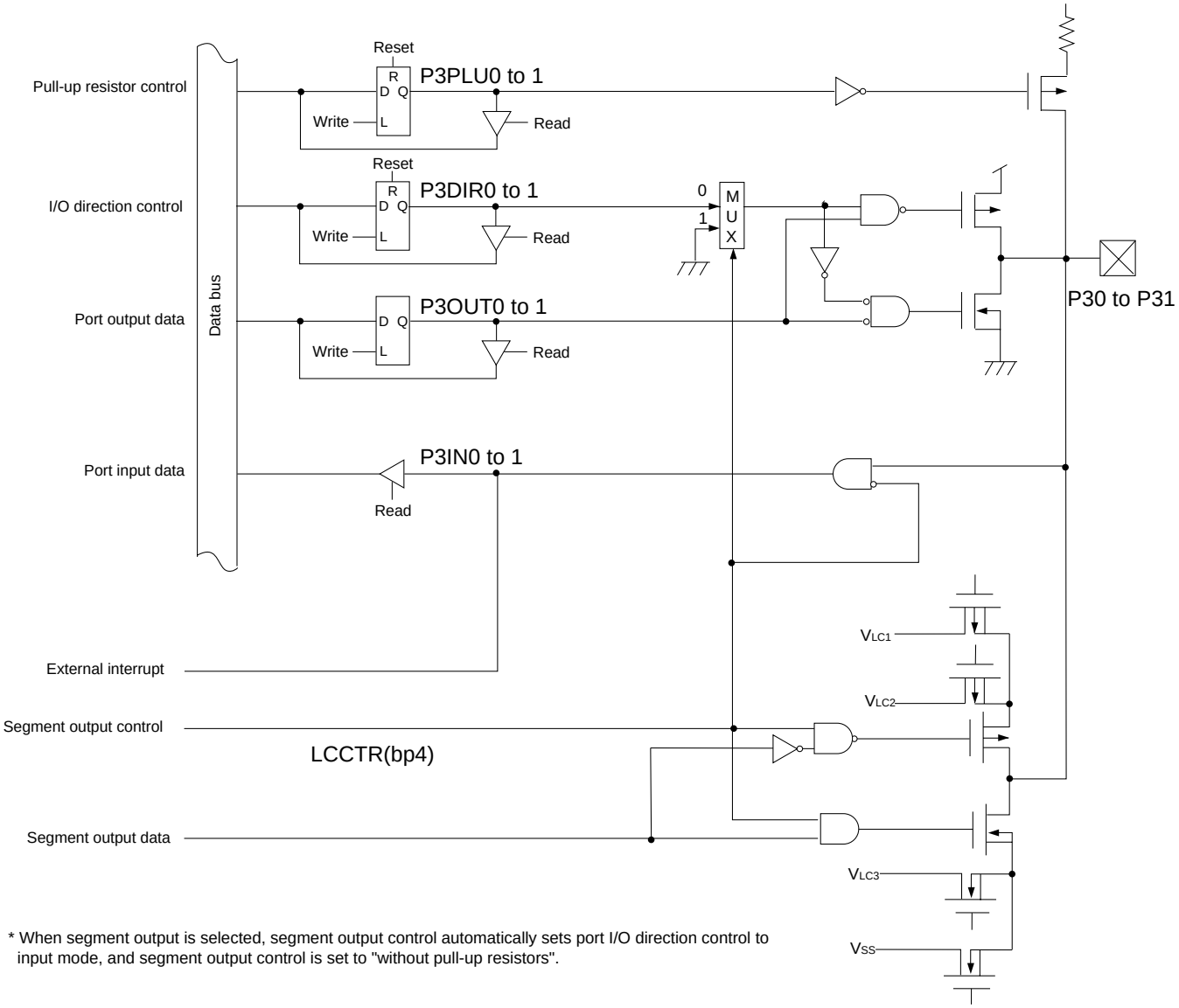

7 6 5 4 3 2 1 0
EXADV
EXADV3 EXADV2 EXADV1 — — — — —
(At reset : 0 0 0 - - - - -)
EXADV1
P73 to P70 (A11 to A8) address output control at memory expansion
0
"A11 to A8" address output disable
1
"A11 to A8" address output enable
EXADV2
P77 to P74 (A15 to A12) address output control at memory expansion
0
"A15 to A12" address output disable
1
"A15 to A12" address output enable
EXADV3
P35, P36 (A17, A16) address output control at memory expansion
0
"A17 to A16" address output disable
1
"A17 to A16" address output enable

Figure 4-5-4 Expansion address control Register (EXADV : x'03F0E, R/W)

4-5-3 Block Diagram



* When segment output is selected, segment output control automatically sets port I/O direction control to input mode, and segment output control is set to "without pull-up resistors".

Figure 4-5-5 Block Diagram (P30 to P31)

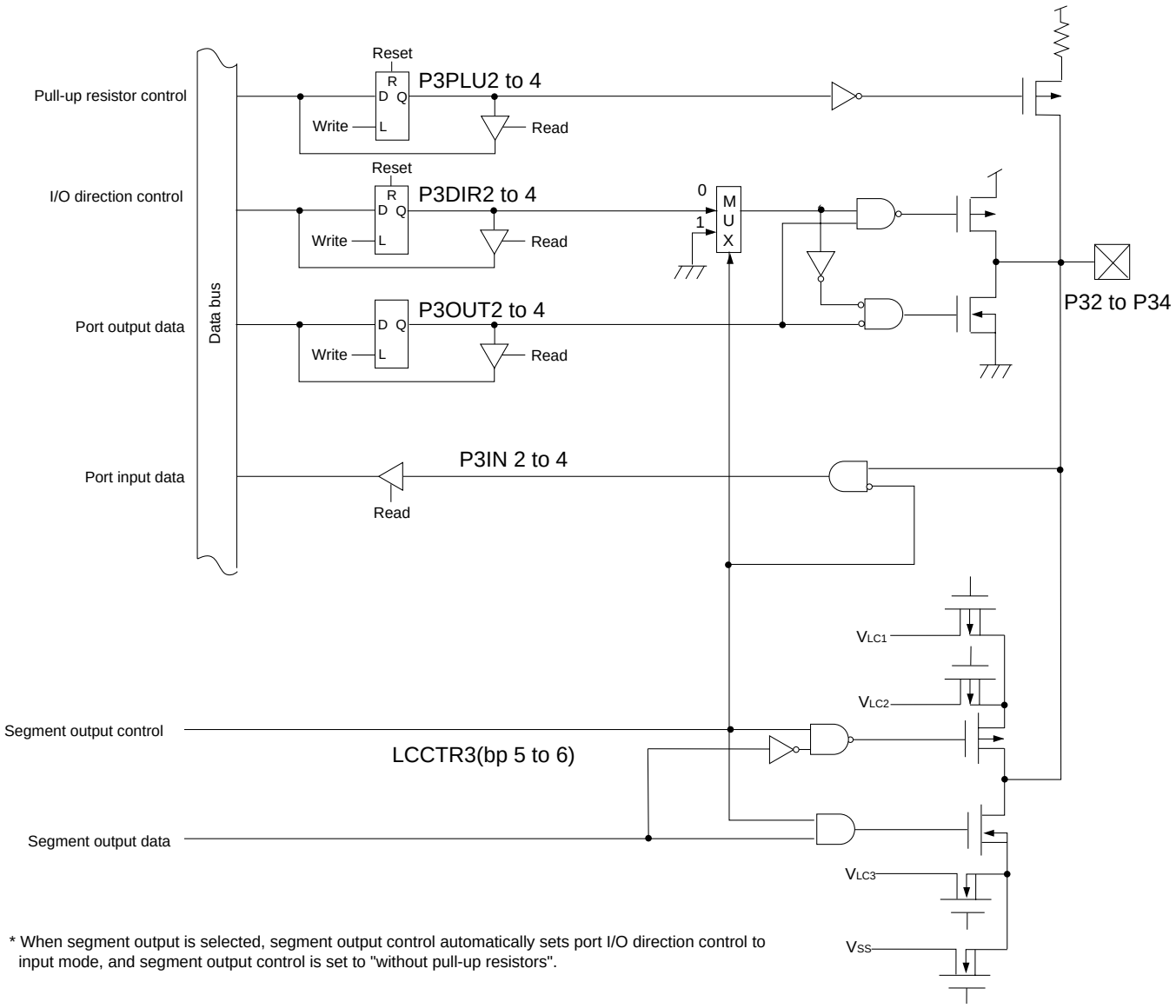


Figure 4-5-6 Block Diagram (P32 to P34)

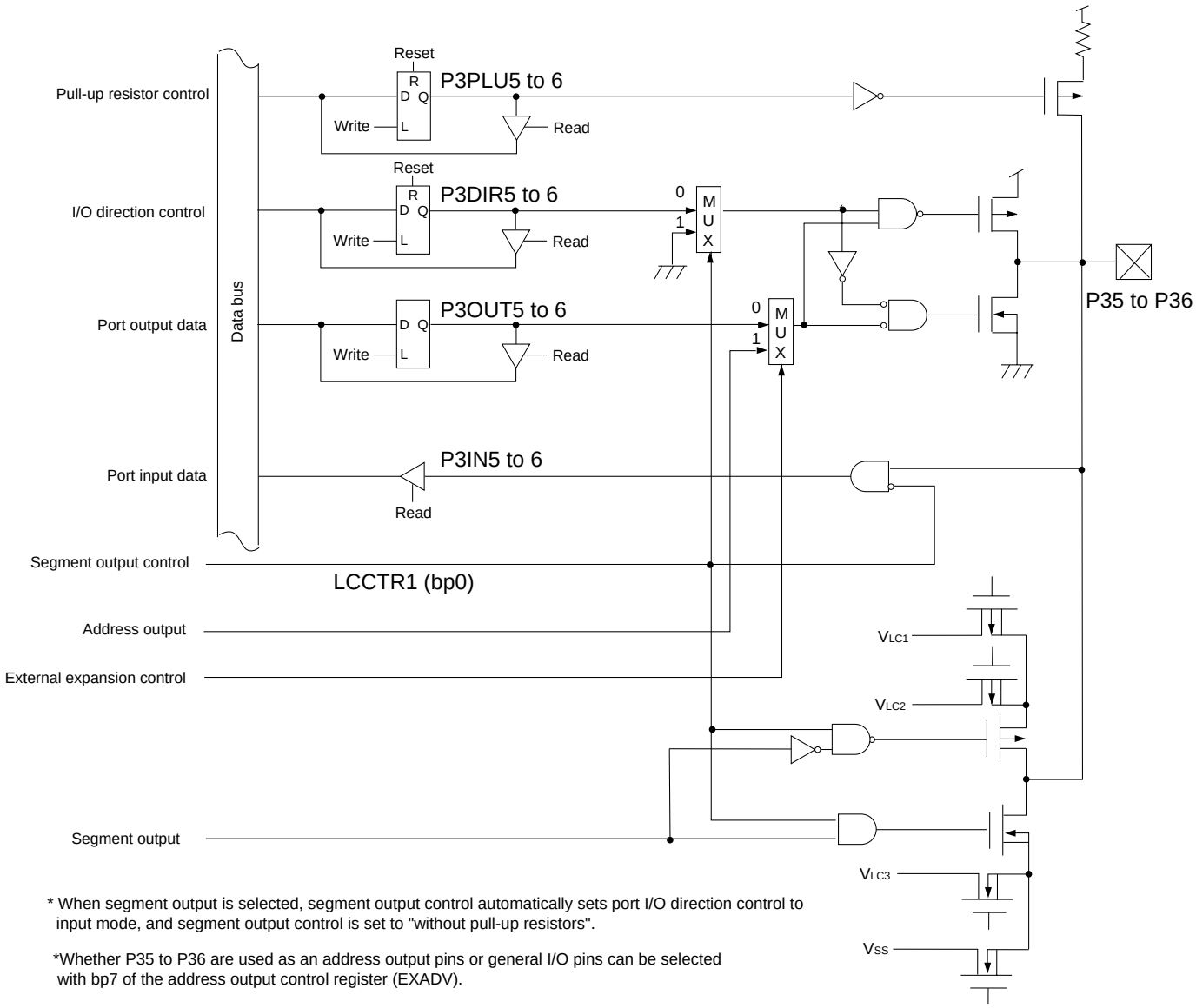


Figure 4-5-7 Block Diagram (P35 to P36)

4-6 Port 4

4-6-1 Description

■General Port Setup

Each bit can be set individually to either an input or output by the port 4 I/O direction control register (P4DIR). The control flag of the port 4 direction control register (P4DIR) is set to"1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 4 direction control register (P4DIR) to "0" and read the value of the port 4 input register (P4IN).

To output data to pin, set the control flag of the port 4 direction control register (P4DIR) to "1" and write data to the port 4 output register (P4OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 4 pull-up resistor control register (P4PLU). Set the control flag of the port 4 pull-up resistor control register (P4PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup

P40 to P47 are used as input pins for KEY interrupt, as well.

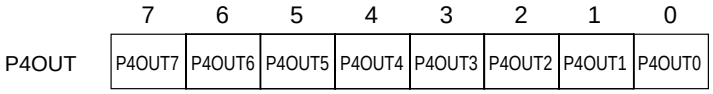
[☞ Chapter 3 3-3-6. Key Input Interrupt]

[☞ Chapter 3 3-3-2. Block Diagram, 3-3-3. Control Registers]

Each bit can be set individually to synchronous output by the port 4 synchronous output control register (P4SYO). The port 4 synchronous output control register (P4SYO) is set to "1" for synchronous output, and "0" for general port. The pin control register (FLOAT) can select the event that generates synchronous output. When the bp1, bp0 of the pin control register (FLOAT) is "00", the external interrupt 2 (IRQ2) is selected. And "01" for the timer 7 interrupt, "10" for the timer 2 interrupt, "11" for the timer 1 interrupt. For further detail, refer to 4-14. Synchronous output function [p.IV-68].

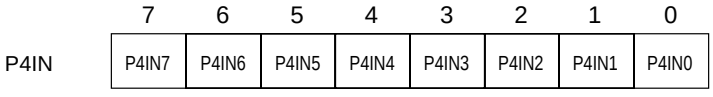
P40 to P47 can be used as the LCD segment output pin. Set "1" to bits 0 to 3 (LC3SL0 to LC3SL3) of the LCD output control register 3 (LCCTR3) to use SEG33 to SEG26 pins. The port and segment pins can be set by 2-bits. When segment output is selected, input mode is set and the pull-up resistors are set off automatically.

4-6-2 Registers



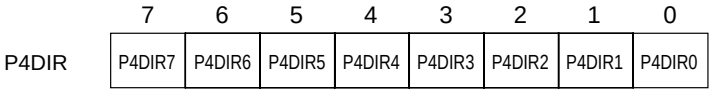
P4OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 4 output register (P4OUT : x'03F14', R/W)



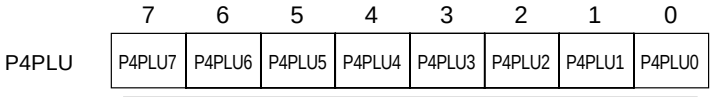
P4IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 4 input register (P4IN : x'03F24', R)



P4DIR	I/O mode selection
0	Input mode
1	Output mode

Port 4 direction control register (P4DIR : x'03F34', R/W)



P4PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 4 pull-up resistor control register (P4PLU : x'03F44', R/W)

Figure 4-6-1 Port 4 Registers (1/3)

	7	6	5	4	3	2	1	0	
P4SYO	P4SYO7	P4SYO6	P4SYO5	P4SYO4	P4SYO3	P4SYO2	P4SYO1	P4SYO0	(At reset : 0 0 0 0 0 0 0 0)

P4SYO	I/O port, synchronous output pin selection
0	I/O port (Disable synchronous output)
1	Synchronous output pin (Enable synchronous output)

Port 4 synchronous output control register (P4SYO : x'03F1E', R/W)

	7	6	5	4	3	2	1	0	
FLOAT	SC0SEL	PARDWN	P1RDWN	P0RDWN	—	—	SYOEVS1	SYOEVS0	(At reset : 0 0 0 0 - - 0 0)

SYOEVS1	SYOEVS0	P4 synchronous output event selection
0	0	External interrupt IRQ2
	1	Timer 7 interrupt
1	0	Timer 2 interrupt
	1	Timer 1 interrupt

P0RDWN	P0 pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

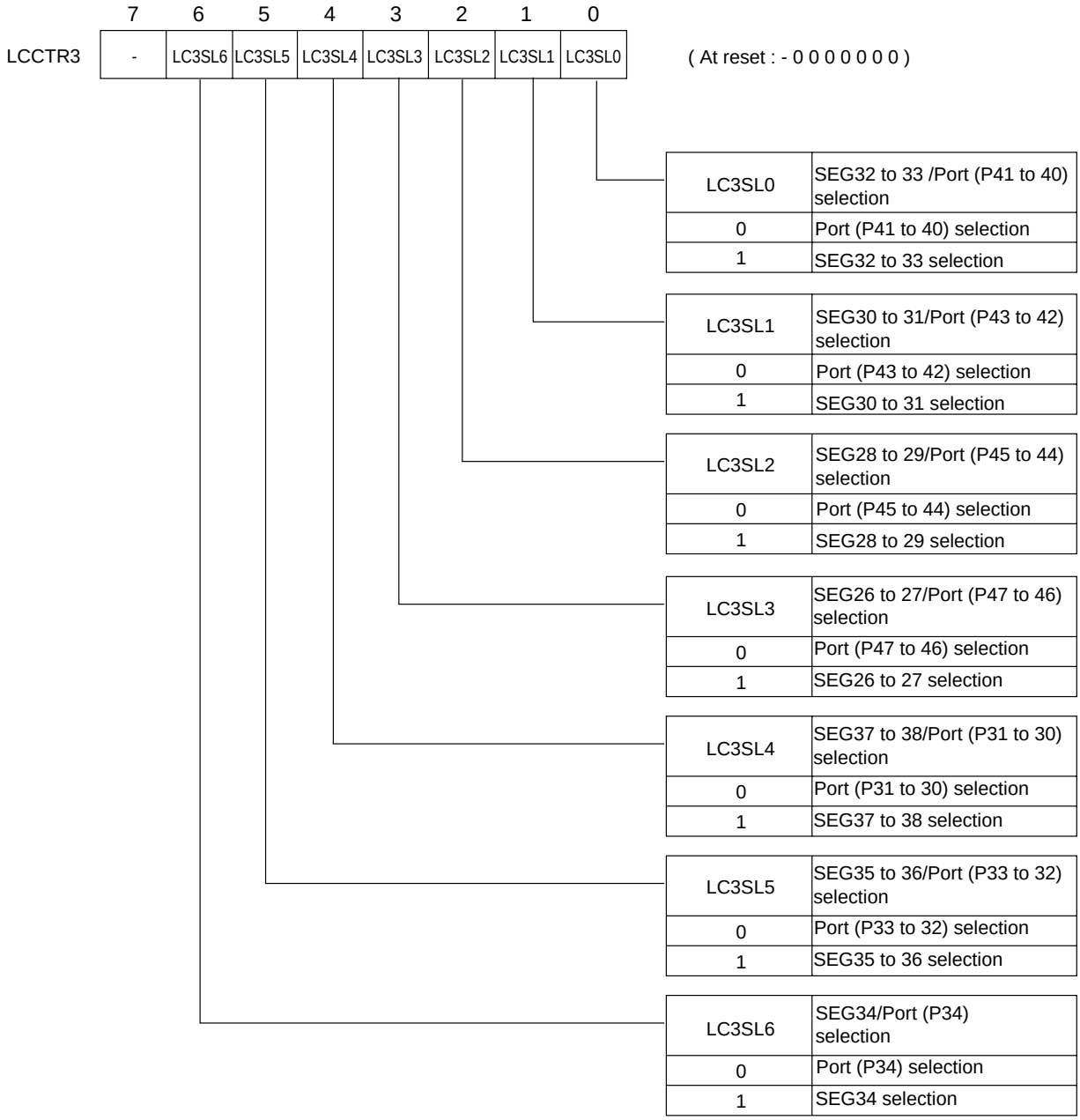
P1RDWN	P1 pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

PARDWN	PA pull-up / pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

SC0SEL	Serial interface 0 input / output pin selection
0	Port0
1	Port B

Pull-up / Pull-down resistor selection, Pin control register (FLOAT : x'03F2E', R/W)

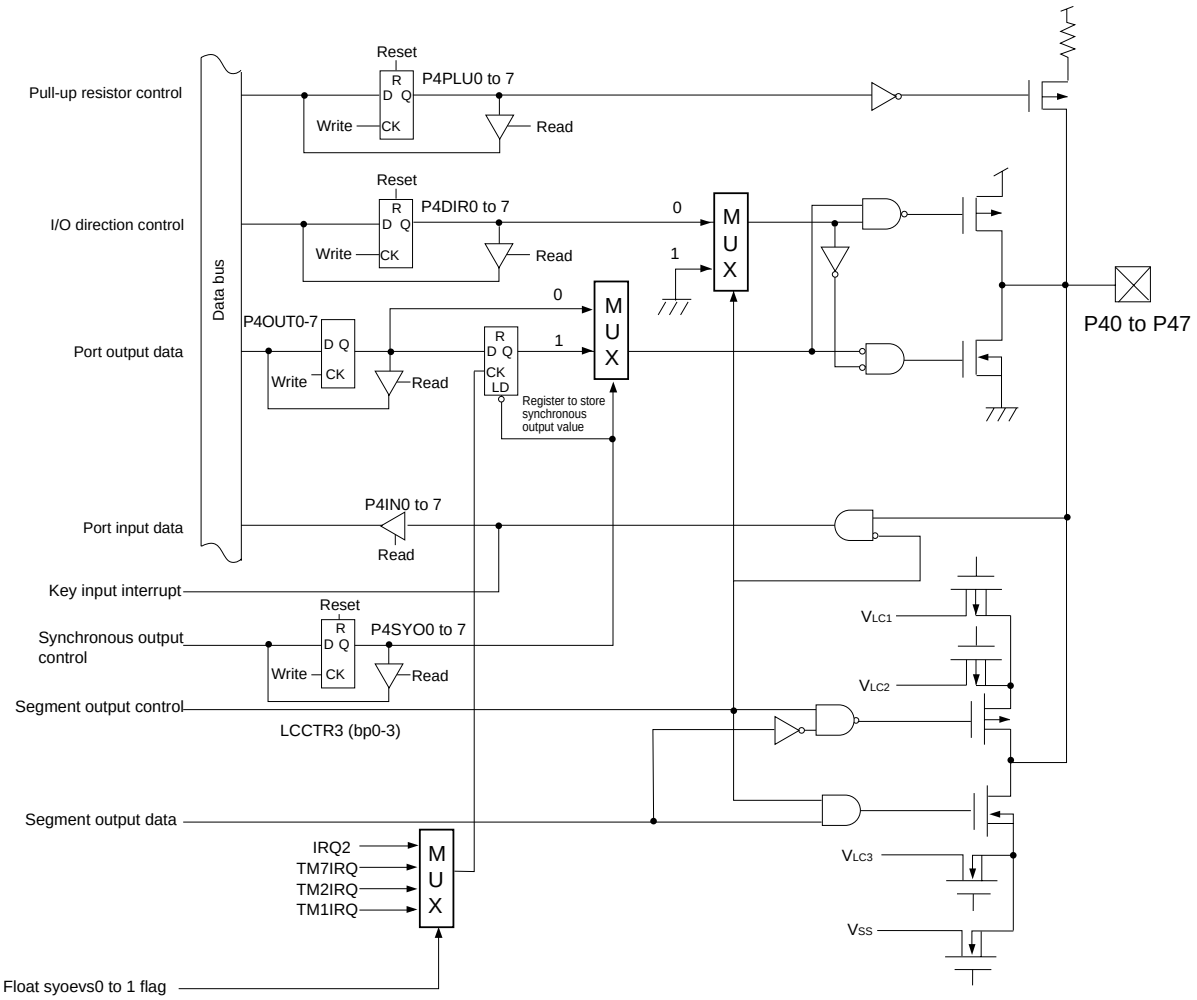
Figure 4-6-2 Port 4 Registers (2/3)


7 6 5 4 3 2 1 0
LCCTR3
- LC3SL6 LC3SL5 LC3SL4 LC3SL3 LC3SL2 LC3SL1 LC3SL0
(At reset : - 0 0 0 0 0 0 0)
LC3SL0 SEG32 to 33 /Port (P41 to 40) selection
0 Port (P41 to 40) selection
1 SEG32 to 33 selection
LC3SL1 SEG30 to 31/Port (P43 to 42) selection
0 Port (P43 to 42) selection
1 SEG30 to 31 selection
LC3SL2 SEG28 to 29/Port (P45 to 44) selection
0 Port (P45 to 44) selection
1 SEG28 to 29 selection
LC3SL3 SEG26 to 27/Port (P47 to 46) selection
0 Port (P47 to 46) selection
1 SEG26 to 27 selection
LC3SL4 SEG37 to 38/Port (P31 to 30) selection
0 Port (P31 to 30) selection
1 SEG37 to 38 selection
LC3SL5 SEG35 to 36/Port (P33 to 32) selection
0 Port (P33 to 32) selection
1 SEG35 to 36 selection
LC3SL6 SEG34/Port (P34) selection
0 Port (P34) selection
1 SEG34 selection

LCD Control Register 3 (LCCTR3 : X'03FDD', R/W)

Figure 4-6-3 Port 4 Registers (3/3)

4-6-3 Block Diagram



* When segment output is selected, segment output control automatically sets port I/O direction control to input mode, and segment output control is set to "without pull-up resistors".

Figure 4-6-4 Block Diagram (P40 to P47)

4-7 Port 5

4-7-1 Description

■General Port Setup

Each bit can be set individually to either an input or output by the port 5 I/O direction control register (P5DIR). The control flag of the port 5 direction control register (P5DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 5 direction control register (P5DIR) to "0" and read the value of the port 5 input register (P5IN).

To output data to pin, set the control flag of the port 5 direction control register (P5DIR) to "1" and write data to the port 5 output register (P5OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 5 pull-up resistor control register (P5PLU). Set the control flag of the port 5 pull-up resistor control register (P5PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup

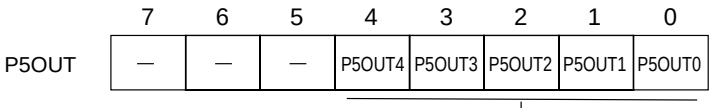
P50 to P54 are large current output pins and can be used as output pins of timer 0, timer 7, timer 2, and timer 8. The output mode for each pin can be selected with port 5 output mode register (P5OMD). When "1" is set to the port 5 output mode resister (P5OMD), each pin can be used as the timer output pin. When "0" is set to the port 5 output mode register (P5OMD), each pin can be used as the general purpose port pin.

P50 to P52 are used as output pins of control signal to external expansion memory in memory expansion mode. This mode automatically sets P50 to P52 to output mode.

Table 4-7-1 P50 to P52

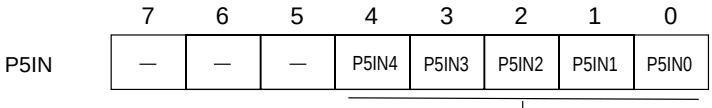
Pin	In Memory expansion mode *
P50	NWE
P51	NRE
P52	NCS

4-7-2 Registers



P5OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 5 output register (P5OUT : x'03F15', R/W)

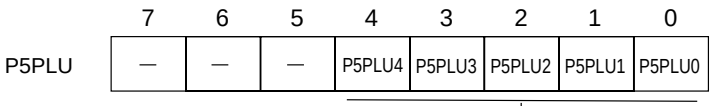


P5IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 5 input register (P5IN : x'03F25', R)

P5DIR	I/O mode selection
0	Input mode
1	Output mode

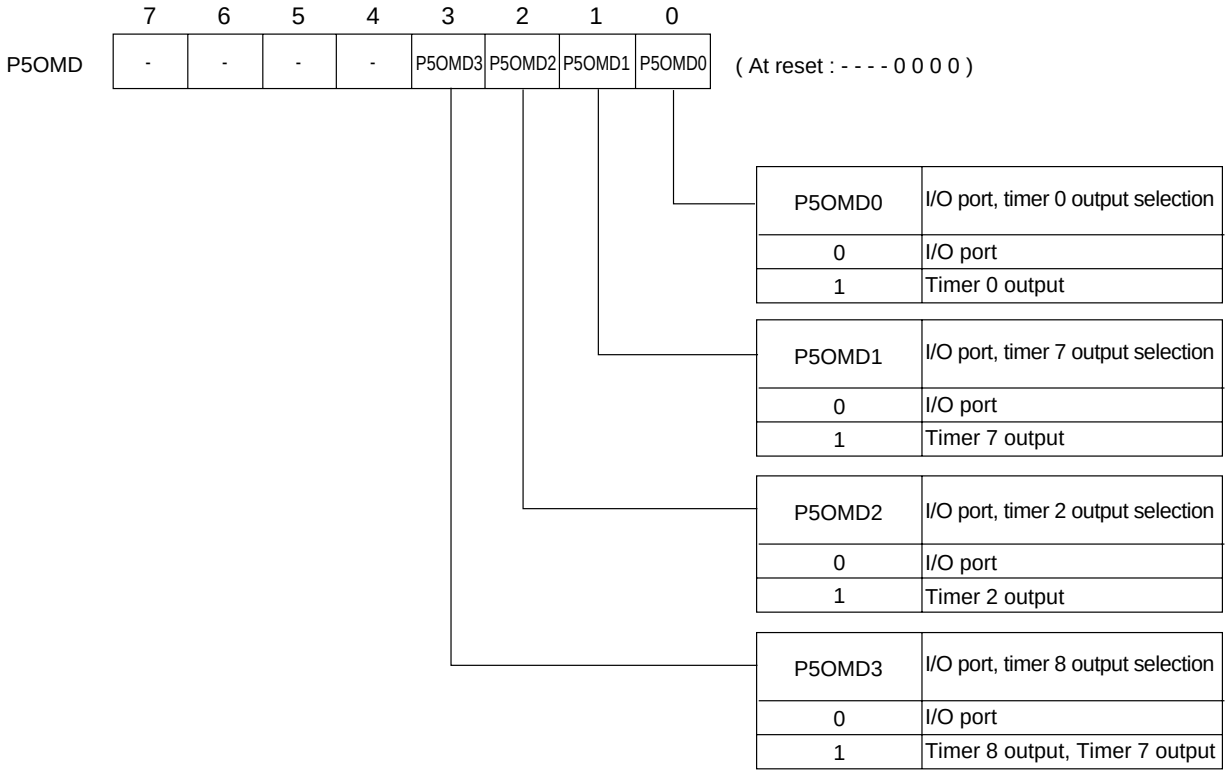
Port 5 direction control register (P5DIR : x'03F35', R/W)



P5PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

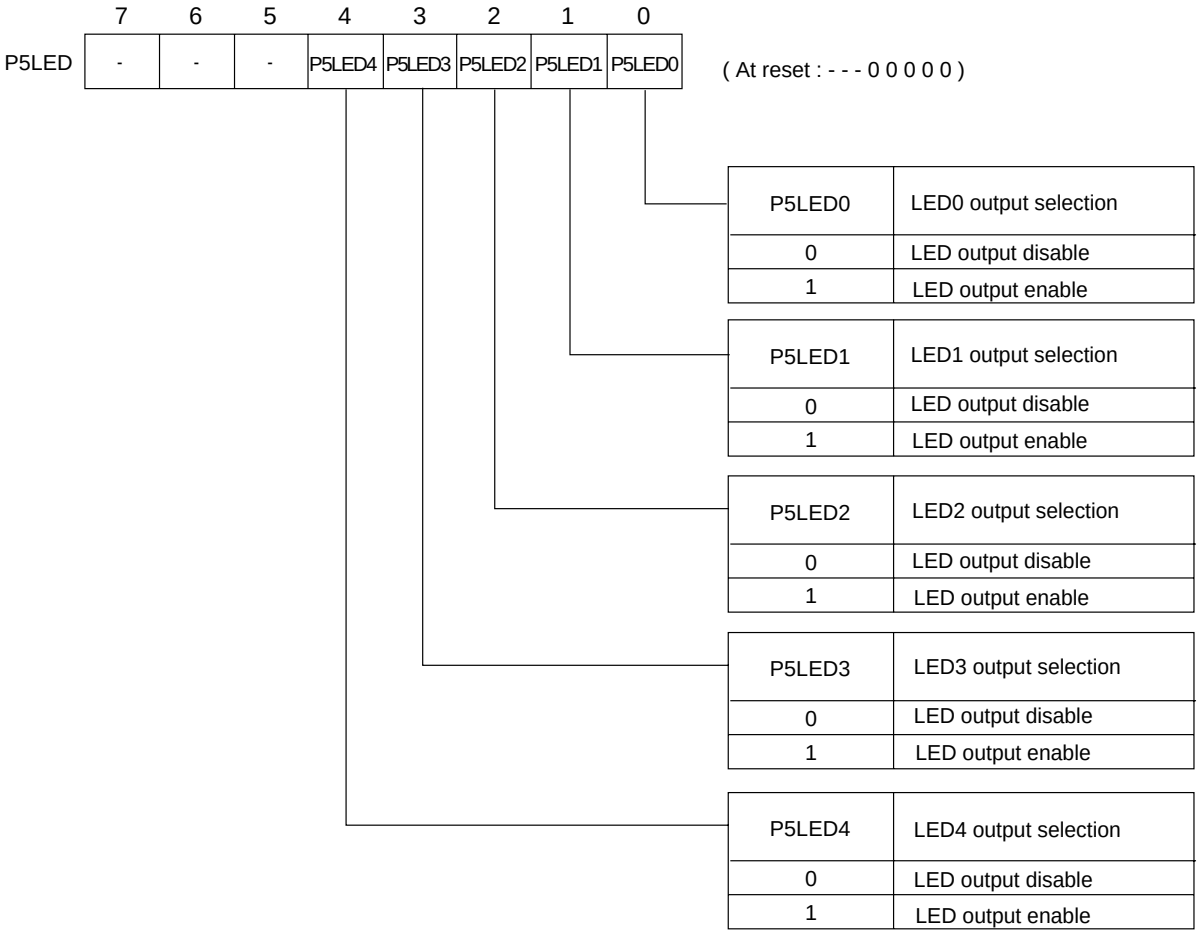
Port 5 pull-up resistor control register (P5PLU : x'03F45', R/W)

Figure 4-7-1 Port 5 Registers (1/3)


7 6 5 4 3 2 1 0
P5OMD
- - - - P5OMD3 P5OMD2 P5OMD1 P5OMD0
(At reset : - - - - 0 0 0 0)
P5OMD0 I/O port, timer 0 output selection
0 I/O port
1 Timer 0 output
P5OMD1 I/O port, timer 7 output selection
0 I/O port
1 Timer 7 output
P5OMD2 I/O port, timer 2 output selection
0 I/O port
1 Timer 2 output
P5OMD3 I/O port, timer 8 output selection
0 I/O port
1 Timer 8 output, Timer 7 output

Port 5 Output Mode Register (P5OMD : X'03F3F', R/W)

Figure 4-7-2 Port 5 Registers (2/3)


7 6 5 4 3 2 1 0
P5LED
- - - P5LED4 P5LED3 P5LED2 P5LED1 P5LED0
(At reset : - - - 0 0 0 0 0)
P5LED0 LED0 output selection
0 LED output disable
1 LED output enable
P5LED1 LED1 output selection
0 LED output disable
1 LED output enable
P5LED2 LED2 output selection
0 LED output disable
1 LED output enable
P5LED3 LED3 output selection
0 LED output disable
1 LED output enable
P5LED4 LED4 output selection
0 LED output disable
1 LED output enable

Port5 Large Current Drive Control Register (P5LED : X'03F4F', R/W)

Figure 4-7-3 Port 5 Registers (3/3)

4-7-3 Block Diagram

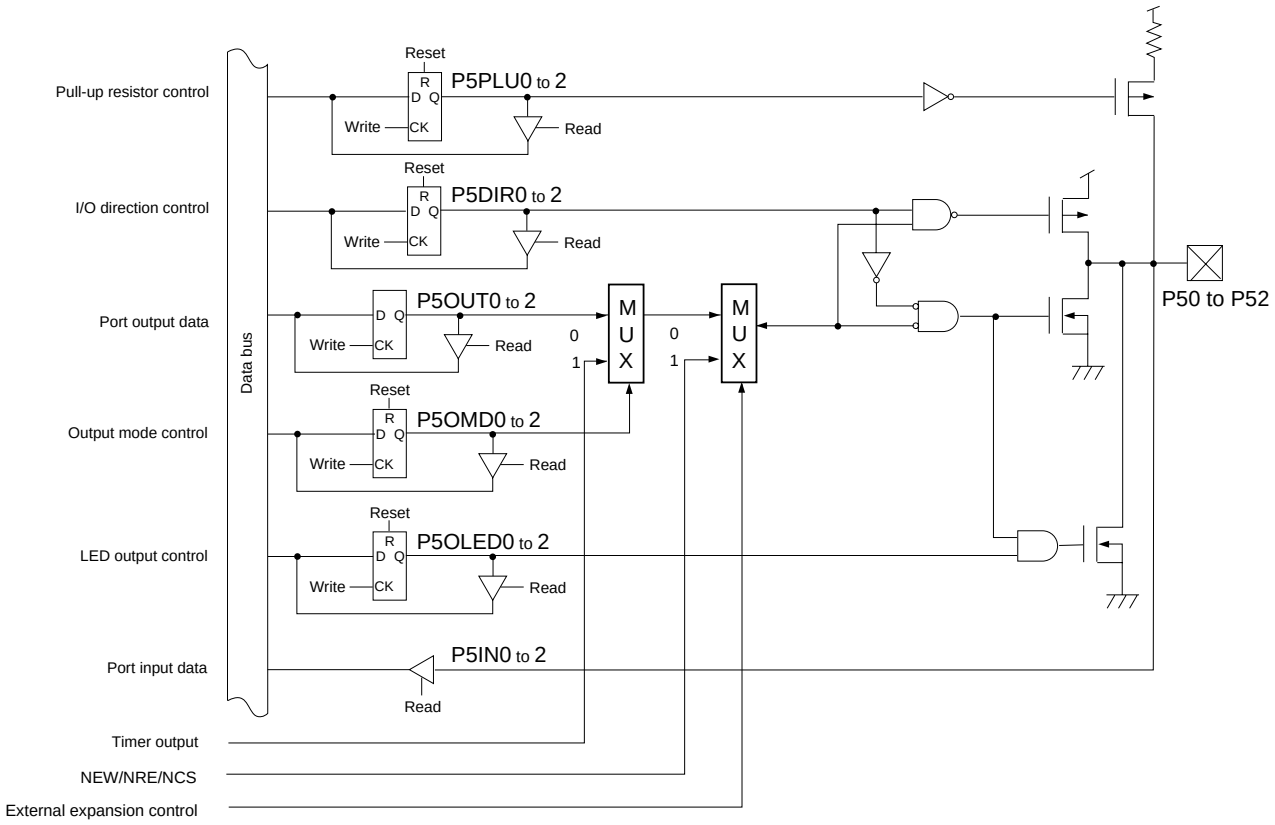


Figure 4-7-4 Block Diagram (P50 to P52)

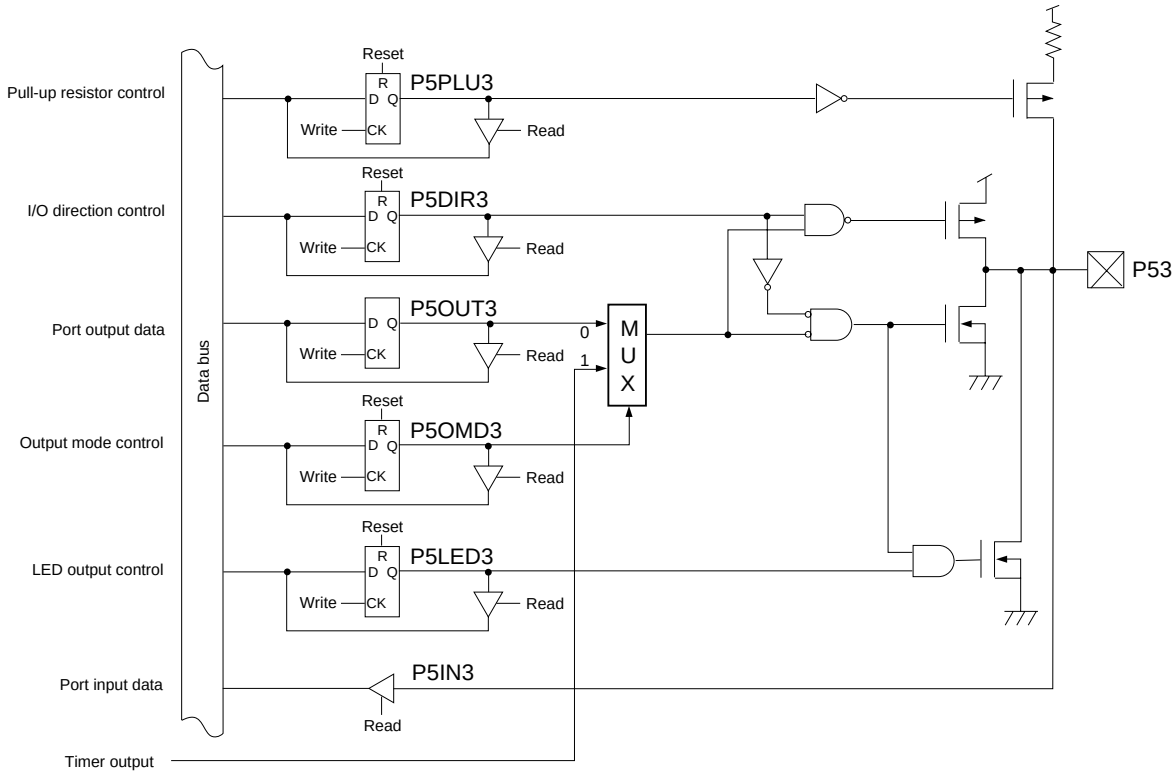


Figure 4-7-5 Block Diagram (P53)

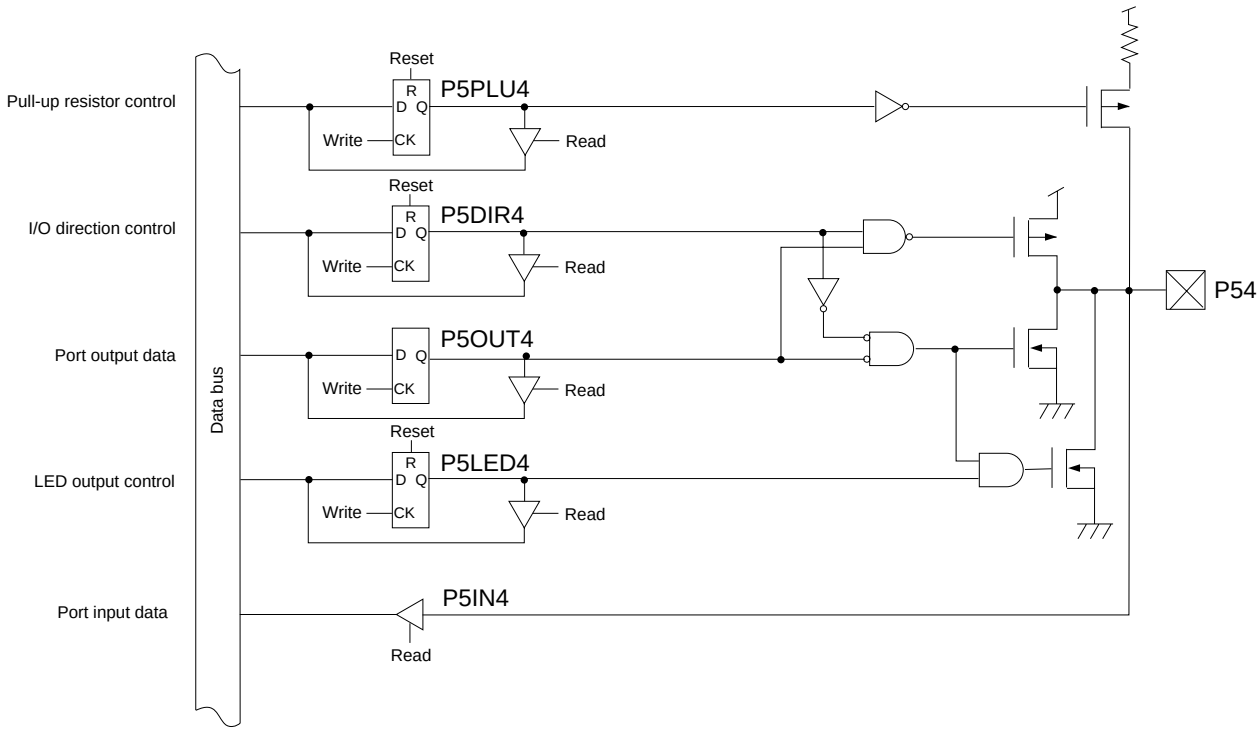


Figure 4-7-6 Block Diagram (P54)

4-8 Port 6

4-8-1 Description

■General port Setup
Each bit can be set individually to either an input or output by the port 6 I/O direction control register (P6DIR). The control flag of the port 6 direction control register (P6DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 6 direction control register (P6DIR) to "0" and read the value of the port 6 input register (P6IN).

To output data to pin, set the control flag of the port 6 direction control register (P6DIR) to "1" and write data to the port 6 output register (P6OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 6 pull-up resistor control register (P6PLU). Set the control flag of the port 6 pull-up resistor control register (P6PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup
P60 to P67 can be used as the LCD segment output pins, as well. To use these ports as SEG25 to SEG18 pins, set "1" to bit0 to 3 (LC2SL0 to LC2SL3) in the LCD output control register 2 (LCCTR2). The ports and the segments can be switched by 2-bits. When segment output is selected, input mode is set and the pull-up resistors are set off automatically.
P60 to P67 are address output pins of external expansion memory in memory expansion mode.
In this mode, controling I/O with registers is disabled. These ports output address only at accessing to the external expansion memory and are in high-impedance condision (input mode) at any other time (NCS="H").

Table 4-8-1 P60 to P67 External Expansion pins

Pin	In Memory expansion mode *
P60	A0 (External memory address bp0)
P61	A1 (External memory address bp1)
P62	A2 (External memory address bp2)
P63	A3 (External memory address bp3)
P64	A4 (External memory address bp4)
P65	A5 (External memory address bp5)
P66	A6 (External memory address bp6)
P67	A7 (External memory address bp7)

4-8-2 Registers

	7	6	5	4	3	2	1	0	
P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	(At reset : X X X X X X X X)

P6OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 6 output register (P6OUT : x'03F16', R/W)

	7	6	5	4	3	2	1	0	
P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	(At reset : X X X X X X X X)

P6IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 6 intput register (P6IN : x'03F26', R)

	7	6	5	4	3	2	1	0	
P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	(At reset : 0 0 0 0 0 0 0 0)

P6DIR	I/O mode selection
0	Input mode
1	Output mode

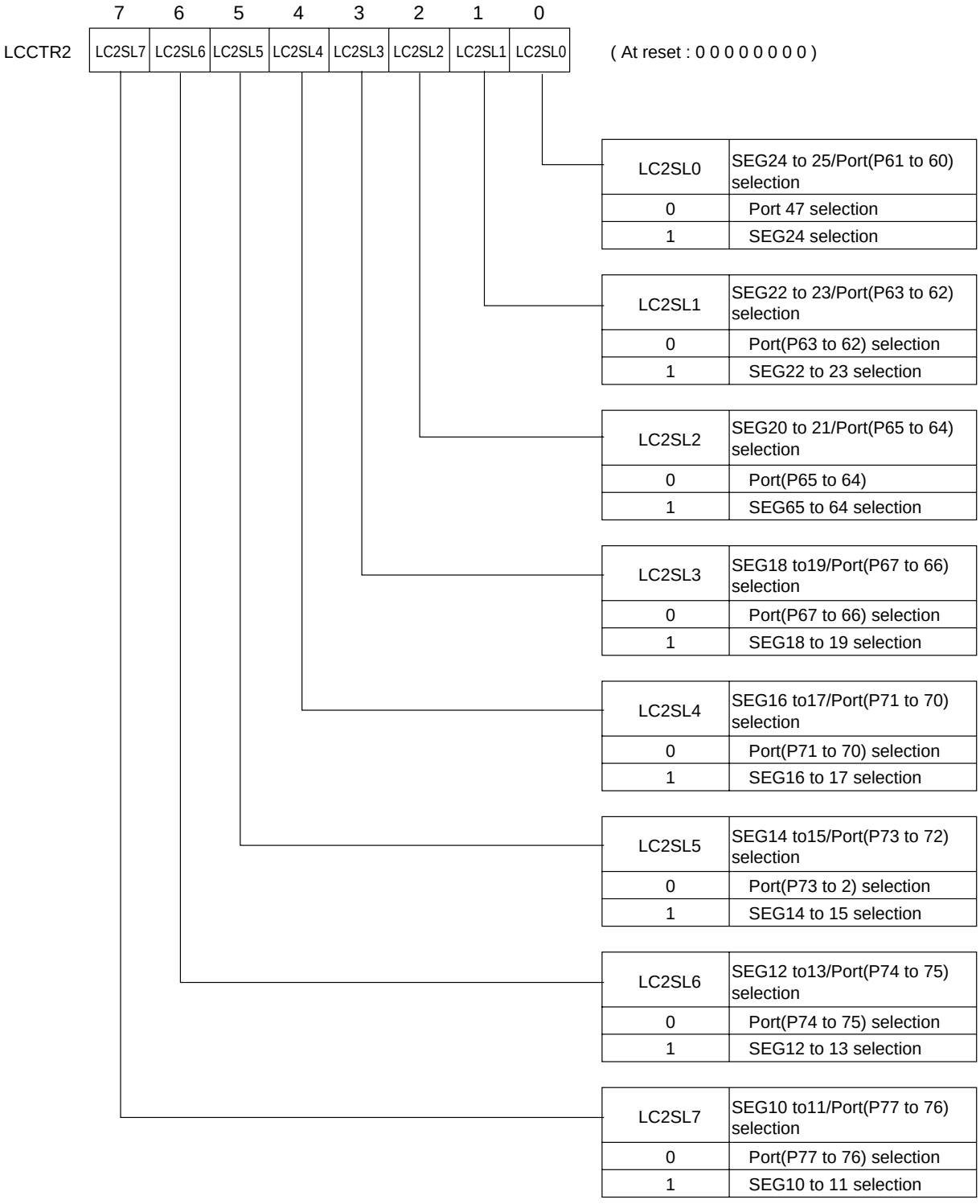
Port 6 direction control register (P6DIR : x'03F36', R/W)

	7	6	5	4	3	2	1	0	
P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	(At reset : 0 0 0 0 0 0 0 0)

P6PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 6 pull-up resistor control register (P6PLU : x'03F46', R/W)

Figure 4-8-1 Port 6 Registers (1/2)


7 6 5 4 3 2 1 0
LCCTR2
LC2SL7 LC2SL6 LC2SL5 LC2SL4 LC2SL3 LC2SL2 LC2SL1 LC2SL0
(At reset : 0 0 0 0 0 0 0 0)
LC2SL0 SEG24 to 25/Port(P61 to 60) selection
0 Port 47 selection
1 SEG24 selection
LC2SL1 SEG22 to 23/Port(P63 to 62) selection
0 Port(P63 to 62) selection
1 SEG22 to 23 selection
LC2SL2 SEG20 to 21/Port(P65 to 64) selection
0 Port(P65 to 64)
1 SEG65 to 64 selection
LC2SL3 SEG18 to19/Port(P67 to 66) selection
0 Port(P67 to 66) selection
1 SEG18 to 19 selection
LC2SL4 SEG16 to17/Port(P71 to 70) selection
0 Port(P71 to 70) selection
1 SEG16 to 17 selection
LC2SL5 SEG14 to15/Port(P73 to 72) selection
0 Port(P73 to 2) selection
1 SEG14 to 15 selection
LC2SL6 SEG12 to13/Port(P74 to 75) selection
0 Port(P74 to 75) selection
1 SEG12 to 13 selection
LC2SL7 SEG10 to11/Port(P77 to 76) selection
0 Port(P77 to 76) selection
1 SEG10 to 11 selection

LCD Control Register 2(LCCTR2 : X'03FDC', R/W)

Figure 4-8-2 Port 6 Registers (2/2)

4-8-3 Block Diagram

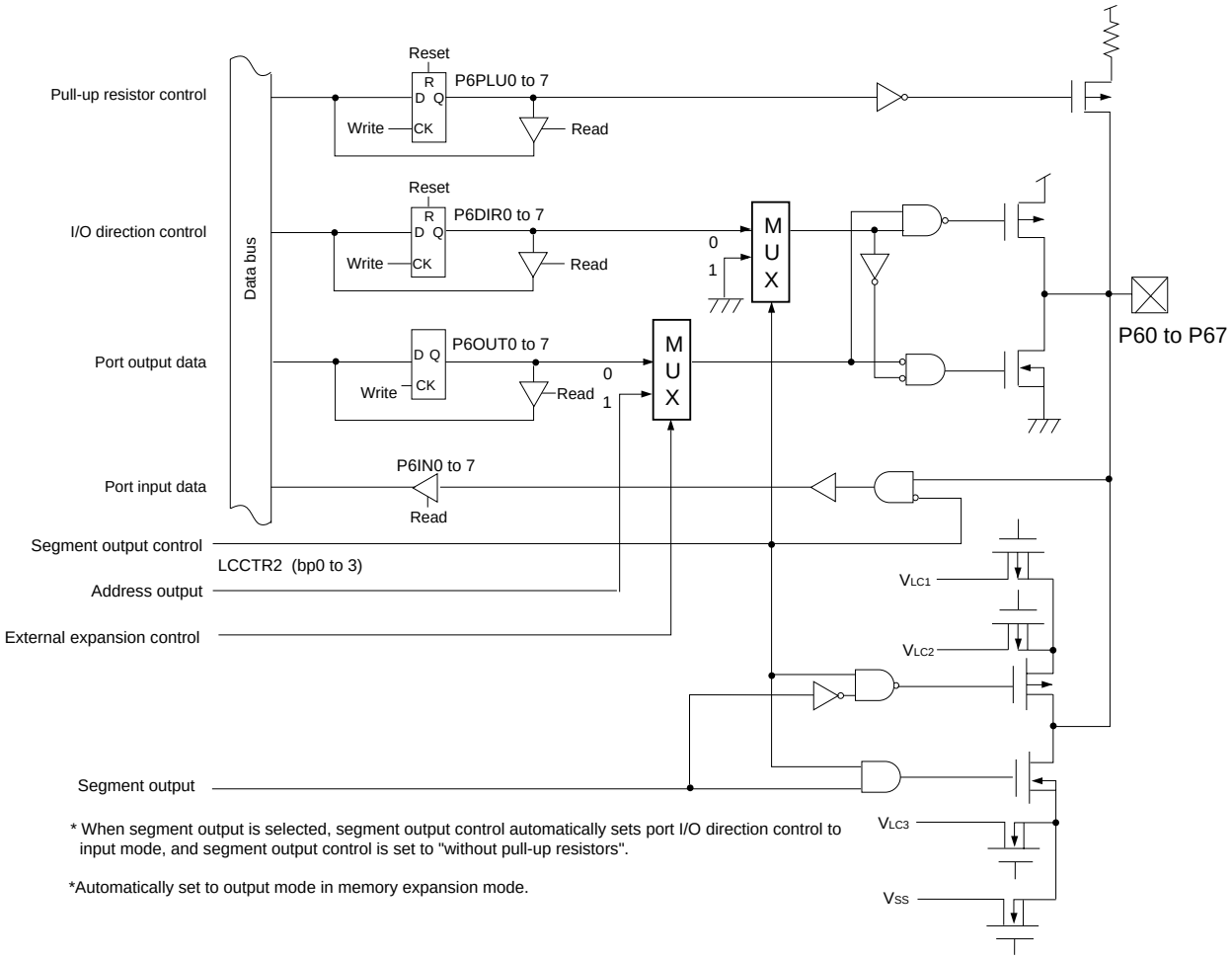


Figure 4-8-3 Block Diagram (P60 to P67)

4-9 Port 7

4-9-1 Description

■General Port Setup
Each bit can be set individually to either an input or output by the port 7 I/O direction control register (P7DIR). The control flag of the port 5 direction control register (P7DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 7 direction control register (P7DIR) to "0" and read the value of the port 7 input register (P7IN).

To output data to pin, set the control flag of the port 7 direction control register (P7DIR) to "1" and write data to the port 7 output register (P7OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 7 pull-up resistor control register (P7PLU). Set the control flag of the port 7 pull-up resistor control register (P7PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup
P70 to P77 can be used as the LCD segment output pins, as well. When used as SEG17 to SEG10 pins, set "1" of bit 4 to 7 (LC2SL4 to LC2SL7) in the LCD output control register 2 (LCCTR2). The ports and the segments can be switched by 2-bits. When segment output is selected, input mode is set and the pull-up resistors are set off automatically.
P70 to P77 are address output pins of external expansion memory in memory expansion mode.
Whether they are used as an address output pins or general I/O pins can be selected with bp5 and bp6 of the address output control register (EXADV).

Table 4-9-1 P70 to P77 External Expansion pins

Pin	In Memory expansion mode *
P70	A8 (External memory address bp8)
P71	A9 (External memory address bp9)
P72	A10 (External memory address bp10)
P73	A11 (External memory address bp11)
P74	A12 (External memory address bp12)
P75	A13 (External memory address bp13)
P76	A14 (External memory address bp14)
P77	A15 (External memory address bp15)

*P70 to 77 do not output address without setting bp5 and bp6 of the EXADV register to "1".

4-9-2 Registers

	7	6	5	4	3	2	1	0	
P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	(At reset : X X X X X X X X)

P7OUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port 7 output register (P7OUT : x'03F17', R/W)

	7	6	5	4	3	2	1	0	
P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	(At reset : X X X X X X X X)

P7IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 7 input register (P7IN : x'03F27', R)

	7	6	5	4	3	2	1	0	
P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	(At reset : 0 0 0 0 0 0 0 0)

P7DIR	I/O mode selection
0	Input mode
1	Output mode

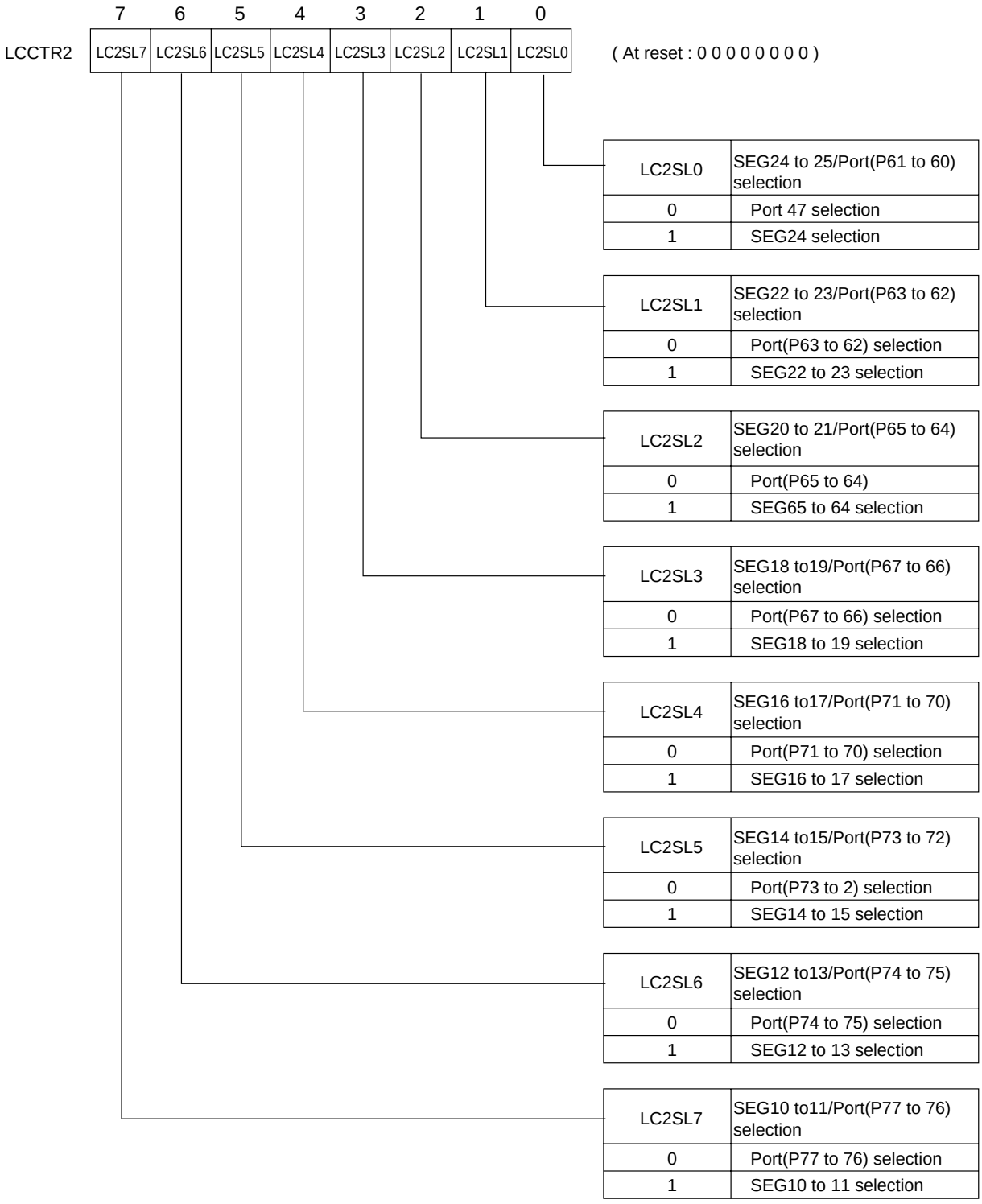
Port 7 direction control register (P7DIR : x'03F37', R/W)

	7	6	5	4	3	2	1	0	
P7PLU	P7PLU7	P7PLU6	P7PLU5	P7PLU4	P7PLU3	P7PLU2	P7PLU1	P7PLU0	(At reset : 0 0 0 0 0 0 0 0)

P7PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

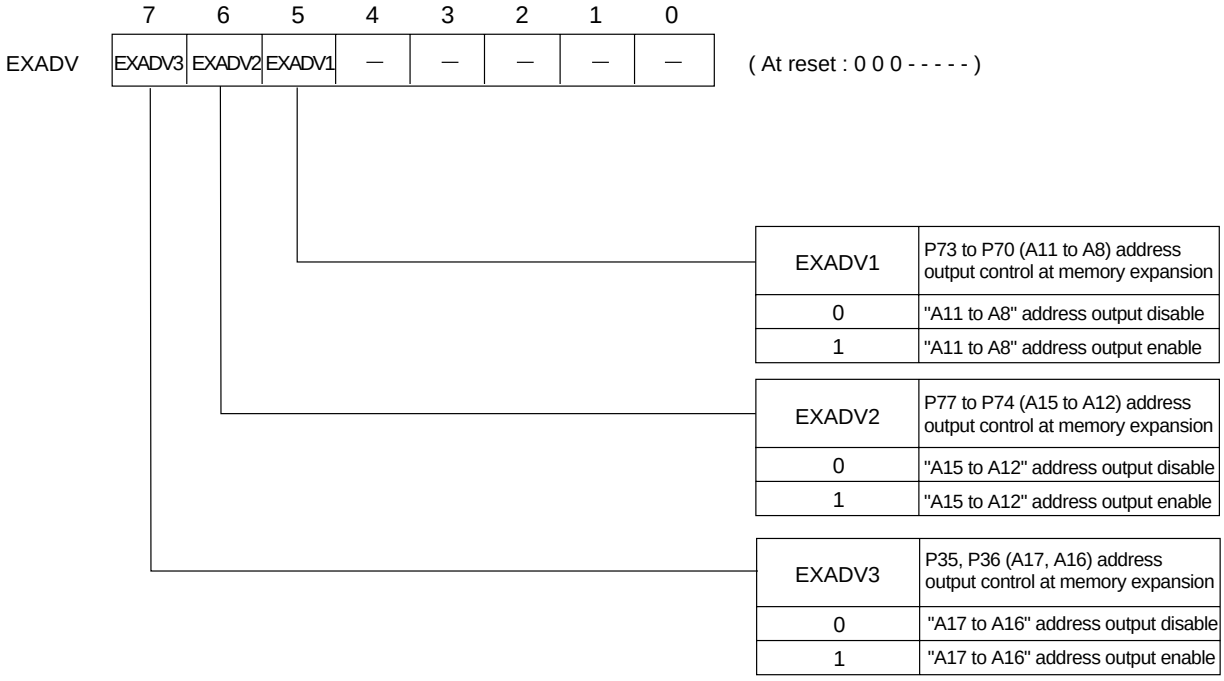
Port 7 pull-up resistor control register (P7PLUD : x'03F47', R/W)

Figure 4-9-1 Port 7 Registers (1/2)


7 6 5 4 3 2 1 0
LCCTR2
LC2SL7 LC2SL6 LC2SL5 LC2SL4 LC2SL3 LC2SL2 LC2SL1 LC2SL0
(At reset : 0 0 0 0 0 0 0 0)
LC2SL0 SEG24 to 25/Port(P61 to 60) selection
0 Port 47 selection
1 SEG24 selection
LC2SL1 SEG22 to 23/Port(P63 to 62) selection
0 Port(P63 to 62) selection
1 SEG22 to 23 selection
LC2SL2 SEG20 to 21/Port(P65 to 64) selection
0 Port(P65 to 64)
1 SEG65 to 64 selection
LC2SL3 SEG18 to19/Port(P67 to 66) selection
0 Port(P67 to 66) selection
1 SEG18 to 19 selection
LC2SL4 SEG16 to17/Port(P71 to 70) selection
0 Port(P71 to 70) selection
1 SEG16 to 17 selection
LC2SL5 SEG14 to15/Port(P73 to 72) selection
0 Port(P73 to 2) selection
1 SEG14 to 15 selection
LC2SL6 SEG12 to13/Port(P74 to 75) selection
0 Port(P74 to 75) selection
1 SEG12 to 13 selection
LC2SL7 SEG10 to11/Port(P77 to 76) selection
0 Port(P77 to 76) selection
1 SEG10 to 11 selection

LCD Control Register 2(LCCTR2 : X'03FDC', R/W)

Figure 4-9-2 Port 7 Registers (2/2)



EXADV1	P73 to P70 (A11 to A8) address output control at memory expansion
0	"A11 to A8" address output disable
1	"A11 to A8" address output enable

EXADV2	P77 to P74 (A15 to A12) address output control at memory expansion
0	"A15 to A12" address output disable
1	"A15 to A12" address output enable

EXADV3	P35, P36 (A17, A16) address output control at memory expansion
0	"A17 to A16" address output disable
1	"A17 to A16" address output enable

Figure 4-9-3 Expansion Address Control Registers

4-9-3 Block Diagram

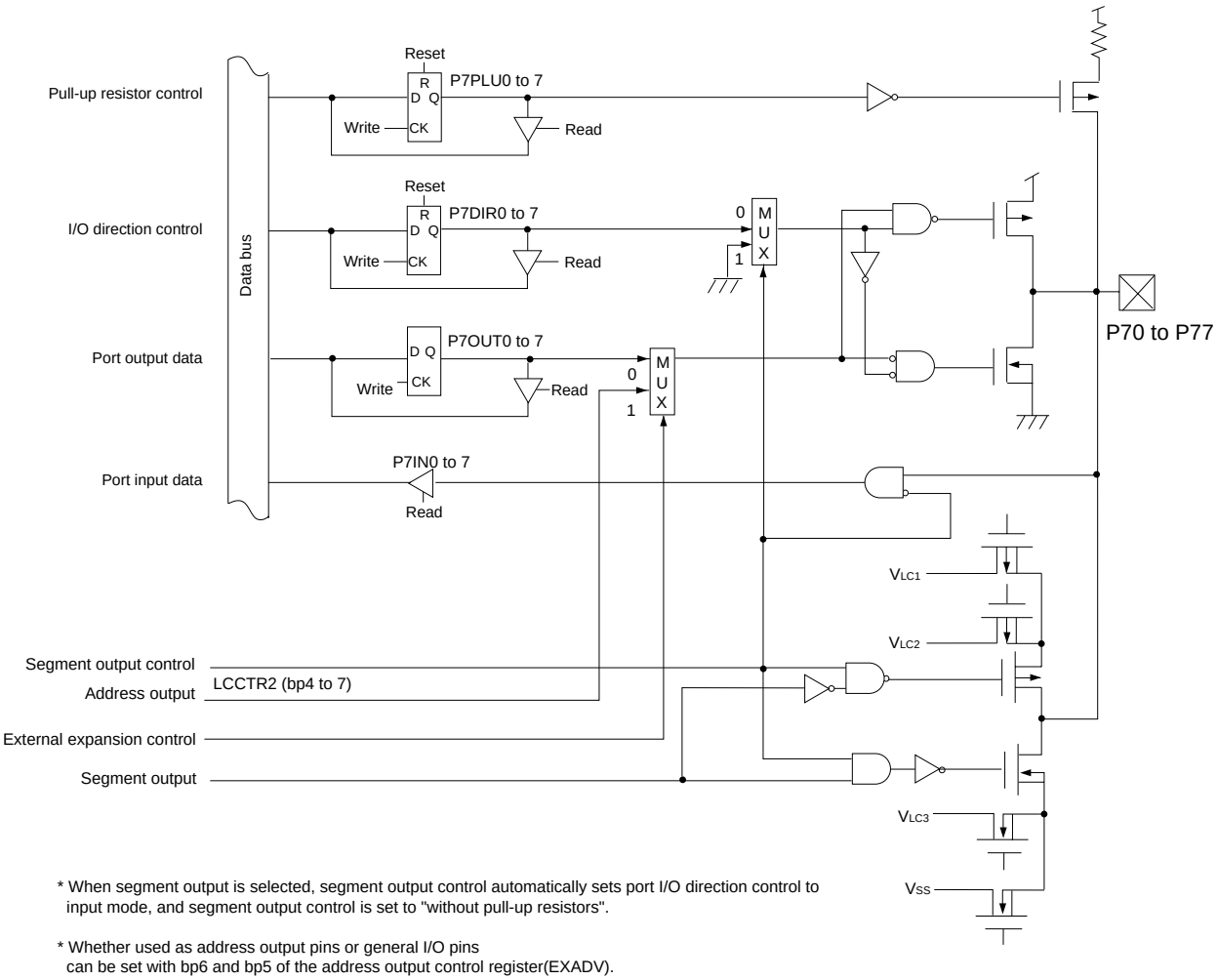


Figure 4-9-4 Block Diagram (P70 to P77)

4-10 Port 8

4-10-1 Description

■General Port Setup
Each bit can be set individually to either an input or output by the port 8 control I/O direction register (P8DIR). The control flag of the port 8 direction control register (P8DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 8 direction control register (P8DIR) to "0" and read the value of the port 8 input register (P8IN).

To output data to pin, set the control flag of the port 8 direction control register (P8DIR) to "1" and write data to the port 8 output register (P8OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 8 pull-up resistor control register (P8PLU). Set the control flag of the port 8 pull-up resistor control register (P8PLU) to "1" to add pull-up resistor.

■ Special Function Pin Setup
P80 to P87 can be used as the LCD segment output pins. To use these ports as SEG0 to SEG7 pins, set "1" to bit 1 (LC1SL1) in the LCD output control register 1 (LCCTR1). The ports and the segments can be switched by 8-bits. When segment output is selected, input mode is set and the pull-up resistors are set off automatically.
P80 to P87 are data I/O pins of external expansion memory in memory expansion mode.
In this mode, controling I/O with registers is disabled.

Table 4-9-1 P80 to P87 External Expansion pins

Pin	In Memory expansion mode *
P80	D0 (External memory address bp0)
P81	D1 (External memory address bp1)
P82	D2 (External memory address bp2)
P83	D3 (External memory address bp3)
P84	D4 (External memory address bp4)
P85	D5 (External memory address bp5)
P86	D6 (External memory address bp6)
P87	D7 (External memory address bp7)

4-10-2 Registers

	7	6	5	4	3	2	1	0	
P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	(At reset : X X X X X X X X)

P8OUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port 8 output register (P8OUT : x'03F18', R/W)

	7	6	5	4	3	2	1	0	
P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	(At reset : X X X X X X X X)

P8IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 8 input register (P8IN : x'03F28', R)

	7	6	5	4	3	2	1	0	
P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	(At reset : 0 0 0 0 0 0 0 0)

P8DIR	I/O mode selection
0	Input mode
1	Output mode

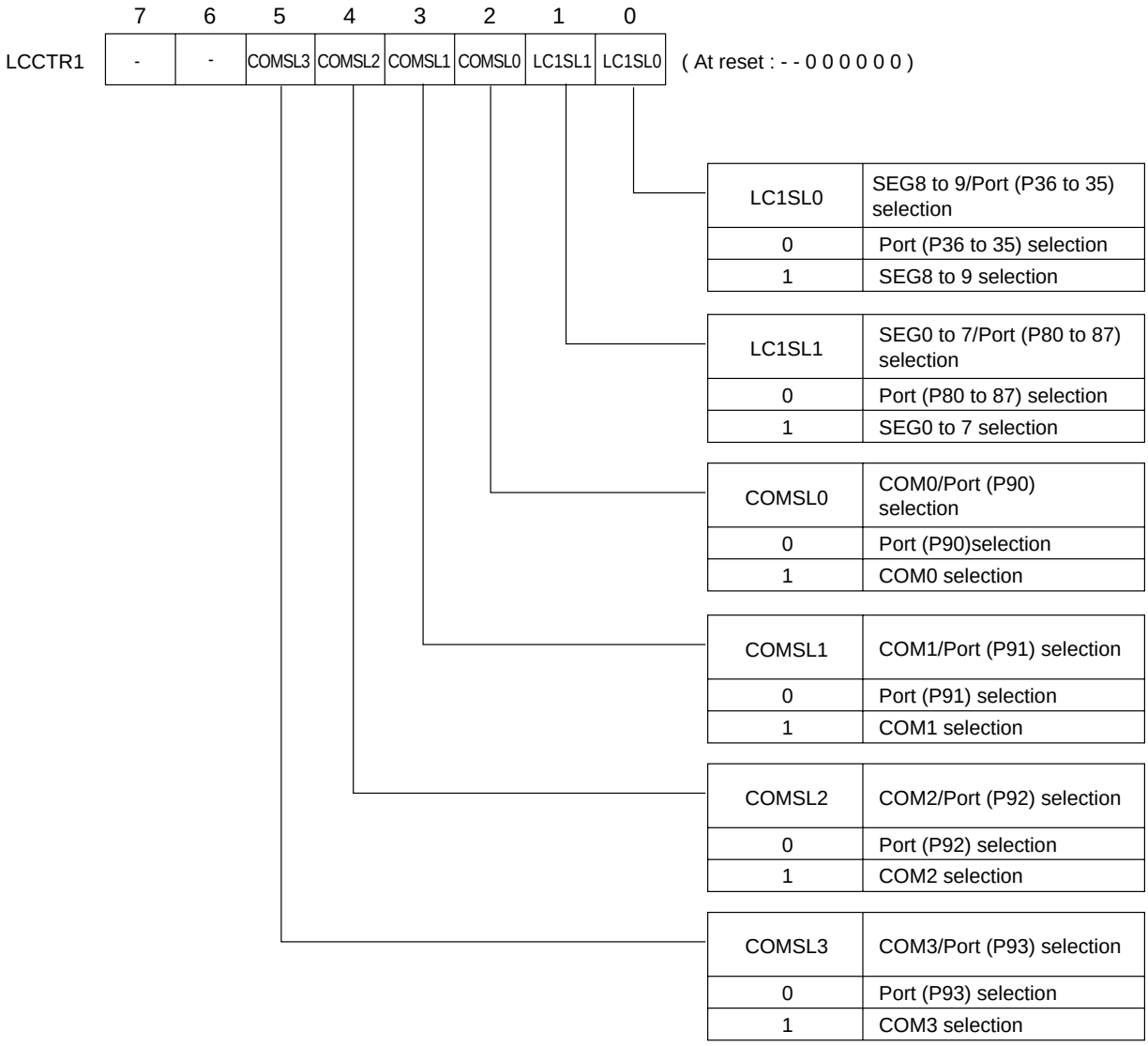
Port 8 direction control register (P8DIR : x'03F38', R/W)

	7	6	5	4	3	2	1	0	
P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	(At reset : 0 0 0 0 0 0 0 0)

P8PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 8 pull-up resistor control register (P8PLU : x'03F48', R/W)

Figure 4-10-1 Port 8 Registers (1/2)


7 6 5 4 3 2 1 0
LCCTR1
- - COMSL3 COMSL2 COMSL1 COMSL0 LC1SL1 LC1SL0
(At reset : - - 0 0 0 0 0 0)
LC1SL0 | SEG8 to 9/Port (P36 to 35) selection
0 | Port (P36 to 35) selection
1 | SEG8 to 9 selection
LC1SL1 | SEG0 to 7/Port (P80 to 87) selection
0 | Port (P80 to 87) selection
1 | SEG0 to 7 selection
COMSL0 | COM0/Port (P90) selection
0 | Port (P90)selection
1 | COM0 selection
COMSL1 | COM1/Port (P91) selection
0 | Port (P91) selection
1 | COM1 selection
COMSL2 | COM2/Port (P92) selection
0 | Port (P92) selection
1 | COM2 selection
COMSL3 | COM3/Port (P93) selection
0 | Port (P93) selection
1 | COM3 selection

LCD Control Register1 (LCCTR1 : X'03FDB', R/W)

Figure 4-10-2 Port 8 Registers (2/2)

4-10-3 Block Diagram

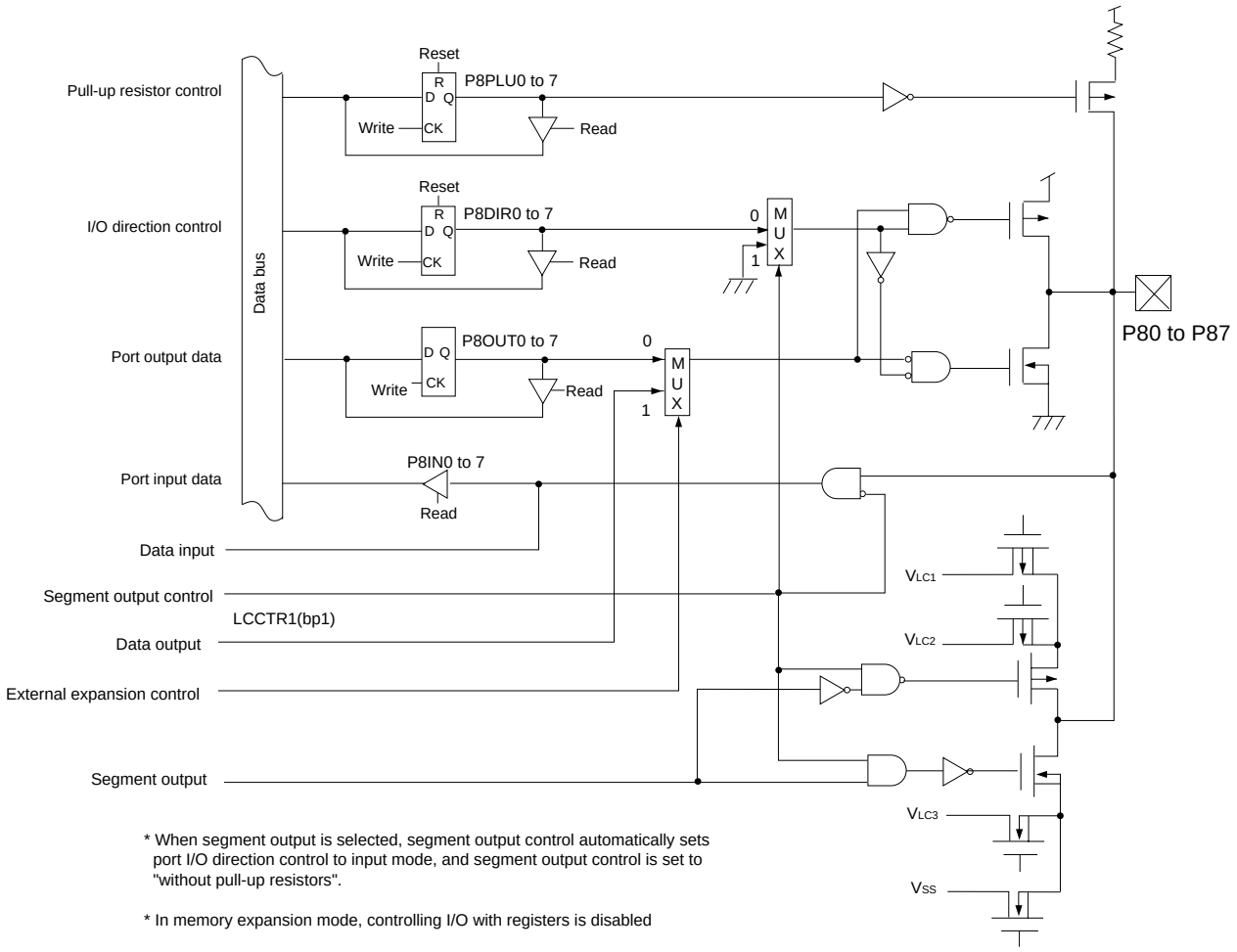


Figure 4-10-3 Block Diagram (P80 to P87)

4-11 Port 9

4-11-1 Description

■General Port Setup
Each bit can be set individually to either an input or output by the port 9 I/O direction control register (P9DIR). The control flag of the port 9 direction control register (P9DIR) is set to "1" for output mode, and "0" for input mode.

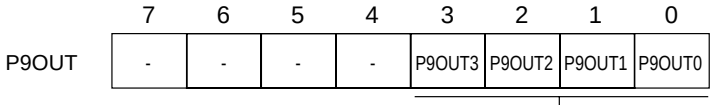
To read input data of pin, set the control flag of the port 9 direction control register (P9DIR) to "0" and read the value of the port 9 input register (P9IN).

To output data to pin, set the control flag of the port 9 direction control register (P9DIR) to "1" and write data to the port 9 output register (P9OUT).

Each bit can be set individually if pull-up resistor is added or not, by the port 9 pull-up resistor control register (P9PLU). Set the control flag of the port 9 pull-up resistor control register (P9PLU) to "1" to add pull-up resistor.

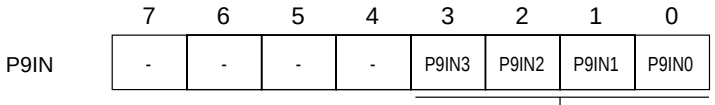
■Special Function Pin Setup
P90 to P93 can be used as the LCD Common output pins (COM0 to COM3). Set "1" to bit 2 to 5 (COMSL0 to 3) of the LCD output control register 1 (LCCTR1) to use these ports.
The ports and common can be switched by 1-bit. When common output is selected, input mode is set and the pull-up resistors are set off automatically.

4-11-2 Registers



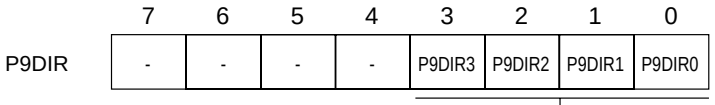
P9OUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port 9 output register (P9OUT : x'03F19', R/W)



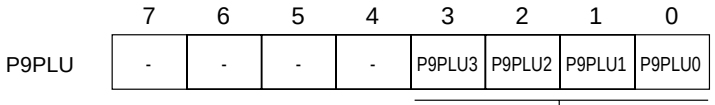
P9IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 9 input register (P9IN : x'03F29', R)



P9DIR	I/O mode selection
0	Input mode
1	Output mode

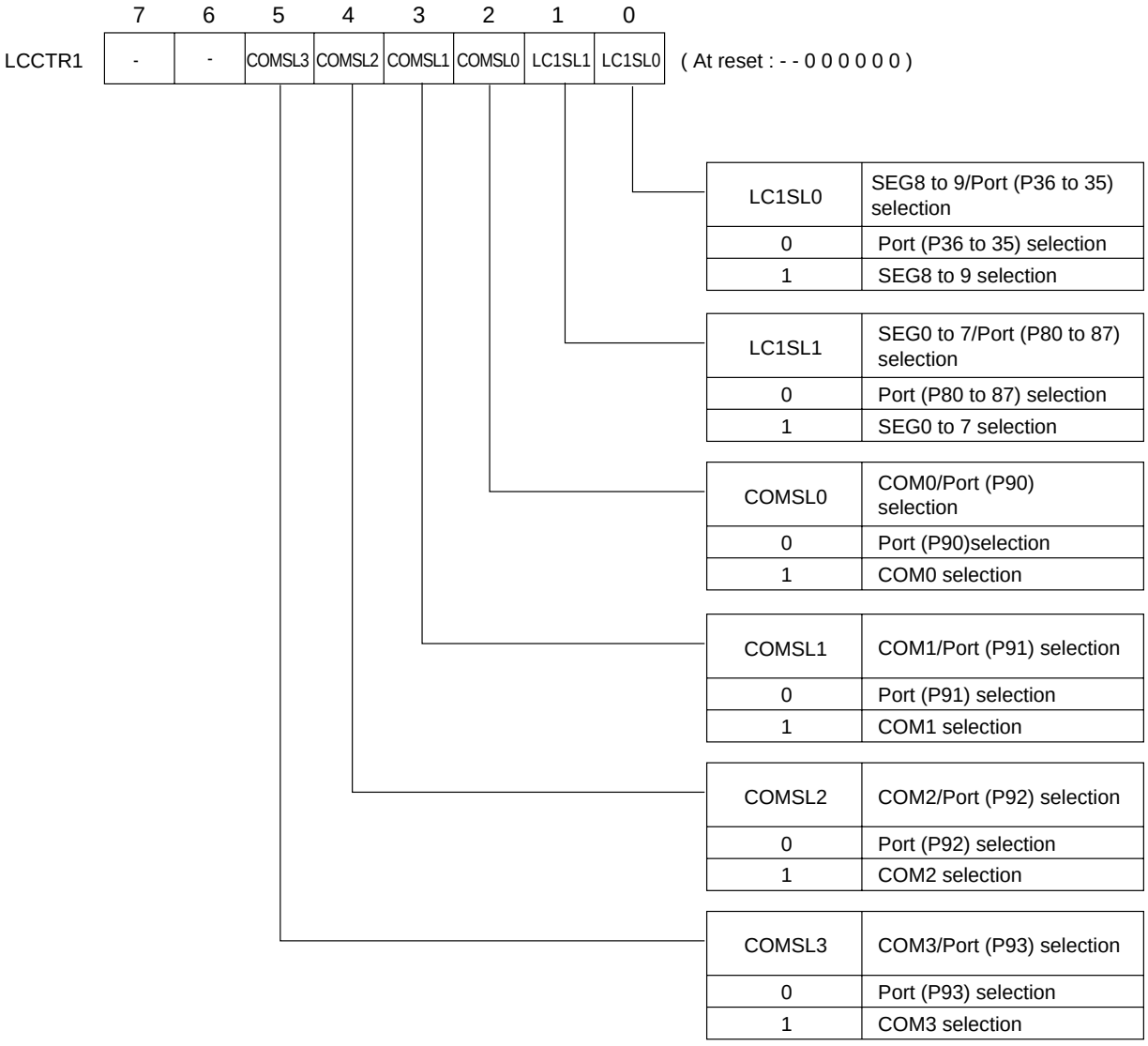
Port 9 direction control register (P9DIR : x'03F39', R/W)



P9PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 9 pull-up resistor control register (P9PLU : x'03F49', R/W)

Figure 4-11-1 Port 9 Registers (1/2)


7 6 5 4 3 2 1 0
LCCTR1
- - COMSL3 COMSL2 COMSL1 COMSL0 LC1SL1 LC1SL0
(At reset : - - 0 0 0 0 0 0)
LC1SL0 | SEG8 to 9/Port (P36 to 35) selection
0 | Port (P36 to 35) selection
1 | SEG8 to 9 selection
LC1SL1 | SEG0 to 7/Port (P80 to 87) selection
0 | Port (P80 to 87) selection
1 | SEG0 to 7 selection
COMSL0 | COM0/Port (P90) selection
0 | Port (P90)selection
1 | COM0 selection
COMSL1 | COM1/Port (P91) selection
0 | Port (P91) selection
1 | COM1 selection
COMSL2 | COM2/Port (P92) selection
0 | Port (P92) selection
1 | COM2 selection
COMSL3 | COM3/Port (P93) selection
0 | Port (P93) selection
1 | COM3 selection

LCD Control Register1 (LCCTR1 : X'03FDB', R/W)

Figure 4-11-2 Port 9 Registers (2/2)

4-11-3 Block Diagram

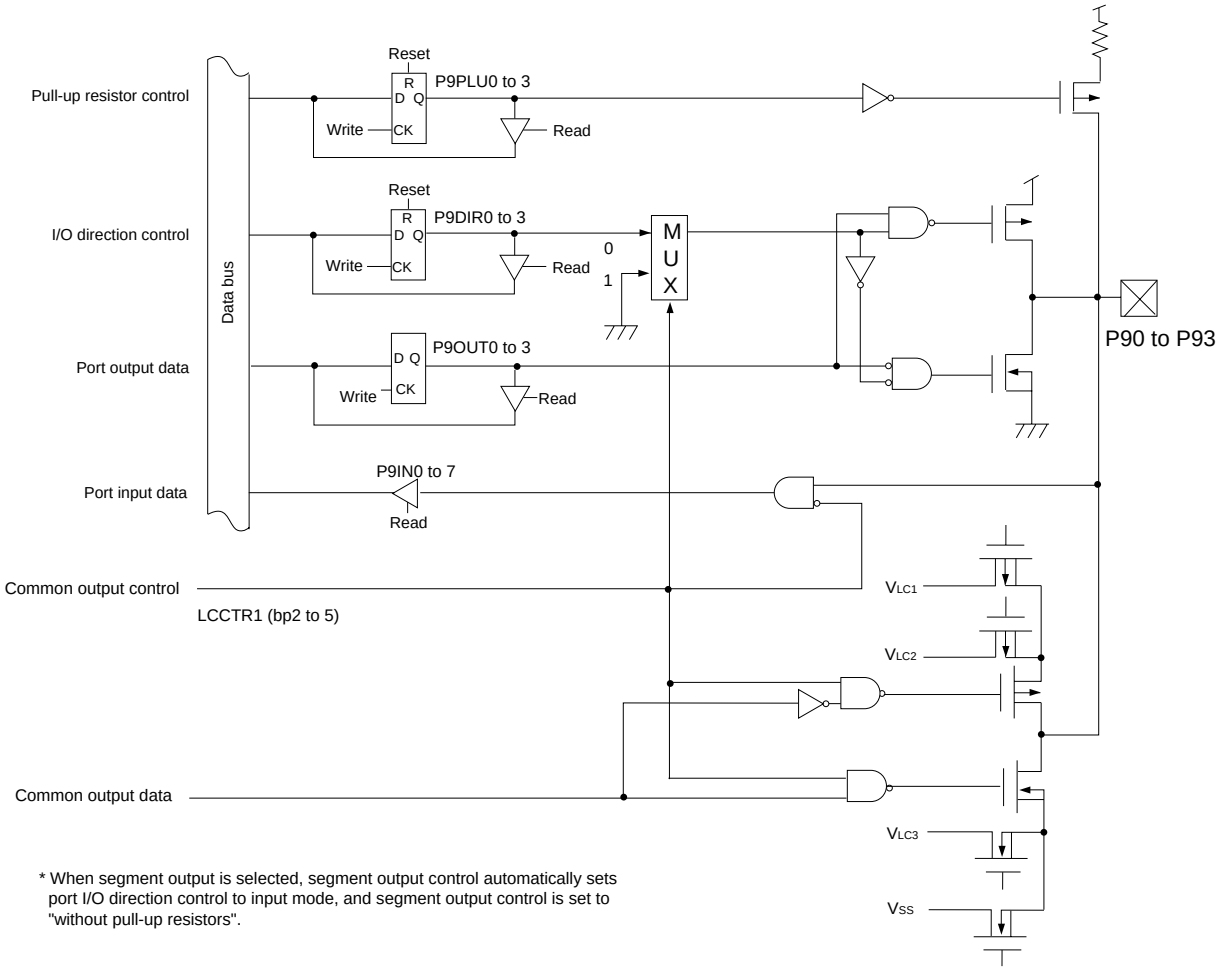


Figure 4-11-3 Block Diagram (P90 to P93)

4-12 Port A

4-12-1 Description

■General Port Setup

Each bit can be set individually to either an input or output by the port A control I/O direction register (PADIR). The control flag of the port A direction control register (PADIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port A direction control register (PADIR) to "0" and read the value of the port A input register (PAIN).

To output data to pin, set the control flag of the port A direction control register (PADIR) to "1" and write the value of the port A output register (PAOUT).

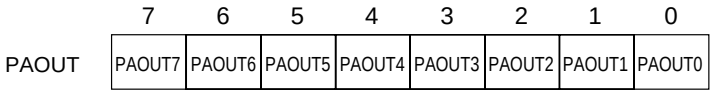
Each bit can be set individually if pull-up / pull-down resistor is added or not, by the port A pull-up / pull-down resistor control register (PAPLUD). Set the control flag of the port A pull-up / pull-down resistor control register (PAPLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp6 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

■Special Function Pin Setup

PA0 to PA7 are used as input pins for analog. Each bit can be set individually as an input by the port A input mode register (PAIMD). When they are used as analog input pins, set the port A input mode register (PAIMD) to "1". Then, the value of the port A input register (PAIN) is read to be "1".

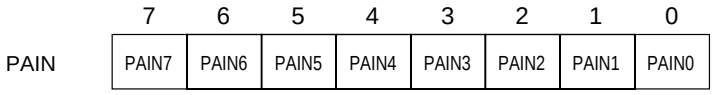
By setting the control flag of the PAIMD register to "1", the through current is not occurred when an analog voltage is set to pin,

4-12-2 Registers



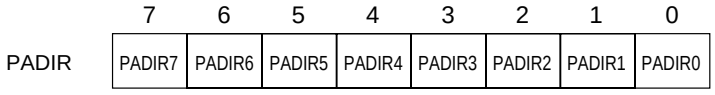
PAOUT	Output data
0	Low (VSS level) is output.
1	High (VDD level) is output.

Port A output register (PAOUT : x'03F1A', R/W)



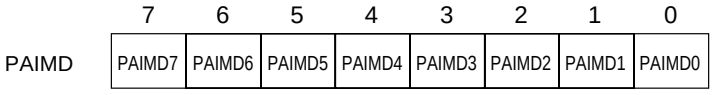
PAIN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port A input register (PAIN : x'03F2A', R)



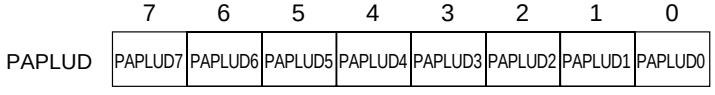
PADIR	I/O mode selection
0	Input mode
1	Output mode

Port A direction control register (PADIR : x'03F3A', R/W)



PAIMD	I/O port, analog input pin selection
0	I/O port
1	Analog input pin

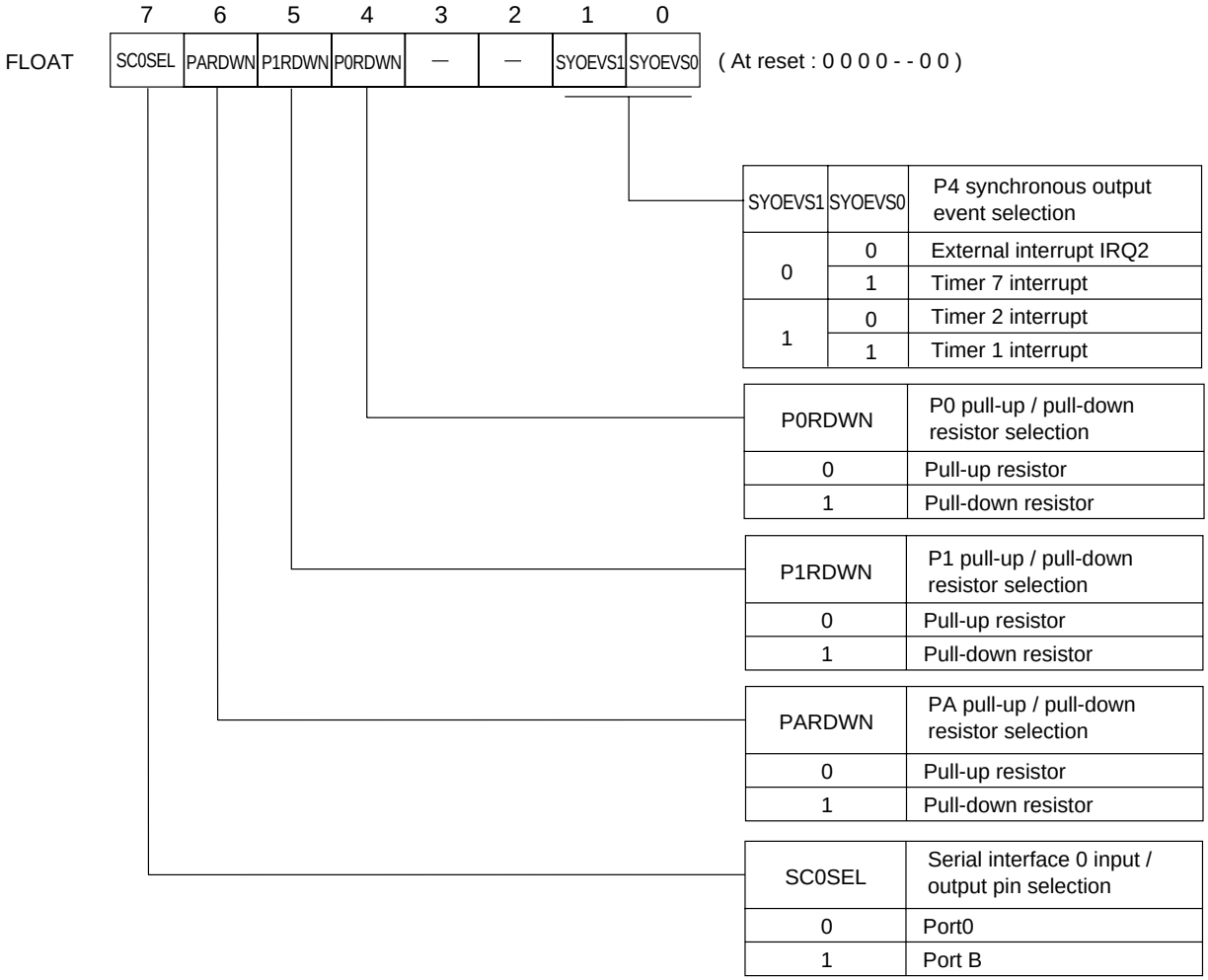
Port A input control register (PAIMD : x'03F3C', R/W)



PAPLUD	Pull-up (or Pull-down) resistor selection
0	No pull-up (or pull-down) resistor
1	Pull-up (or Pull-down) resistor

Port A pull-up / pull-down resistor control register (PAPLUD : x'03F4A', R/W)

Figure 4-12-1 Port A Registers (1/2)


7 6 5 4 3 2 1 0
FLOAT
SC0SEL PARDWN P1RDWN P0RDWN — — SYOEVS1 SYOEVS0
(At reset : 0 0 0 0 - - 0 0)
SYOEVS1 SYOEVS0 P4 synchronous output event selection
0 0 External interrupt IRQ2
1 Timer 7 interrupt
1 0 Timer 2 interrupt
1 Timer 1 interrupt
P0RDWN P0 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
P1RDWN P1 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
PARDWN PA pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
SC0SEL Serial interface 0 input / output pin selection
0 Port0
1 Port B

Pull-up / Pull-down resistor selection, Pin control register (FLOAT : x'03F2E', R/W)

Figure 4-12-2 Port A Registers (2/2)

4-12-3 Block Diagram

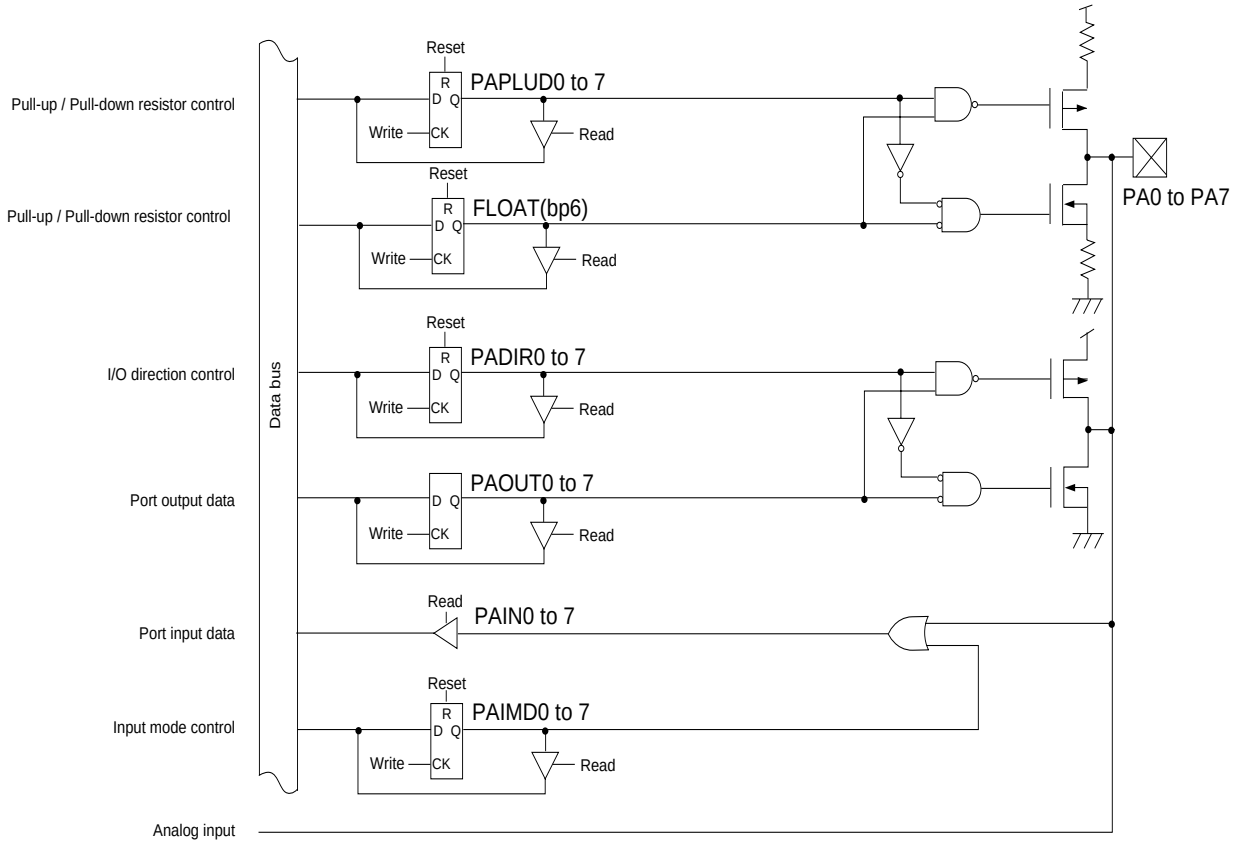


Figure 4-12-3 Block Diagram (PA0 to PA7)

4-13 Port B

4-13-1 Description

■General Port Setup

Each bit can be set individually as either an input or output by the port B control I/O direction register (PBDIR). The control flag of the port B direction control register (PBDIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port B direction control register (PBDIR) to "0" and read the value of the port B input register (PBIN).

To output data to pin, set the control flag of the port B direction control register (PBDIR) to "1" and write the value of the port B output register (PBOUT).

Each bit can be set individually if pull-up / pull-down resistor is added or not, by the port B pull-up / pull-down resistor control register (PBPLU). Set the control flag of the port B pull-up / pull-down resistor control register (PBPLU) to "1" to add pull-up or pull-down resistor.

■Special Function Pin Setup

PB0 to PB7 are used as LCD segment output pins. To use these ports as SEG46 to SEG39 pins, set "1" to bit 0 to 7 (LC4SL0 to LC4SL7) of the LCD control register 4 (LCCTR4). The ports and the segments can be switched by 1-bit. When segment output is selected, input mode is set and the pull-up resistors are set off automatically.

PB to PB7 are used as analog input pins and can be set to input mode by 1-bit with port B input mode register (PBIMD). To use them as analog input pins set "1" to the port B input mode register (PBIMD), and then the value of the port B input register (PBIN) read out is "1".

PB5 to PB7 are used as serial interface 0 transmission data output pins. PB5 is serial interface 0 transmission data output pin and outputs the serial data when SC0SBOS flag of the mode register 1 (SC0MD1) is "1" .

PB6 is input pin of serial interface 0 and the reception data.

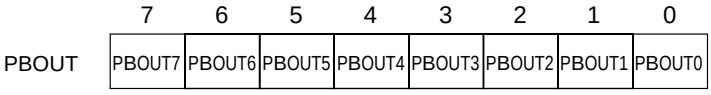
PB7 is serial interface 0 clock I/O pin and outputs the serial clock when SC0SBTS flag of the mode register 1 (SC0MD1) is "1" .

Serial interface 0 port control register (SC0ODC) sets PB5 and PB6 to be either push-pull output or Nch open-drain output.

Also serial 0 I/O pins are assigned to either P00 to P02 or PB5 to PB7 by setting SC0SEL (FLOAT).

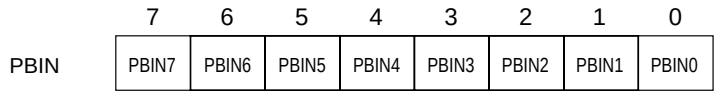
By setting the control flag of the PBIMD register to "1", the through current is not occurred when an analog voltage is set to pin,

4-13-2 Registers



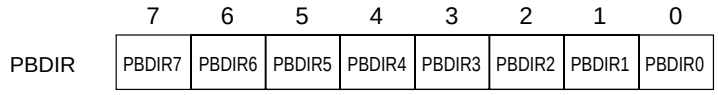
PBOUT	Output data
0	Low (V_{SS} level) is output.
1	High (V_{DD} level) is output.

Port B output register (PBOUT : x'03F1B', R/W)



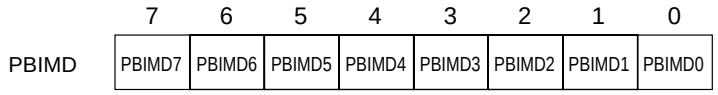
PBIN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port B input register (PBIN : x'03F2B', R)



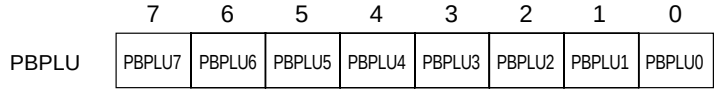
PBDIR	I/O mode selection
0	Input mode
1	Output mode

Port B direction control register (PBDIR : x'03F3B', R/W)



PBIMD	I/O port, analog input pin selection
0	I/O port
1	Analog input pin

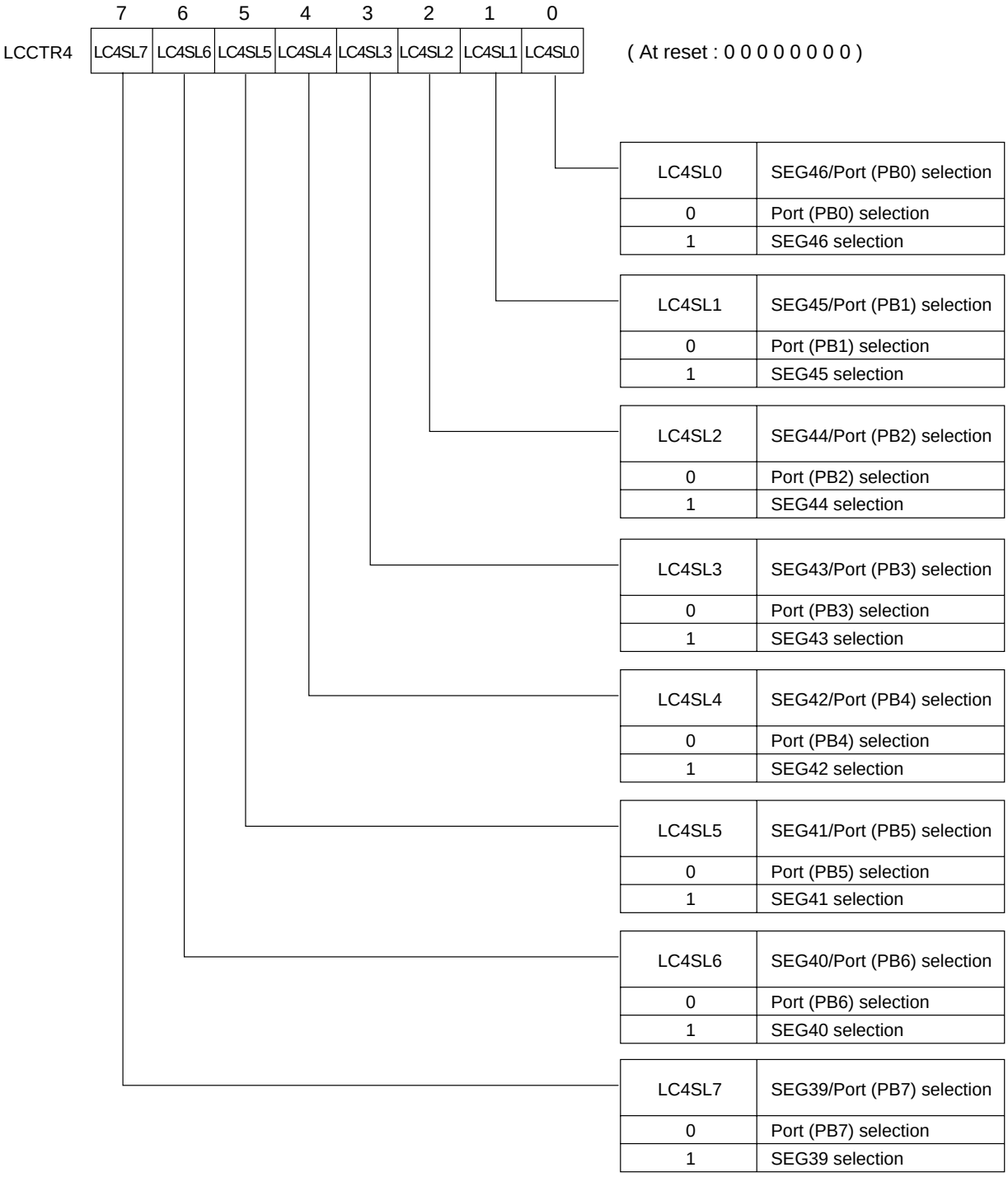
Port B input control register (PBIMD : x'03F3D', R/W)



PBPLU	Pull-up (or Pull-down) resistor selection
0	No pull-up (or pull-down) resistor
1	Pull-up (or Pull-down) resistor

Port B pull-up / pull-down resistor control register (PBPLU : x'03F4B', R/W)

Figure 4-13-1 Port B Registers (1/2)


7 6 5 4 3 2 1 0
LCCTR4
LC4SL7 LC4SL6 LC4SL5 LC4SL4 LC4SL3 LC4SL2 LC4SL1 LC4SL0
(At reset : 0 0 0 0 0 0 0 0)
LC4SL0 SEG46/Port (PB0) selection
0 Port (PB0) selection
1 SEG46 selection
LC4SL1 SEG45/Port (PB1) selection
0 Port (PB1) selection
1 SEG45 selection
LC4SL2 SEG44/Port (PB2) selection
0 Port (PB2) selection
1 SEG44 selection
LC4SL3 SEG43/Port (PB3) selection
0 Port (PB3) selection
1 SEG43 selection
LC4SL4 SEG42/Port (PB4) selection
0 Port (PB4) selection
1 SEG42 selection
LC4SL5 SEG41/Port (PB5) selection
0 Port (PB5) selection
1 SEG41 selection
LC4SL6 SEG40/Port (PB6) selection
0 Port (PB6) selection
1 SEG40 selection
LC4SL7 SEG39/Port (PB7) selection
0 Port (PB7) selection
1 SEG39 selection

LCD Control Register4 (LCCTR4 : X'03FDE', R/W)

Figure 4-13-2 Port B Registers (2/2)

4-13-3 Block Diagram

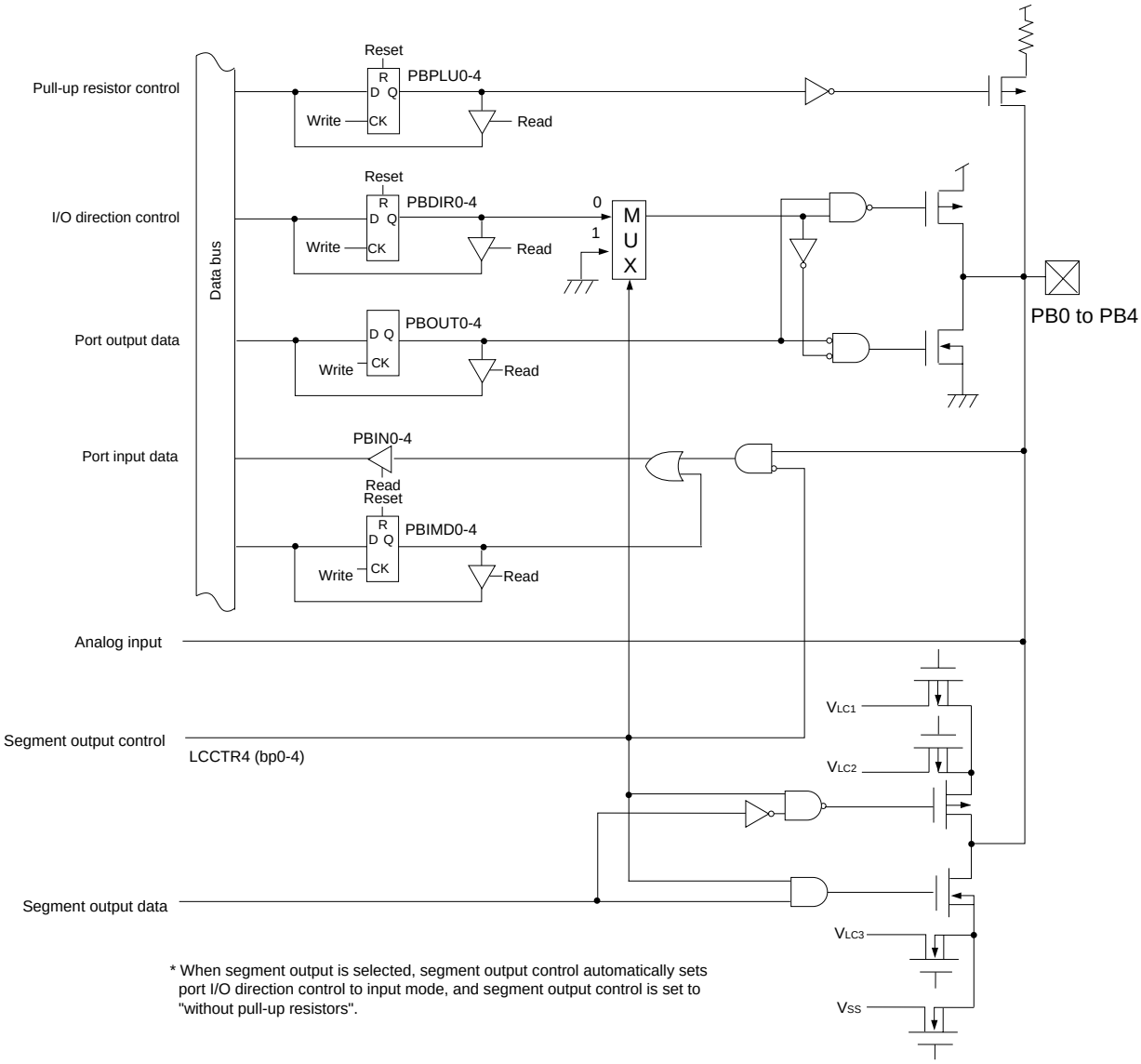


Figure 4-13-3 Block Diagram (PB0 to PB4)

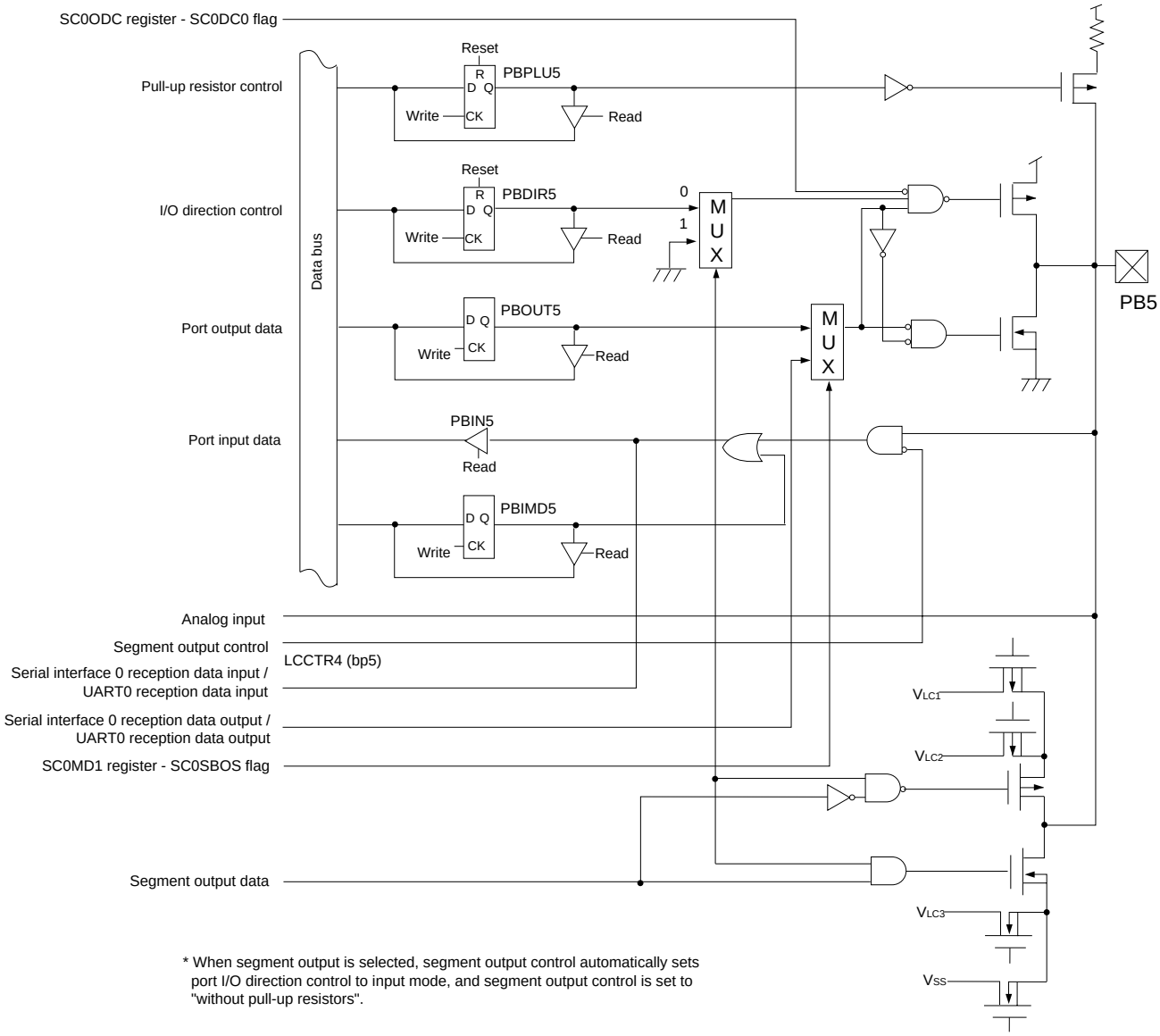


Figure 4-13-4 Block Diagram (PB5)

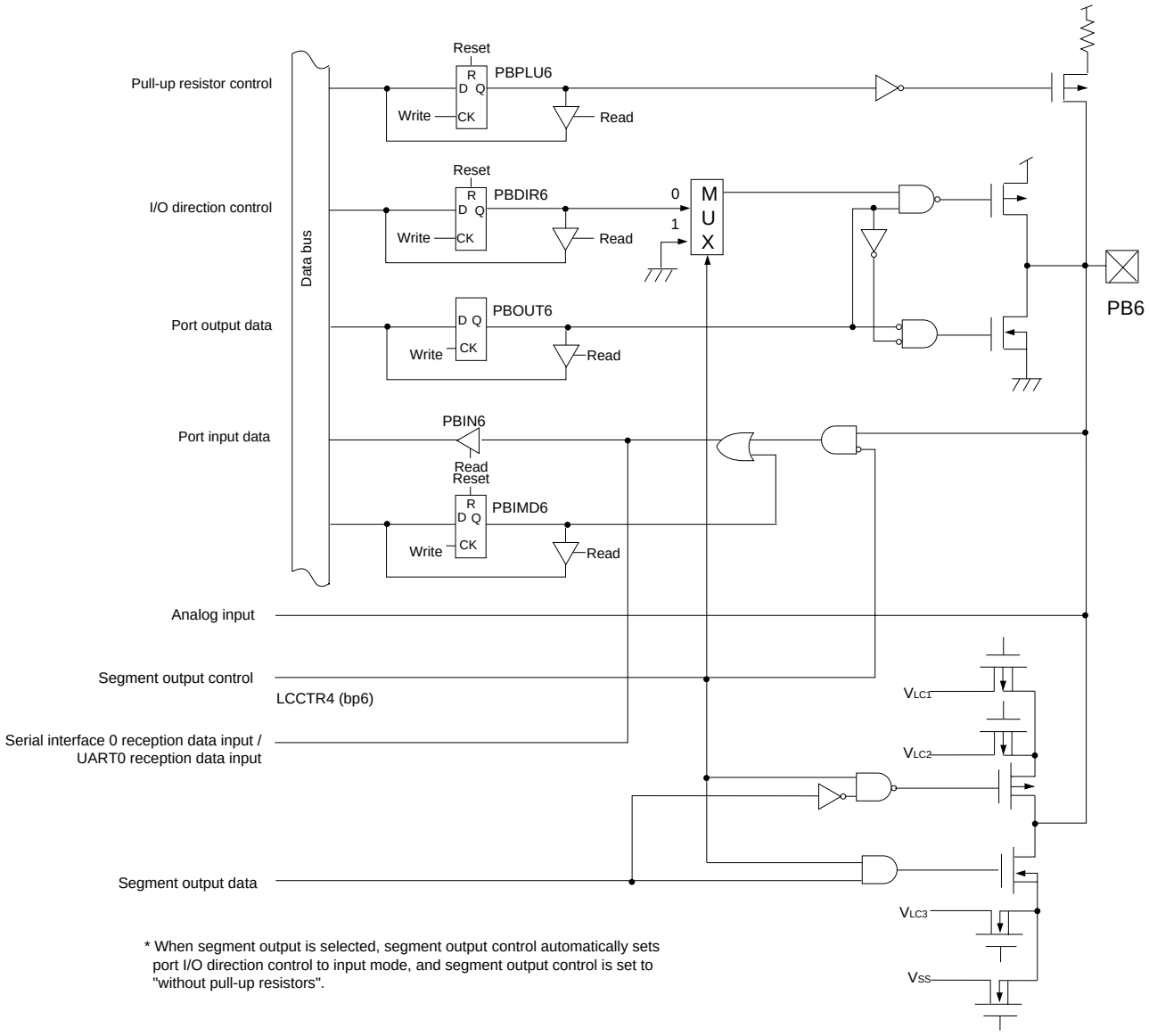


Figure 4-13-5 Block Diagram (PB6)

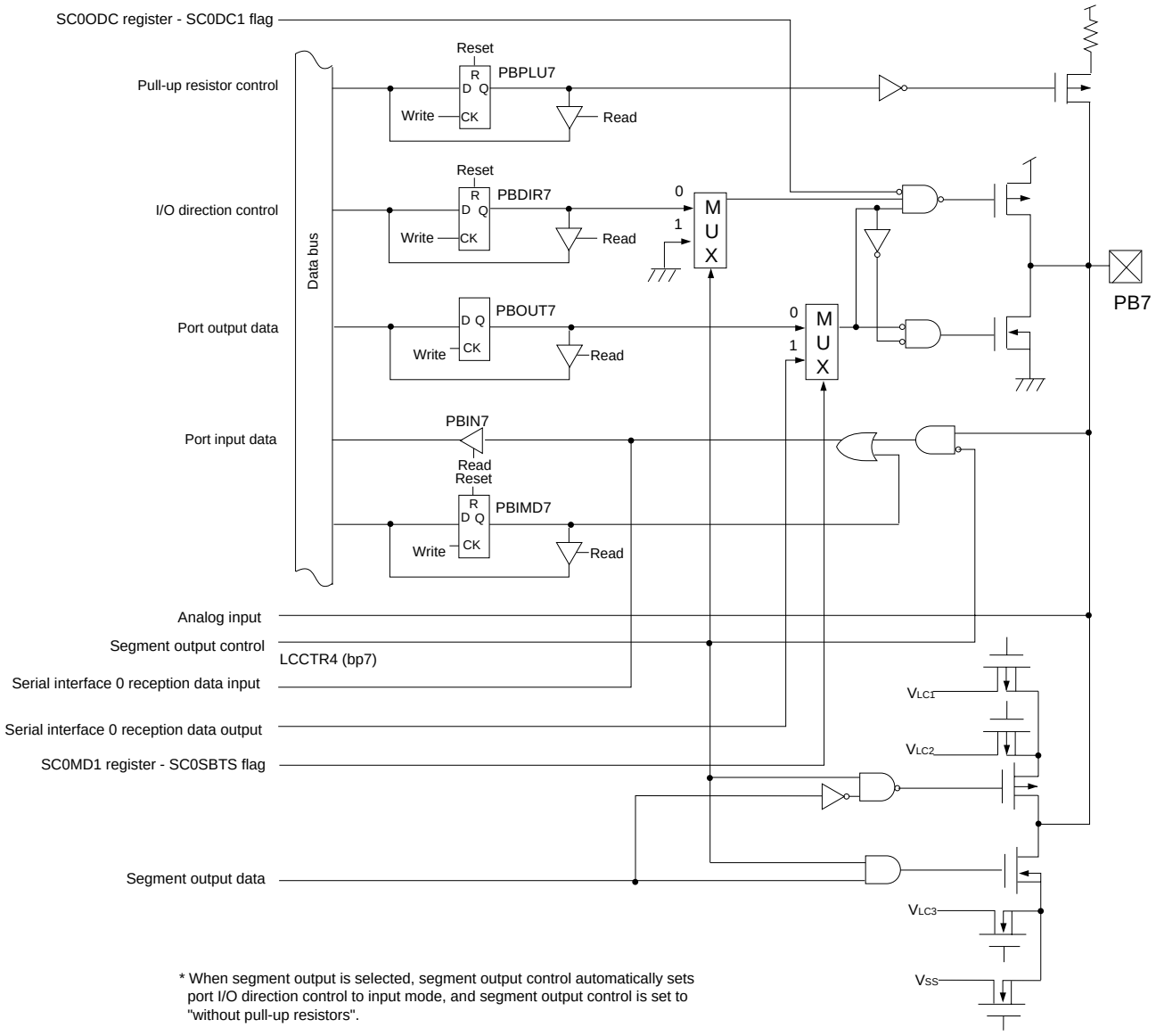


Figure 4-13-6 Block Diagram (PB7)

4-14 Synchronous output (Port 4)

Port 4 has the synchronous output function that outputs the arbitrary set data to pins, in synchronization with the generation of the specified event, without setting program. Synchronous event is selected from the external interrupt 2 (P22/IRQ2), timer 1 interrupt, timer 2 interrupt or timer 7 interrupt signal.

4-14-1 Block Diagram

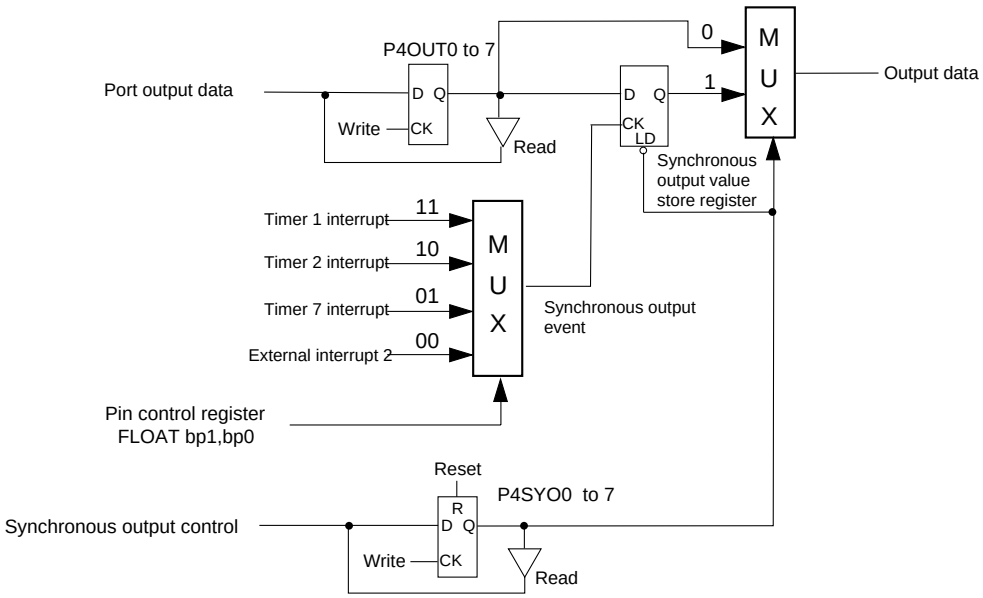


Figure 4-14-1 Synchronous Output Control Block Diagram

4-14-2 Registers

Table 4-14-1 shows the synchronous output control registers of port 4.

Table 4-14-1 Synchronous Output Control Registers

	Register	Address	R/W	Function	Page
Port 4	FLOAT	x'03F2E'	R/W	Pin control register 1	Ⅳ - 8,16,31,59, Ⅺ - 8
	P4SYO	x'03F1E'	R/W	Synchronous output control register	Ⅳ - 31
	P4DIR	x'03F34'	R/W	Port 4 direction control register	Ⅳ - 30
	P4PLU	x'03F44'	R/W	Port 4 Pull-up control register	Ⅳ - 30
	P4OUT	x'03F14'	R/W	Port 4 output register	Ⅳ - 30

R/W : Readable/Writable

4-14-3 Operation

■Synchronous Output Setup

The synchronous output control register (P4SYO) selects the synchronous output pin of the port 4, in each bit.

The synchronous output event is selected by the pin control register (FLOAT).

Table 4-14-2 Synchronous Output Event

	Specify to	Page
Synchronous output port	Port 4	Ⅳ - 27
Output event	External interrupt 2 (IRQ2)	Ⅲ - 19, 38
	Timer 1	Ⅵ - 32
	Timer 2	Ⅵ - 32
	Timer7	Ⅶ - 55

When the external interrupt 2 (IRQ2) is selected, the interrupt edge should be specified. The interrupt edge can be specified by the external interrupt 2 control register (IRQ2ICR) or the both edges interrupt control register (EDGDT). The synchronous output recognizes the generation of the specified edge as an event.

■Synchronous Output Operation

When the synchronous output control register (P4SYO) is set to disable the synchronous output (I/O port), the port 4 is functioned as a general port. When the port 4 is set to disable the synchronous output, the same value to the port 4 output register (P4OUT) is always loaded to the synchronous output value stored register. [☞ Figure 4-12-1. Synchronous Output Control Block Diagram]

After the output mode is selected by the port 4 direction control register (P4DIR), if the synchronous output is enabled by the synchronous output control register (P4SYO), the value of the synchronous output value stored register is output from pins. If the synchronous output event that is set by the pin control register (FLOAT) is never generated, the synchronous output value stored register holds the same value when the synchronous output event is enabled.

Store the value that should be output from pin after the synchronous output event is generated, to the port 4 output register (P4OUT). Once the synchronous output event that is set by the pin control register (FLOAT) is generated, the data of the synchronous output value stored register is switched to the data of the port 4 output register (P4OUT), and the output value from pin is changed.

Before the synchronous output is enabled by the synchronous output control register (P4SYO), set the initial value of the synchronous output to the port 4 output register (P4OUT), in advance.

■Port 4 Synchronous Output (External interrupt 2 IRQ2))

The synchronous output timing when the synchronous output event is set at the falling edge of the external interrupt 2, is shown below. The latched data on port 4 is output in synchronization with the falling edge of the IRQ2.

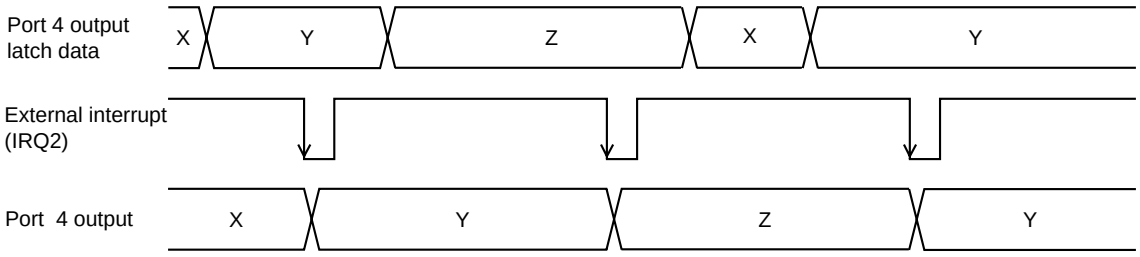


Figure 4-14-2 Synchronous Output Timing by Event Generation (IRQ2)

■Port 4 Synchronous Output (Timer 1, Timer 2, Timer 7)

The timer interrupt flag TMnIRQ is generated when the set values of binary counter and compare register are matched. The latched data on port 4 is output from the port 4 in synchronization with the rising edge of the TMnIRQ. About the setting of each timer operation, refer to chapter 6. 8-bit timers, and chapter 7. 16-bit timers.

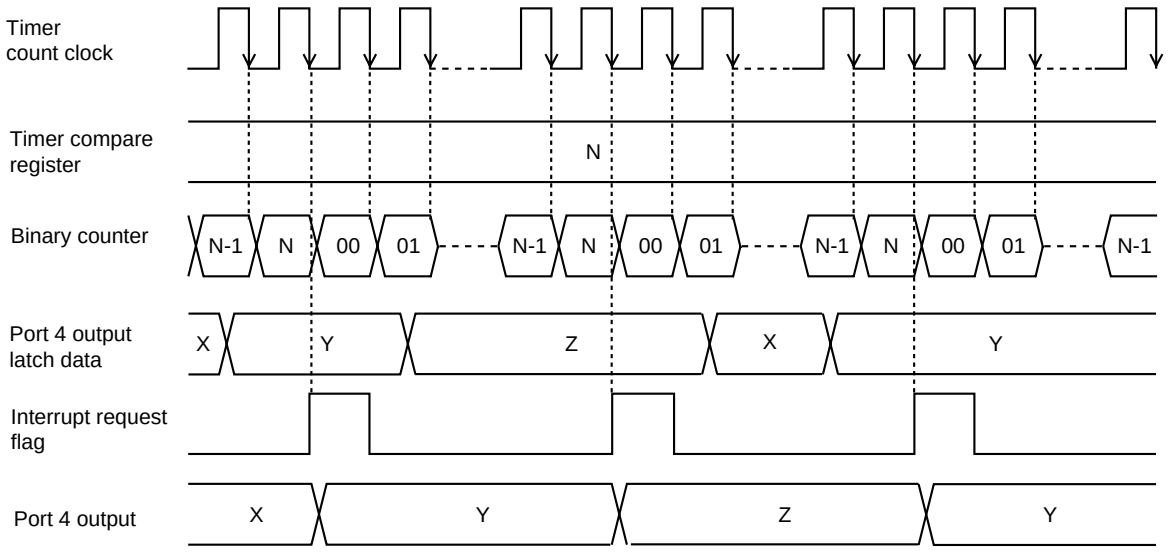


Figure 4-14-3 Synchronous Output Timing by Event Generation (Timers 1, 2 and 7)

4-14-4 Setup Example

A setup example of the port 4 synchronous output by the external interrupt 2 (IRQ2) is shown as follows. As it is operated, the initial output data of port 4 is "55", the synchronous output data is "AA", and the rising edge of the IRQ2 is selected at the synchronous event.

An example setup procedure, with description of each step is shown below.

Setup Procedure	Description
(1) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 :SYOEVS1-0 = 00	(1) Set the SYOEVS1-0 flag of the FLOAT register to "00" to set the synchronous output event to the IRQ2.
(2) Specify the interrupt edge. IRQ2ICR(x'3FE4') bp5 : REDG2 = 1 EDGDT(x'3F8F') bp2 : EDGSEL2 = 0	(2) Set the REDG flag of the IRQ2ICR register to "1" to set the active edge of the IRQ2 at the rising edge. Set the EDGSEL2 flag of the EDGDT register "0" to select the programmable active edge interrupt.
(3) Set the initial output data. P4OUT(x'3F14') bp7-0 : P4OUT7-0 = x'55'	(3) Set the initial output data "55" to the P4OUT register. Port 4 outputs "55".
(4) Set the synchronous output pin. P4SYO(x'3F1E') bp7-0 : P4SYO7-0 = x'FF' P4DIR(x'3F34') bp7-0 : P4DIR7-0 = x'FF'	(4) Set port 4 to synchronous output pin by setting the P4SYO7-0 flag of the P4SYO register to "FF". Select the output mode by setting the P4DIR7-0 flag of the P4DIR register to "FF".
(5) Set the synchronous output data. P4OUT(x'3F14') bp7-0 : P4OUT7-0 = x'AA'	(5) Set the synchronous output data "AA" to the P4OUT register.
(6) Event is generated. Rising edge is generated at P22.	(6) Port 4 outputs "AA" at the rising edge of IRQ2.

Chapter 5 Prescaler

5

5-1 Overview

This LSI contains 2 prescalers that are used among the peripheral functions simultaneously. Each prescaler counts with fosc or fs as a base clock. The hardware is as follows ;

Prescaler 0 (fosc base)	15-bit prescaler
Prescaler 1 (fs base)	3-bit prescaler

Prescaler 0 outputs fosc/2, fosc/4, fosc/16, fosc/32, fosc/64, fosc/128, fosc/2^{9}, fosc/2^{10}, fosc/2^{11}, fosc/2^{12}, fosc/2^{13}, fosc/2^{15} as cycle clock. Prescaler 1 outputs fs/2, fs/4, fs/8 as cycle clock.
Use the prescalers when cycle clock based on fosc and fs is used on the following peripheral functions ;

External interrupt 0 interface (with noise filter)
External interrupt 1 interface (with noise filter)
Timer 0 (8-bit timer counter)
Timer 1 (8-bit timer counter)
Timer 2 (8-bit timer counter)
Timer 3 (8-bit timer counter)
Serial 0 (Clock synchronous / Duplex UART)
Serial 2 (Clock synchronous)
Remote control (with fosc clock)

Refer to chapter 2. 2-5 Clock Switching [p.II-28] for fosc and fs.

5-1-1 Peripheral Functions

Table 5-1-1 shows the selectable clock sources used in each peripheral functions used with prescaler block output.

Table 5-1-1 Peripheral Functions Used with Prescaler Output

Clock source selection	Peripheral Functions								
	External interrupt 0	External interrupt 1	Timer 0	Timer 1	Timer 2	Timer 3	Serial interface 0	Serial interface 2	Remote control
fosc/2	-	-	-	-	-	-	√	√	-
fosc/4	-	-	√	√	√	√	√	√	-
fosc/16	-	-	√	√	√	√	√	√	-
fosc/32	√	-	√	-	√	-	-	√	-
fosc/64	-	-	√	-	√	√	√	-	-
fosc/128	√	√	-	-	-	√	-	-	-
$fosc/2^9$	-	-	-	-	-	-	-	-	√
$fosc/2^{10}$	-	-	-	-	-	-	-	-	√
$fosc/2^{11}$	-	-	-	-	-	-	-	-	√
$fosc/2^{12}$	-	-	-	-	-	-	-	-	√
$fosc/2^{13}$	-	-	-	√	-	-	-	-	-
$fosc/2^{15}$	-	-	-	√	-	-	-	-	-
fs/2	-	-	√	√	√	√	√	√	-
fs/4	-	-	√	-	√	-	√	√	-
fs/8	-	-	-	√	-	√	-	-	-
Timer 3 output	-	-	-	-	-	-	√	√	-

5-1-2 Block Diagram

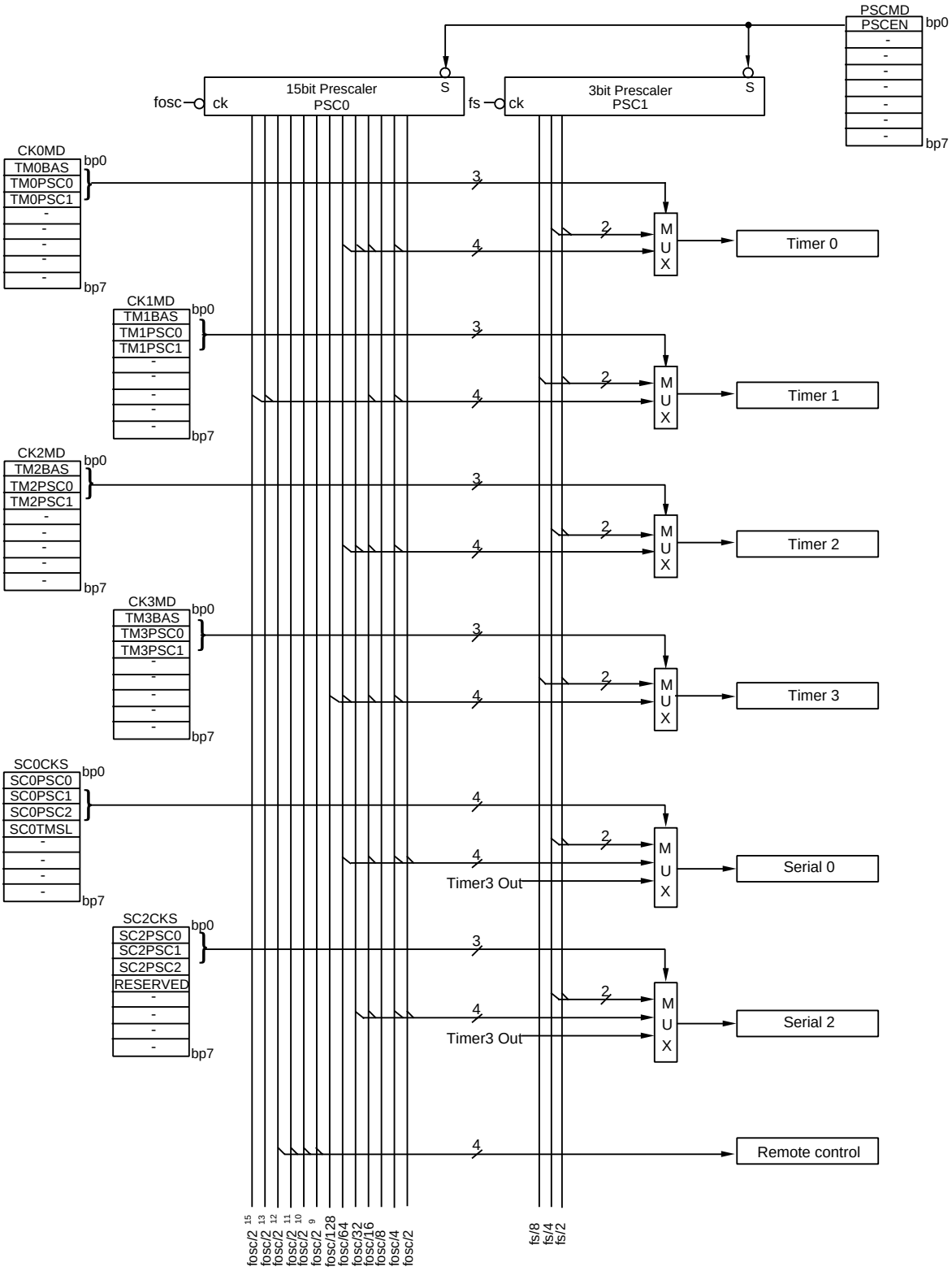


Figure 5-1-1 Prescaler Block Diagram

5-2 Control Registers

5-2-1 Registers List

Table 5-2-1 shows registers control prescaler.

Table 5-2-1 Prescaler Control Registers

Register	Address	R/W	Function	Page
PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
CK0MD	x'03F56'	R/W	Timer 0 prescaler selection register	V-7
CK1MD	x'03F57'	R/W	Timer 1 prescaler selection register	V-7
CK2MD	x'03F5E'	R/W	Timer 2 prescaler selection register	V-8
CK3MD	x'03F5F'	R/W	Timer 3 prescaler selection register	V-8
SC0CKS	x'03F97'	R/W	Serial 0 transfer clock selection register	V-9, XI-12
SC2CKS	x'03FA7'	R/W	Serial 2 transfer clock selection register	V-9, XII-8

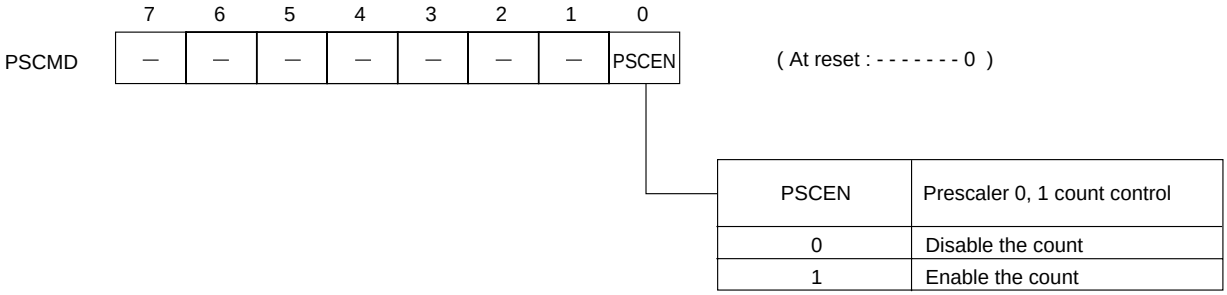
R/W : Readable/Writable

5-2-2 Control Registers

There are three types of Prescaler control registers; the register controls prescaler operation is the prescaler control register (PSCMD), and the register select prescaler output are the timer prescaler selection register (CKnMD) and the serial interface transfer clock selection register (SCnCKS).

The prescaler control register controls prescaler count operation

■Prescaler Control Register (PSCMD)



PSCEN	Prescaler 0, 1 count control
0	Disable the count
1	Enable the count

Figure 5-2-1 Prescaler Control Register (PSCMD : x'03F6F', R/W)

Select the clock for the remote control function with the RMCTR1 register.
[☞ Chapter 15-2-1. Remote Control Registers]

The timer prescaler selection register selects the count clock used for 8-bit timer.

■Timer 0 Prescaler Selection Register (CK0MD)

	7	6	5	4	3	2	1	0	
CK0MD	—	—	—	—	—	TM0PSC1	TM0PSC0	TM0BAS	(At reset : - - - - - X X X)

TM0PSC1	TM0PSC0	TM0BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/64
-	0	1	fs/2
	1		fs/4

Figure 5-2-2 Timer 0 Prescaler Selection Register (CK0MD : x'03F56', R/W)

■Timer 1 prescaler selection register (CK1MD)

	7	6	5	4	3	2	1	0	
CK1MD	—	—	—	—	—	TM1PSC1	TM1PSC0	TM1BAS	(At reset : - - - - - X X X)

TM1PSC1	TM1PSC0	TM1BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/2^{13}
	1		fosc/2^{15}
-	0	1	fs/2
	1		fs/8

Figure 5-2-3 Timer 1 Prescaler Selection Register (CK1MD : x'03F57', R/W)

■Timer 2 Prescaler Selection Register (CK2MD)

	7	6	5	4	3	2	1	0	
CK2MD	—	—	—	—	—	TM2PSC1	TM2PSC0	TM2BAS	(At reset : - - - - - X X X)

TM2PSC1	TM2PSC0	TM2BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/64
-	0	1	fs/2
	1		fs/4

Figure 5-2-4 Timer 2 Prescaler Selection Register (CK2MD : x'03F5E', R/W)

■Timer 3 Prescaler Selection Register (CK3MD)

	7	6	5	4	3	2	1	0	
CK3MD	—	—	—	—	—	TM3PSC1	TM3PSC0	TM3BAS	(At reset : - - - - - X X X)

TM3PSC1	TM3PSC0	TM3BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/64
	1		fosc/128
-	0	1	fs/2
	1		fs/8

Figure 5-2-5 Timer 3 Prescaler Selection Register (CK3MD : x'03F5F', R/W)

The serial interface transfer clock selection register (SCnCKS) selects the transfer clock used for serial interface transfer.

■Serial Interface 0 Transfer Clock Selection Register (SC0CKS)

	7	6	5	4	3	2	1	0
SC0CKS	—	—	—	—	SC0TMSEL	SC0PSC2	SC0PSC1	SC0PSC0

(At reset : - - - - X X X X)

SC0TMSEL	SC0PSC2	SC0PSC1	SC0PSC0	Clock source selection
-	0	0	0	fosc/2
			1	fosc/4
		1	0	fosc/16
			1	fosc/64
	1	0	0	fs/2
			1	fs/4
0		1	0	Disable
			1	Timer 3 output
1			0	Disable
			1	Disable

Figure 5-2-6 Serial Interface 0 Transfer Clock Selection Register (SC0CKS : x'03F97', R/W)

■Serial Interface 2 Transfer Clock Selection Register (SC2CKS)

	7	6	5	4	3	2	1	0
SC2CKS	—	—	—	—	Reserved	SC2PSC2	SC2PSC1	SC2PSC0

(At reset : - - - - X X X X)

SC2PSC2	SC2PSC1	SC2PSC0	Clock source selection
0	0	0	fosc/2
		1	fosc/4
	1	0	fosc/16
		1	fosc/32
1	0	0	fs/2
		1	fs/4
	1		Timer 3 output

Reserved	When serial interface 2 is used set always to "0".

Figure 5-2-7 Serial Interface 2 Transfer Clock Selection Register (SC2CKS : x'03FA7', R/W)

5-3 Operation

5-3-1 Operation

■Prescaler Operation (Prescalers 0 and 1)
Prescaler 0 and prescaler 1 are 15-bit, 3-bit free running counter that divide the base clock. The PSCEN flag of the prescaler control register (PSCMD) starts or stops the count up operation.

■Count Timing of Prescaler Operation (Prescalers 0 and 1)
Prescaler 0 counts up at the falling edge of fosc.
Prescaler 1 counts up at the falling edge of fs.

■Peripheral Functions with Prescaler Output Cycle Clock
Table 5-3-1 shows the peripheral functions that are capable of using prescaler output clock as a clock source, and the control registers that select the clock source..

Table 5-3-1 Peripheral Functions Used with Prescaler Output Cycle Clock

Peripheral functions		Control register
External interrupt 0	Noise filter sampling clock	-
External interrupt 1	Noise filter sampling clock	-
Timer 0	Count clock	CK0MD
Timer 1	Count clock	CK1MD
Timer 2	Count clock	CK2MD
Timer 3	Count clock	CK3MD
Serial interface 0	Transfer clock	SC0CKS
Serial interface 2	Transfer clock	SC2CKS
Remote control	Sampling clock	RMCTR1

When the prescaler output clock source is used, counting of prescaler should be enabled before starting the peripheral functions.

When the sampling clock for the remote control function is based on fx, remote control function can be used even if the prescaler count operation is disabled.

5-3-2 Setup Example

■Prescaler Setup Example (Timer 0 count clock)
Select the clock of fosc/16 output from the prescaler 0, for the count clock of the timer 0.
Example of the setup procedure is shown below.

Setup Procedure	Description
(1) Select the prescaler output. CK0MD (x'3F56') bp2-1 : TM0PSC1-0 = 01 bp0 : TM0BAS = 0 (2) Enable the prescaler output. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Select the prescaler output to fosc/16 by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). (2) Enable the prescaler counting by setting the PSCEN flag of the prescaler control register (PSCMD) to "1".

Enable the prescaler counting by the PSCEN flag of the prescaler control register (PSCMD). The prescaler counting is started after it is enabled.
Start the timer operation after the prescaler is set. Also, the selection of the prescaler output should be set by the timer mode register.

Chapter 6 8-bit Timers

6

6-1 Overview

This LSI contains four general purpose 8-bit timers (Timers 0, 1, 2 and 3). The general purpose 8-bit timers are configured in pairs so that they can be used as 16-bit timers with cascade connection. In a cascade connecion, timers 0, and 2 form the "timer 0", or the lower 8 bits of 16-bit counter, and timers 1 and 3 form the "timer 1", or the upper 8 bits.

Fosc or fs can be selected as the clock source for each timer by using the prescaler. Also, remote control output circuit is built in.

6-1-1 Functions

Table 6-1-1 shows functions that can be used with each timer.

Table 6-1-1 Timer Functions

	Timer 0 (8 bit)	Timer 1 (8 bit)	Timer 2 (8 bit)	Timer 3 (8 bit)
Interrupt source	TM0IRQ	TM1IRQ	TM2IRQ	TM3IRQ
Timer operation	√	√	√	√
Event count	√	√	√	√
Timer pulse output	√	√	√	√
PWM output	√	-	√	-
Large current timer output pin	√	-	√	-
Additional pulse method PWM(2bit)	-	-	√	-
Synchronous output	-	√	√	-
Serial transfer clock output	-	-	-	√
Pulse width measurement	√	-	√	-
Cascade connection	√		√	
Remote control carrier output	√	-	-	√
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input	fosc fosc/4 fosc/16 $fosc/2^{13}$ $fosc/2^{15}$ fs/2 fs/8 fx TM1IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM2IO input	fosc fosc/4 fosc/16 fosc/64 fosc/128 fs/2 fs/8 fx TM3IO input

fosc : Machine clock (High frequency oscillation)
fx : Machine clock (Low frequency oscillation)
fs : System clock [☞ Chapter 2 2-5 Clock Switching]
- When timers 3 are used as a baud rate timer for serial function, it is not used as a general timer.

6-1-2 Block Diagram

■Timers 0 and 1 Block Diagram

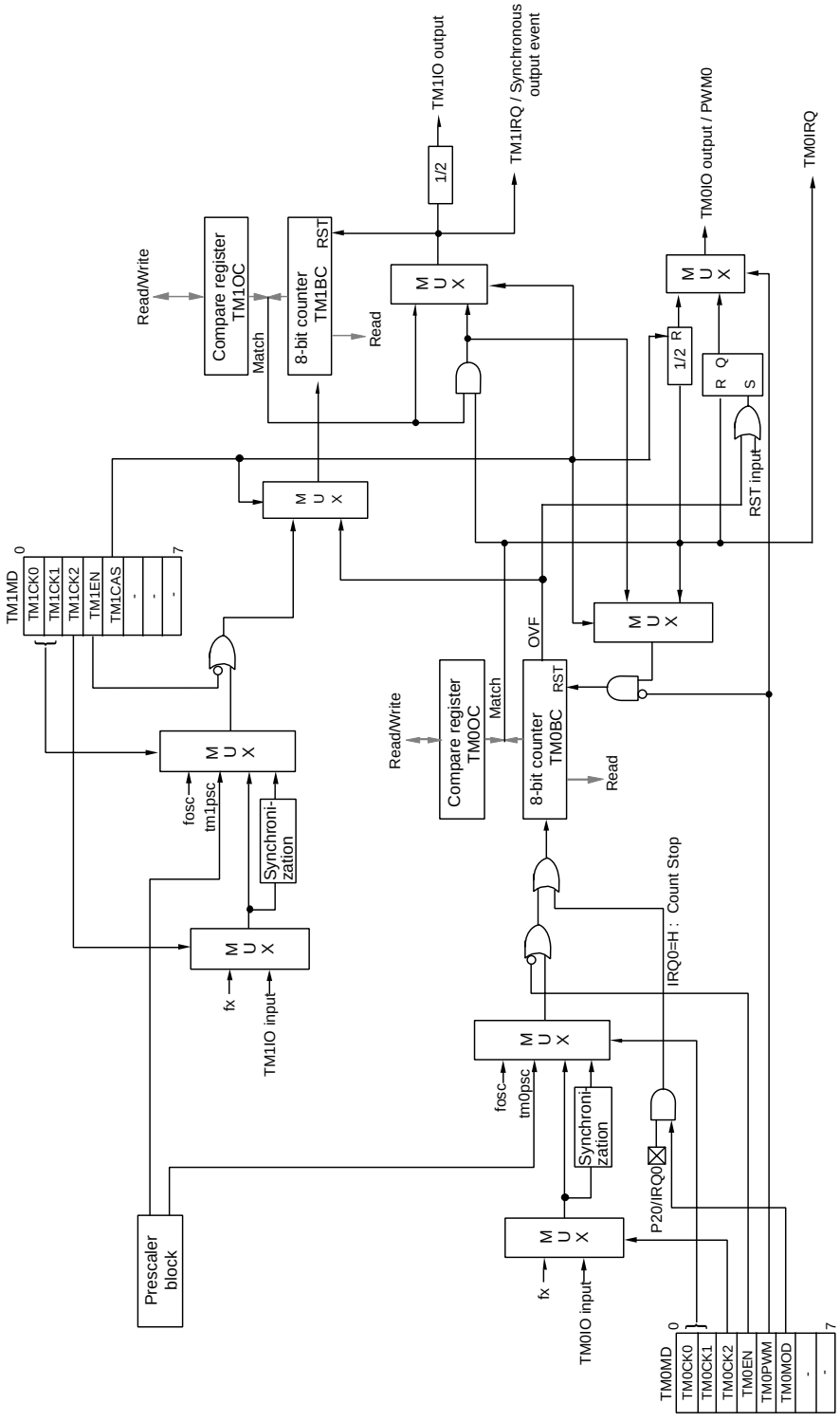


Figure 6-1-1 Timers 0 and 1 Block Diagram

■Timers 2 and 3 Block Diagram

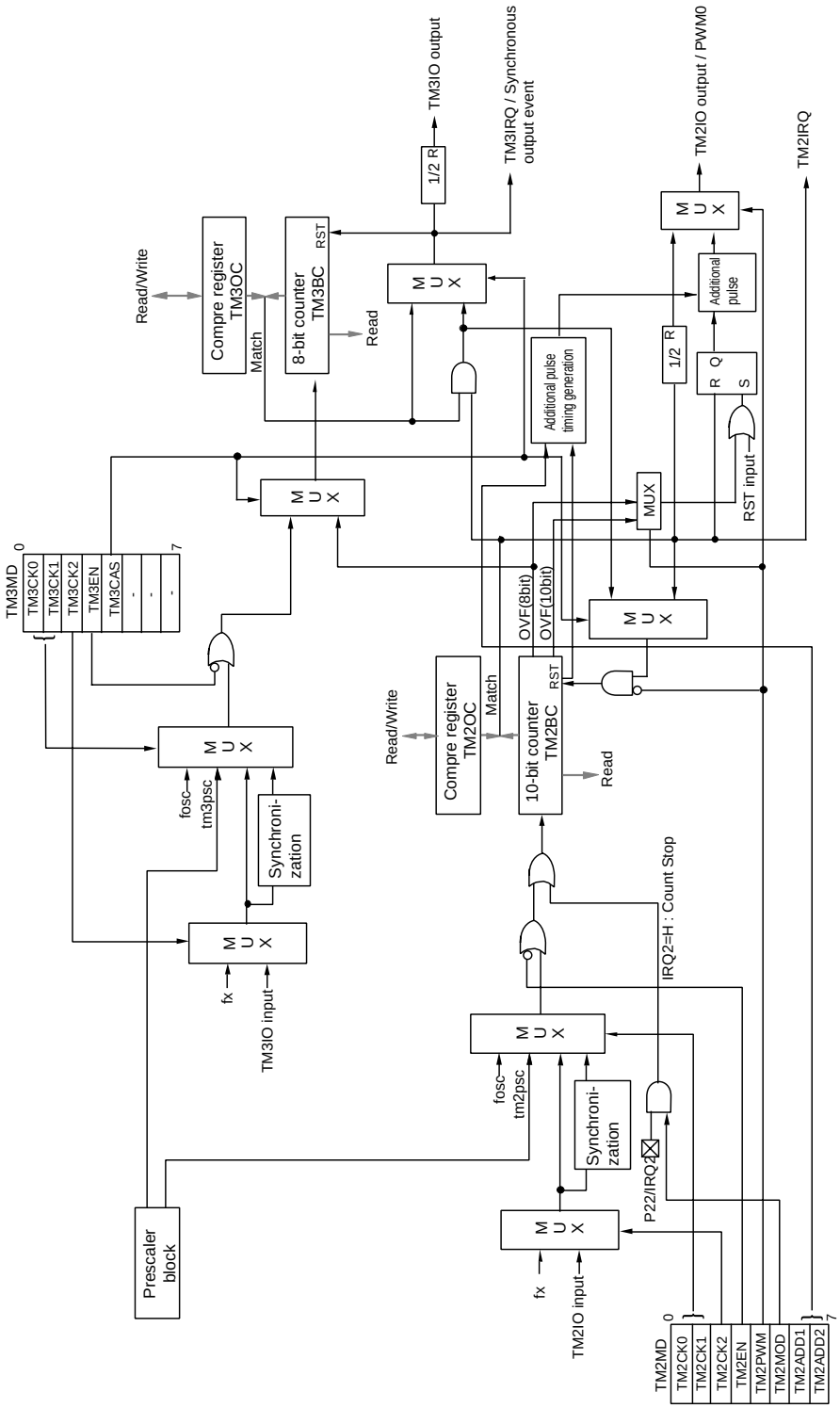


Figure 6-1-2 Timers 2 and 3 Block Diagram

■Remote Control Carrier Output Block Diagram

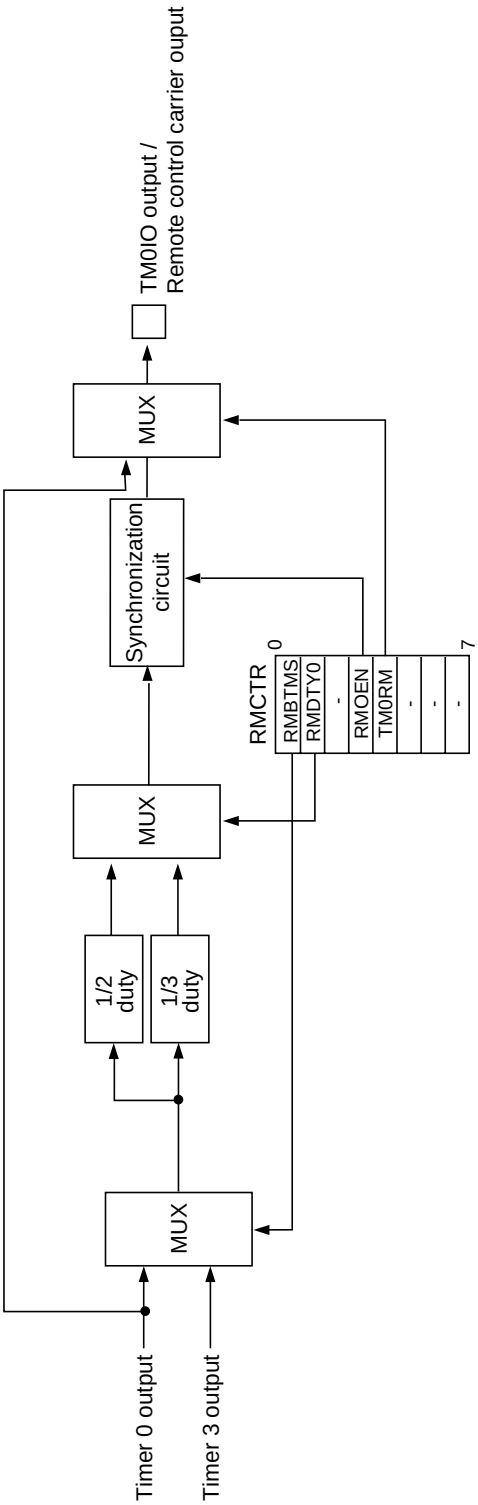


Figure 6-1-3 Remote Control Carrier Output Block Diagram

6-2 Control Registers

Timers 0 to 3 consist of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD).
When the prescaler output is selected as the count clock source of timers 0 to 3, they should be controlled by the prescaler control register (PSCMD) and the prescaler selection register (CKnMD). Remote control is controlled by the remote control carrier output control register (RMCTR).

6-2-1 Registers

Table 6-2-1 shows registers that control timers 0 to 3 and remote control.

Table 6-2-1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 0	TM0BC	x'03F50'	R	Timer 0 binary counter	VI-9
	TM0OC	x'03F52'	R/W	Timer 0 compare register	VI-8
	TM0MD	x'03F54'	R/W	Timer 0 mode register	VI-10
	CK0MD	x'03F56'	R/W	Timer 0 prescaler selection register	V-7
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM0ICR	x'03FE9'	R/W	Timer 0 interrupt control register	III-24
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-15
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-14
Timer 1	TM1BC	x'03F51'	R	Timer 1 binary counter	VI-9
	TM1OC	x'03F53'	R/W	Timer 1 compare register	VI-8
	TM1MD	x'03F55'	R/W	Timer 1 mode register	VI-11
	CK1MD	x'03F57'	R/W	Timer 1 prescaler selection register	V-7
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM1ICR	x'03FEA'	R/W	Timer 1 interrupt control register	III-25
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-15
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-14
Timer 2	TM2BC	x'03F58'	R	Timer 2 binary counter	VI-9
	TM2OC	x'03F5A'	R/W	Timer 2 compare register	VI-8
	TM2MD	x'03F5C'	R/W	Timer 2 mode register	VI-12
	CK2MD	x'03F5E'	R/W	Timer 2 prescaler selection register	V-8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM2ICR	x'03FEB'	R/W	Timer 2 interrupt control register	III-26
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-15
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-14

	Register	Address	R/W	Function	Page
Timer 3	TM3BC	x'03F59'	R	Timer 3 binary counter	VI-9
	TM3OC	x'03F5B'	R/W	Timer 3 compare register	VI-8
	TM3MD	x'03F5D'	R/W	Timer 3 mode register	VI-13
	CK3MD	x'03F5F'	R/W	Timer 3 prescaler selection register	V-8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM3ICR	x'03FEC'	R/W	Timer 3 interrupt control register	III-27
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-15
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-14
Remote control	RMCTR	x'03F6E'	R/W	Remote control carrier output control register	VI-14

R/W : Readable / Writable

R : Readable only

6-2-2 Programmable Timer Registers

Each of timers 0 to 3 has 8-bit programmable timer registers. Programmable timer register consists of compare register and binary counter.

Compare register is 8-bit register which stores the value to be compared to binary counter are stocked.

■Timer 0 Compare Register (TM0OC)

	7	6	5	4	3	2	1	0	
TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	(At reset : X X X X X X X X)

Figure 6-2-1 Timer 0 Compare Register (TM0OC : x'03F52', R/W)

■Timer 1 Compare Register (TM1OC)

	7	6	5	4	3	2	1	0	
TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	(At reset : X X X X X X X X)

Figure 6-2-2 Timer 1 Compare Register (TM1OC : x'03F53', R/W)

■Timer 2 Compare Register (TM2OC)

	7	6	5	4	3	2	1	0	
TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	(At reset : X X X X X X X X)

Figure 6-2-3 Timer 2 Compare Register (TM2OC : x'03F5A', R/W)

■Timer 3 Compare Register (TM3OC)

	7	6	5	4	3	2	1	0	
TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	(At reset : X X X X X X X X)

Figure 6-2-4 Timer 3 Compare Register (TM3OC : x'03F5B', R/W)

Binary counter is 8-bit up counter. If any data is written to compare register the counting is stopped and binary counter is cleared to x'00'.

■Timer 0 Binary Counter (TM0BC)

	7	6	5	4	3	2	1	0	
TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	(At reset : X X X X X X X X)

Figure 6-2-5 Timer 0 Binary Counter (TM0BC : x'03F50', R)

■Timer 1 Binary Counter (TM1BC)

	7	6	5	4	3	2	1	0	
TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	(At reset : X X X X X X X X)

Figure 6-2-6 Timer 1 Binary Counter (TM1BC : x'03F51', R)

■Timer 2 Binary Counter (TM2BC)

	7	6	5	4	3	2	1	0	
TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	(At reset : X X X X X X X X)

Figure 6-2-7 Timer 2 Binary Counter (TM2BC : x'03F58', R)

■Timer 3 Binary Counter (TM3BC)

	7	6	5	4	3	2	1	0	
TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	(At reset : X X X X X X X X)

Figure 6-2-8 Timer 3 Binary Counter (TM3BC : x'03F59', R)

6-2-3 Timer Mode Registers

Timer mode register is readable/writable register that controls timers 0 to 3.

■Timer 0 Mode Register (TM0MD)

	7	6	5	4	3	2	1	0
TM0MD	-	-	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0

(At reset : - - 0 0 0 0 0 0)

TM0CK2	TM0CK1	TM0CK0	Clock source selection
-	0	0	fosc
		1	tm0psc (prescaler output)
0	1	0	fx
		1	Synchronous fx
1		0	TM0IO input
		1	Synchronous TM0IO input

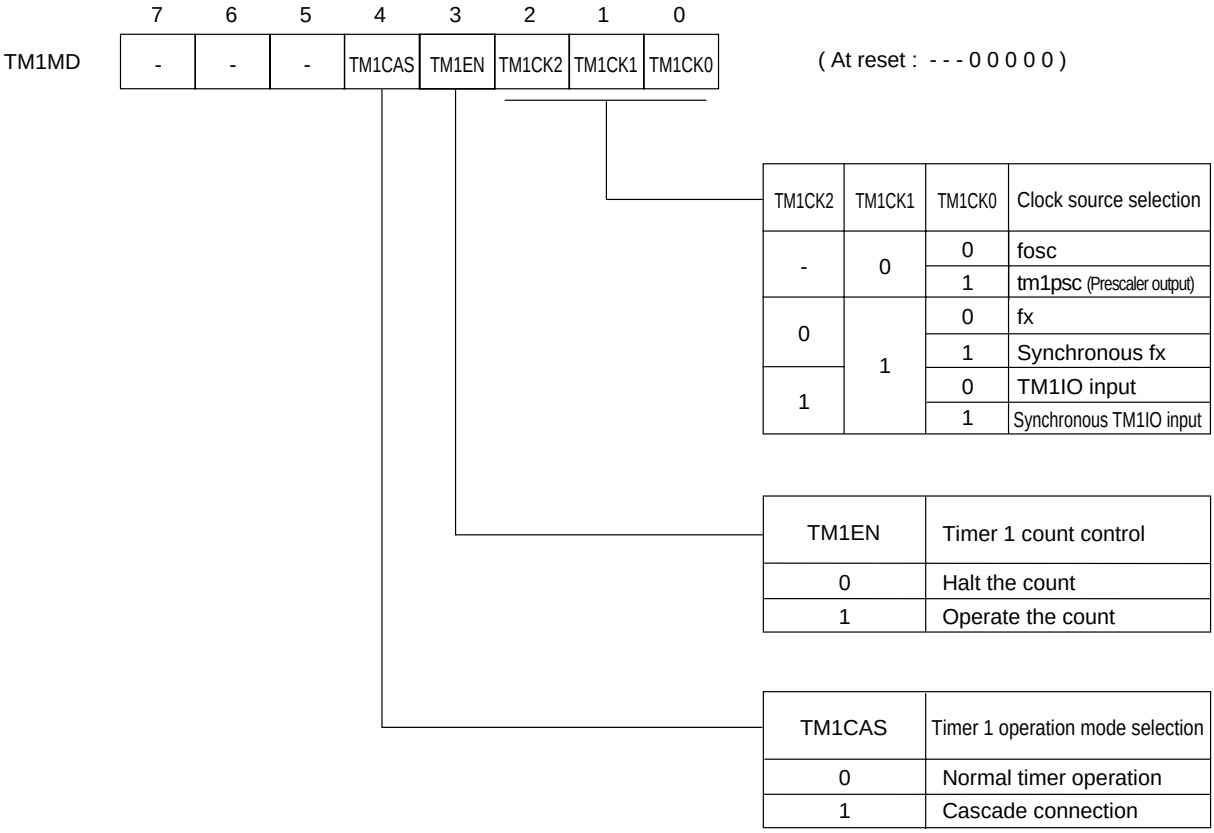
TM0EN	Timer 0 count control
0	Halt the count
1	Operate the count

TM0PWM	Timer 0 operation mode selection
0	Normal timer operation
1	PWM operation

TM0MOD	Pulse width measurement control
0	Normal timer operation
1	Measure the pulse width of P20/IRQ0

Figure 6-2-9 Timer 0 Mode Register (TM0MD : x'03F54', R/W)

■Timer 1 Mode Register (TM1MD)



TM1CK2	TM1CK1	TM1CK0	Clock source selection
-	0	0	fosc
		1	tm1psc (Prescaler output)
0	1	0	fx
		1	Synchronous fx
1		0	TM1IO input
		1	Synchronous TM1IO input

TM1EN	Timer 1 count control
0	Halt the count
1	Operate the count

TM1CAS	Timer 1 operation mode selection
0	Normal timer operation
1	Cascade connection

Figure 6-2-10 Timer 1 Mode Register (TM1MD : x'03F55', R/W)

■Timer 2 Mode Register (TM2MD)

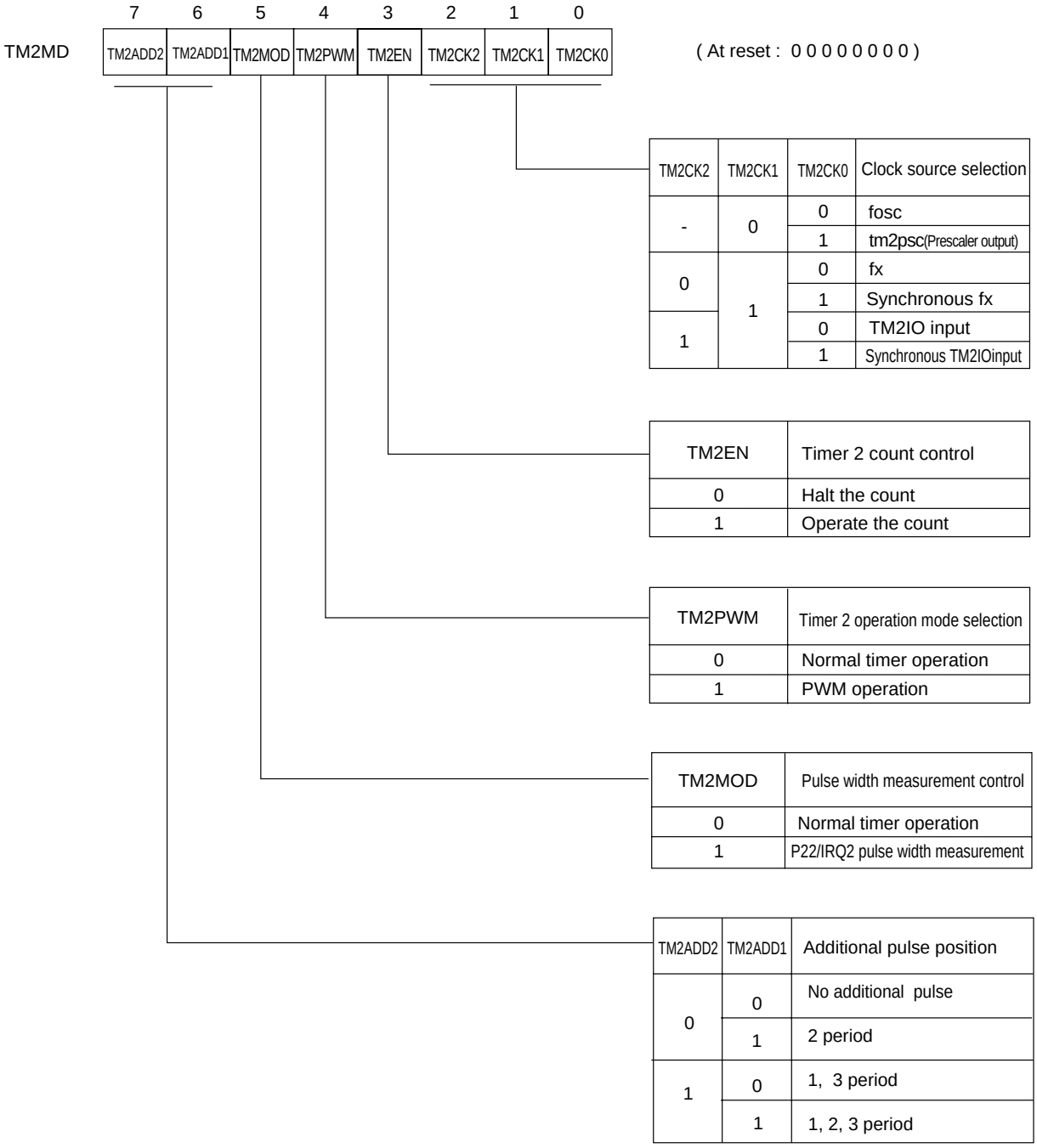
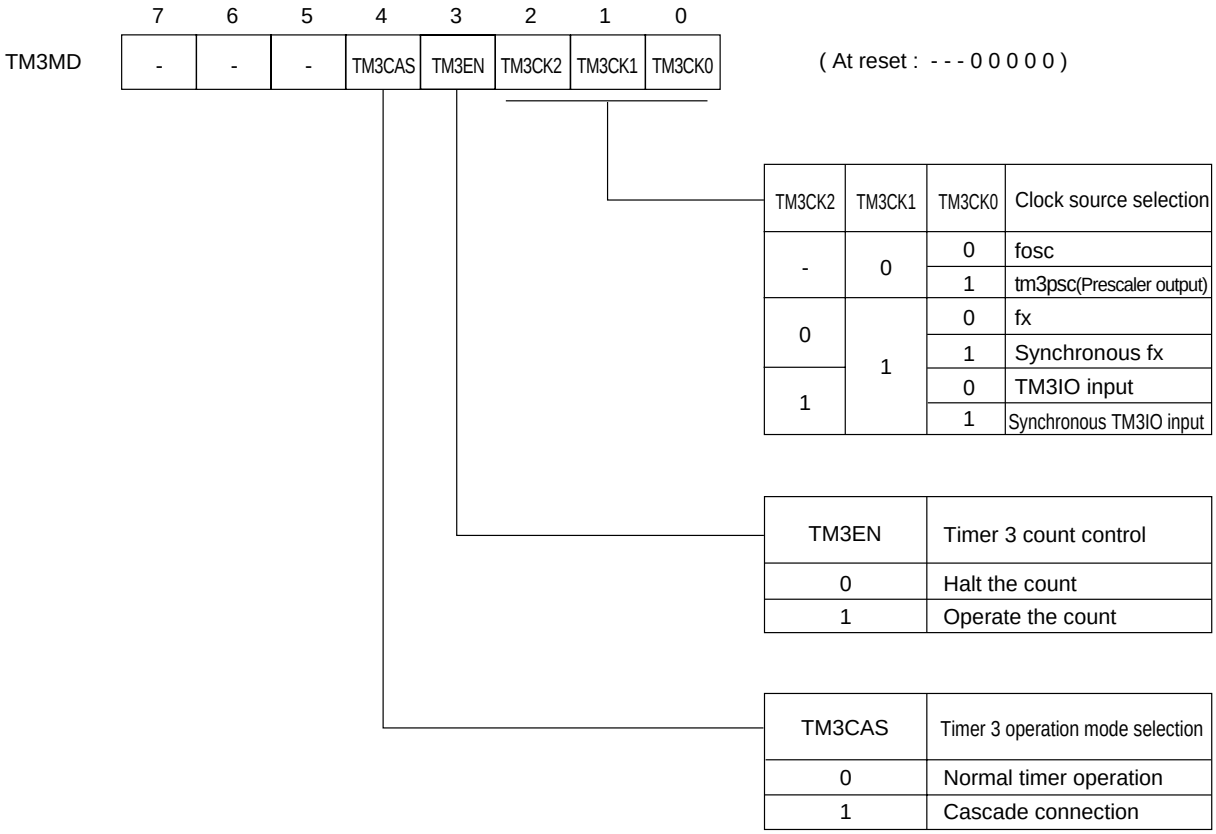

7 6 5 4 3 2 1 0
TM2MD
TM2ADD2 TM2ADD1 TM2MOD TM2PWM TM2EN TM2CK2 TM2CK1 TM2CK0
(At reset : 0 0 0 0 0 0 0 0)
TM2CK2 TM2CK1 TM2CK0 Clock source selection
- 0 0 fosc
1 tm2psc(Prescaler output)
0 1 0 fx
1 Synchronous fx
1 0 TM2IO input
1 Synchronous TM2IOinput
TM2EN Timer 2 count control
0 Halt the count
1 Operate the count
TM2PWM Timer 2 operation mode selection
0 Normal timer operation
1 PWM operation
TM2MOD Pulse width measurement control
0 Normal timer operation
1 P22/IRQ2 pulse width measurement
TM2ADD2 TM2ADD1 Additional pulse position
0 0 No additional pulse
1 2 period
1 0 1, 3 period
1 1, 2, 3 period

Figure 6-2-11 Timer 2 Mode Register (TM2MD : x'03F5C', R/W)

■Timer 3 Mode Register (TM3MD)



TM3CK2	TM3CK1	TM3CK0	Clock source selection
-	0	0	fosc
		1	tm3psc(Prescaler output)
0	1	0	fx
		1	Synchronous fx
1		0	TM3IO input
		1	Synchronous TM3IO input

TM3EN	Timer 3 count control
0	Halt the count
1	Operate the count

TM3CAS	Timer 3 operation mode selection
0	Normal timer operation
1	Cascade connection

Figure 6-2-12 Timer 3 Mode Register (TM3MD : x'03F5D', R/W)

■Remote Control Carrier Output Control Register (RMCTR)

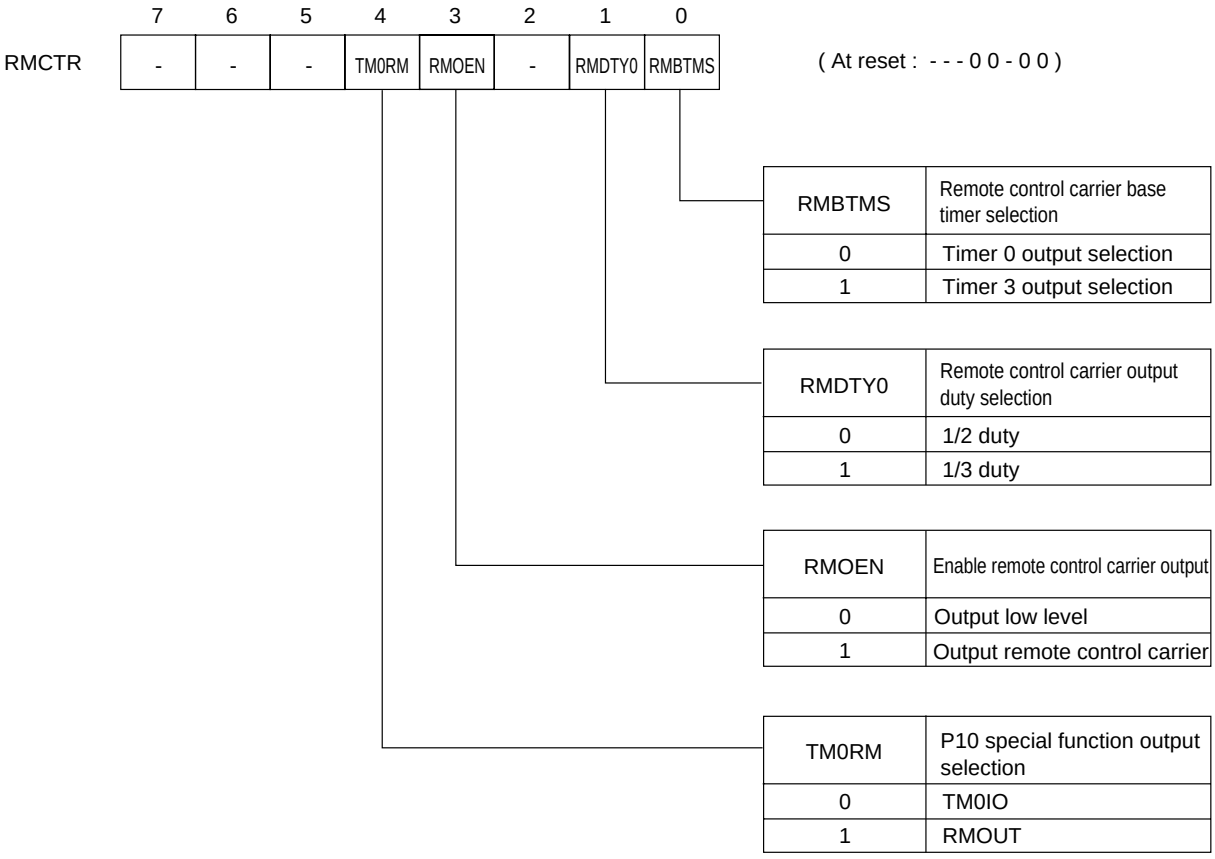


Figure 6-2-13 Remote Control Carrier Output Control Register (RMCTR : x'03F6E', R/W)

6-3 Operation

6-3-1 Operation

The timer operation can constantly generate interrupts.

■8-bit Timer Operation (Timers 0, 1, 2, and 3)
The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from x'00'.
Table 6-3-1 shows clock source that can be selected by timer.

Table 6-3-1 Clock Source (Timers 0, 1, 2, and 3) at Timer Operation

Clock source	per Count	Timer 0 (8 bit)	Timer 1 (8 bit)	Timer 2 (8 bit)	Timer 3 (8 bit)
fosc	50 ns	√	√	√	√
fosc/4	200 ns	√	√	√	√
fosc/16	800 ns	√	√	√	√
fosc/32	1.6 µs	√	-	√	-
fosc/64	3.2 µs	√	-	√	√
fosc/128	6.4 µs	-	-	-	√
$fosc/2^{13}$	409.6 µs	-	√	-	-
$fosc/2^{15}$	1.64 ms	-	√	-	-
fs/2	200 ns	√	√	√	√
fs/4	400 ns	√	-	√	-
fs/8	800 ns	-	√	-	√
fx	30.5 µs	√	√	√	√
Notes : fosc = 20 MHz fx = 32.768 kHz fs = fosc/2 = 10 MHz					

■Count Timing of Timer Operation (Timers 0, 1, 2, and 3)

Binary counter counts up with selected clock source as a count clock.

The basic operation of the whole function of 8-bit timer is as follows ;

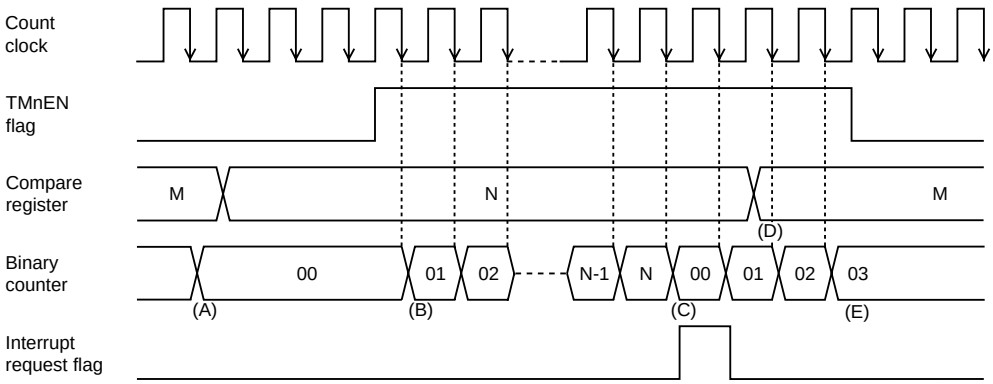


Figure 6-3-1 Count Timing of Timer Operation (Timers 0, 1, 2, and 3)

(A) If the value is written to the compare register during the TMnEN flag is stopped ("0"), the binary counter is cleared to x'00', at the writing cycle.

(B) If the TMnEN flag is operated ("1"), the binary counter is started to count.
The counter starts to count up at the falling edge of the count clock.

(C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to x'00' and the counting is restarted.

(D) Even if the compare register is rewritten during the TMnEN flag is enabled ("1"), the binary counter is not changed.

(E) If the TMnEN flag is stopped ("0"), the binary counter is stopped.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So set the compare register as: Compare register setting = (count till the interrupt request - 1)

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer is started.

The timer n interrupt request generation (at TMnOC = x'00') has the same waveform at TMnOC = x'01'.

6-3-2 Setup Example

■Timer Operation Setup Example (Timers 0, 1, 2, and 3)
Timer function can be set by using timer 0 that generates the constant interrupt. Interrupt is generated every 250 cycles (100 µs) by selecting fs/4 (at fosc = 20 MHz operation) as a clock source.
A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the counting of timer 0.
(2) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(2) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 001	(3) Select the prescaler output to the clock source by the TM0CK2-0 flag of the TM0MD register.
(4) Select the prescaler output and enable the counting. CK0MD (x'3F56') bp2-1 :TM0PSC1-0 = 01 bp0 :TM0BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(4) Select fs/4 to the prescaler output by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the counting of the prescaler.
(5) Set the cycle of the interrupt generation. TM0OC (x'3F52') = x'F9'	(5) Set the value of the interrupt generation cycle to the timer 0 compare register (TM0OC). The cycle is 250, so that the setting value is set to 249 (x'F9'). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Set the interrupt level. TM0ICR (x'3FE9') bp7-6 :TM0LV1-0 = 10	(6) Set the interrupt level by the TM0LV1-0 flag of the timer 0 interrupt control register (TM0ICR). [☞ Chapter 3 3-1-4. Interrupt flag setting] If the interrupt request flag may be already set, clear the request flag.

Setup Procedure	Description
(7) Enable the interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 1	(7) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(8) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to "1" to start the timer 0.

The TM0BC starts to count up from 'x00'. When the TM0BC reaches the setting value of the TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of the TM0BC becomes x'00' and restart to count up.

When the TMnEN flag of the TMnMD register is changed at the same time to other bit, binary counter may start to count up by the switching operation.

6-4 8-bit Event Count

6-4-1 Operation

Event count operation has 2 types ; TMnIO input and synchronous TMnIO input, according to the clock source selection.

■8-bit Event Count Operation

Event count operation means that the binary counter (TMnBC) counts the input signal from external to the TMnIO pin. If the value of the binary counter reaches the setting value of the compare register (TMnOC), interrupts can be generated at the next count clock.

Table 6-4-1 Event Count Input Clock

	Timer 0	Timer 1	Timer 2	Timer 3
Event input	TM0IO input (P10)	TM1IO input (P11)	TM2IO input (P12)	TM3IO input (P13)
	Synchronous TM0IO input	Synchronous TM1IO input	Synchronous TM2IO input	Synchronous TM3IO input

■Count Timing of TMnIO Input (Timers 0, 1, 2, and 3)

When TMnIO input is selected, TMnIO input signal is directly input to the count clock of the timer n. The binary counter is started to count up at the falling edge of the TMnIO input signal.

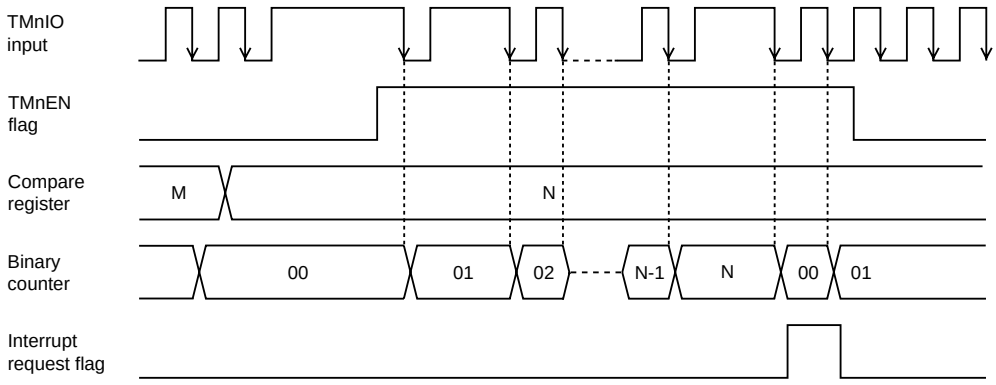


Figure 6-4-1 Count Timing of TMnIO Input (Timers 0 to 3)

When the TMnIO input is selected for count clock source and the value of the timer n binary counter is read out during operation, incorrect value at count up may be read out. To prevent this, use the event count by synchronous TMnIO input, as the following page.

■Count Timing of Synchronous TMnIO Input (Timers 0, 1, 2, and 3)

If the synchronous TMnIO input is selected, the synchronous circuit output signal is inputted to the timer n count clock. The synchronous circuit output signal is in synchronization with the falling edge of the system clock derived the TMnIO input signal.

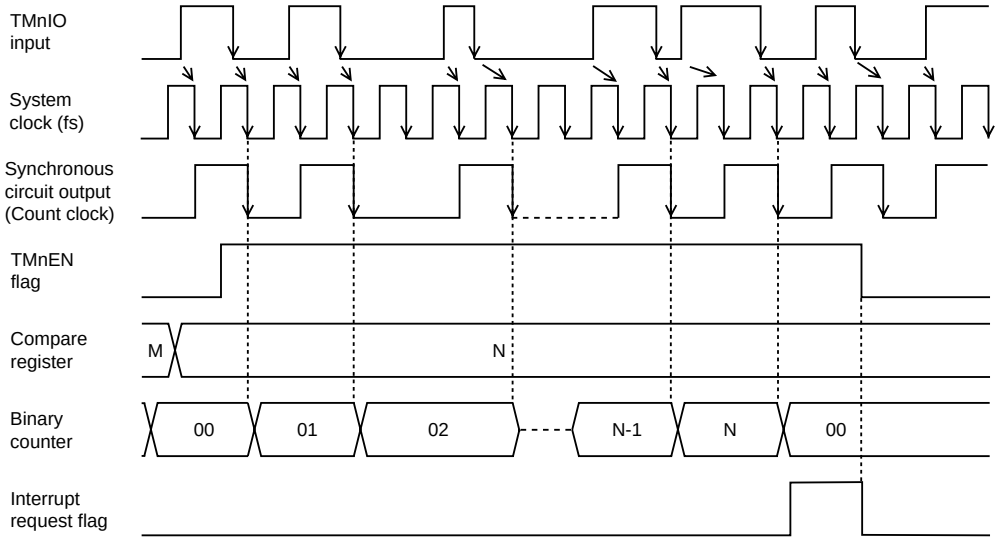


Figure 6-4-2 Count Timing of Synchronous TMnIO Input (Timers 0 to 3)

When the synchronous TMnIO input is selected as the count clock source, the timer n counter counts up in synchronization with system clock, therefore the correct value is always read out.

Synchronous TMnIO input cannot return from STOP/HALT mode.

6-4-2 Setup Example

■Event Count Setup Example (Timers 0, 1, 2, and 3)
If the falling edge of the TMnIO input pin signal is detected 5 times, an interrupt is generated.
A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to input. P1DIR (x'3F31') bp0 :P1DIR0 = 0	(2) Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "0" to set P10 pin to input mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4. I/O Port Function]
(3) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 110	(4) Select the clock source to TM0IO input by the TM0CK2-0 flag of the TM0MD register.
(5) Set the interrupt generation cycle. TM0OC (x'3F52') = x'04'	(5) Set the timer 0 compare register (TM0OC) the interrupt generation cycle. Counting is 5, so the setting value should be 4. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Set the interrupt level. TM0ICR (x'3FE9') bp7-6 :TM0LV1-0 = 10	(6) Set the interrupt level by the TM0LV1-0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, cancel all existing interrupt requests. [☞ Chapter 3 3-1-4. Interrupt Flag Setting]

Setup Procedure	Description
(7) Enable the interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 1	(7) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(8) Start the event counting. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to start timer 0.

Every time TM0BC detects the falling edge of TM0IO input, TM0BC counts up from 'x00'. When TM0BC reaches the setting value of theTM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of TM0BC becomes x'00' and counting up is restarted.

6-5 8-bit Timer Pulse Output

6-5-1 Operation

The TMnIO pin can output a pulse signal at any frequency.

■Operation of Timer Pulse Output (Timers 0, 1, 2, and 3)
The timers can output signals of 2 x cycle of the setup value in the compare register (TMnOC). Output pins are as follows;

Table 6-5-1 Timer Pulse Output Pins

	Timer 0	Timer 1	Timer 2	Timer 3
Pulse output pin	TM0IO output (P10)	TM1IO output (P11)	TM2IO output (P12)	TM3IO output (P13)

■Count Timing of Timer Pulse Output (Timers 0, 1, 2, and 3)

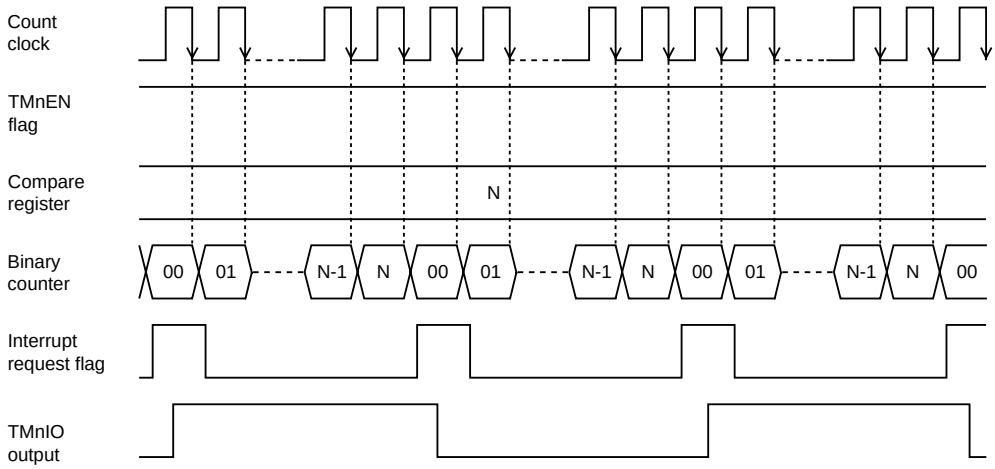


Figure 6-5-1 Count Timing of Timer Pulse Output (Timers 0 to 3)

The TMnIO pin outputs signals of 2 x cycle of the setup value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to x'00', TMnIO output (timer output) is inverted. The inversion of the timer output is changed at the rising edge of the count clock. This is happened to form waveform inside to correct the output cycle.

6-5-2 Setup Example

■Timer Pulse Output Setup Example (Timer 0, 1, 2, and 3)
TM0IO pin outputs 50 kHz pulse by using timer 0. For this, select fosc for clock source, and set a 1/2 cycle (100 kHz) for the timer 0 compare register (at fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F2F') bp0 :P1OMD0 = 1 P1DIR (x'3F31') bp0 :P1DIR0 = 1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 the special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4. I/O Ports]
(3) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 000	(4) Select fosc for the clock source by the TM0CK2-0 flag of the TM0MD register.
(5) Set the timer pulse output cycle. TM0OC (x'3F52') = x'C7'	(5) Set the timer 0 compare register (TM0OC) to the 1/2 of the timer pulse output cycle. The setting value should be 200-1=199(x'C7'), for 100 kHz to be divided by 20 MHz. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(6) Set the TM0EN flag of the TM0MD register to "1" to start timer 0.

TM0BC counts up from x'00'. If TM0BC reaches the setting value of the TM0OC register, then TM0BC is cleared to x'00', TM0IO output signal is inverted and TM0BC restart to count up from x'00'.

At TMnOC = x'00', timer pulse output has the same waveform to at x'01'.

If any data is written to compare register binary counter is stopped, timer output is reset to "L".

6-6 8-bit PWM Output

The TMnIO pin outputs the PWM waveform, which is determined by the match timing for the compare register and the overflow timing of the binary counter.

6-6-1 Operation

■Operation of 8-bit PWM Output (Timers 0, and 2)

The PWM waveform with an arbitrary duty cycle is generated by setting the duty cycle of PWM period to the compare register (TMnOC). The cycle is the period from the full count to the overflow of the 8-bit timer. Table 6-6-1 shows PWM output pins ;

Table 6-6-1 Output Pins of PWM Output

	Timer 0	Timer 2
PWM output pin	TM0IO output pin (P10)	TM2IO output pin (P12)

■Count Timing of PWM Output (at Normal) (Timers 0, and 2)

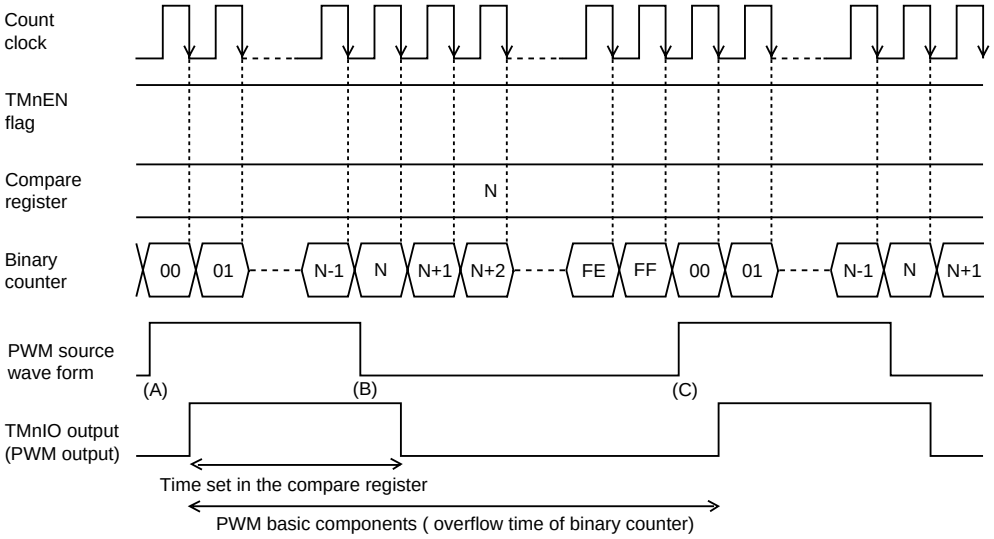


Figure 6-6-1 Count Timing of PWM Output (at Normal)

PWM source waveform,

(A) is "H" while counting up from x'00' to the value stored in the compare register.

(B) is "L" after the match to the value in the compare register, then the binary counter continues counting up till the overflow.

(C) is "H" again, if the binary counter is overflown.

The PWM outputs PWM source waveform with 1 count clock delay, because the waveform is created inside to correct the output cycle.

■Count Timing of PWM Output (when the compare register is x'00') (Timers 0, and 2)
Here is the count timing when the compare register is set to x'00' ;

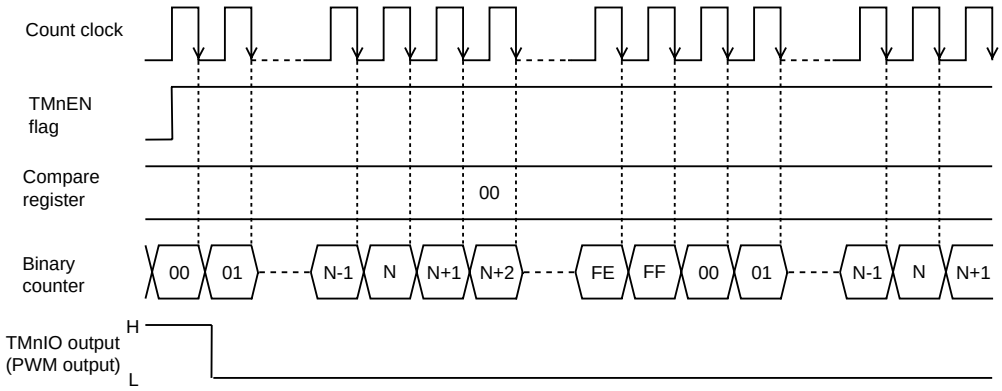


Figure 6-6-2 Count Timing of PWM Output (when compare register is x'00')

When TMnEN flag is stopped ("0") PWM output is "H".

■Count Timing of PWM Output (when the compare register is x'FF') (Timers 0, and 2)
Here is the count timing when the compare register is set to x'FF' ;

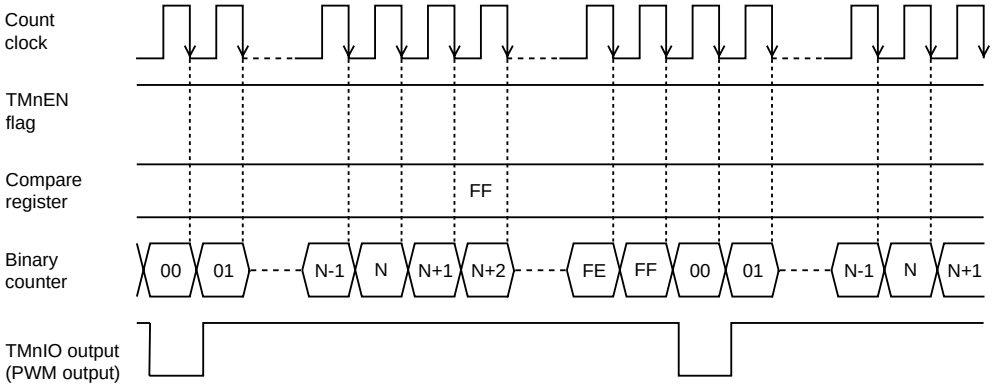


Figure 6-6-3 Count Timing of PWM Output (when compare register is x'FF')

6-6-2 Setup Example

■PWM Output Setup Example (Timers 0, and 2)

The 1/4 duty cycle PWM output waveform is output from the TM0IO output pin at 128 Hz by using timer 0. Low frequency oscillation(fx) is at 32.768 kHz. Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register.

An example setup procedure, with a description of each step is shown below.

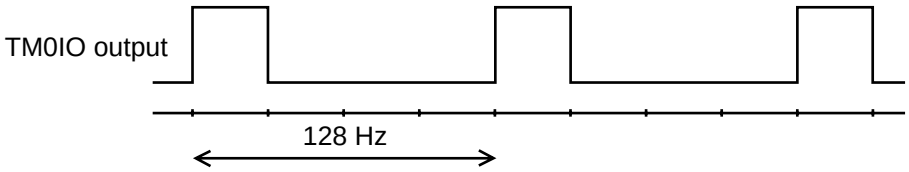


Figure 6-6-4 Output Waveform of TM0IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F2F') bp0 :P1OMD0 = 1 P1DIR (x'3F31') bp0 :P1DIR0 = 1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin to the special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for the output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4. I/O Ports]
(3) Select the PWM operation. TM0MD (x'3F54') bp4 :TM0PWM = 1 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag of the TM0MD register to "1", the TM0MOD flag to "0" to select the PWM operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 010	(4) Select "fs" for the clock source by the TM0CK2-0 flag of the TM0MD register.

Setup Procedure	Description
(5) Set the period of PWM "H" output. TM0OC (x'3F52') = x'40'	(5) Set the "H" period of PWM output to the timer 0 compare register (TM0OC). The setting value is set to 256 / 4 = 64 (x'40'), because it should be the 1/4 duty of the full count (256). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(6) Set the TM0EN flag of the TM0MD register to "1" to operate timer 0.

TM0BC counts up from x'00'. PWM source waveform outputs "H" till TM0BC reaches the setting value of the TM0OC register, and outputs "L" after that. Then, TM0BC continues counting up, and PWM source waveform outputs "H" again, once overflow is happened, and TM0BC restarts counting up from x'00'. TM0IO pin outputs the PWM source waveform with 1 count clock delay.

The initial setting of PWM output is changed from "L" output to "H" output at the selection of PWM operation by the TMnPWM flag of the TMnMD register.

6-6-3 PWM Output With Additional Pulse

■PWM Output with Additional Pulse Method (Timer 2)

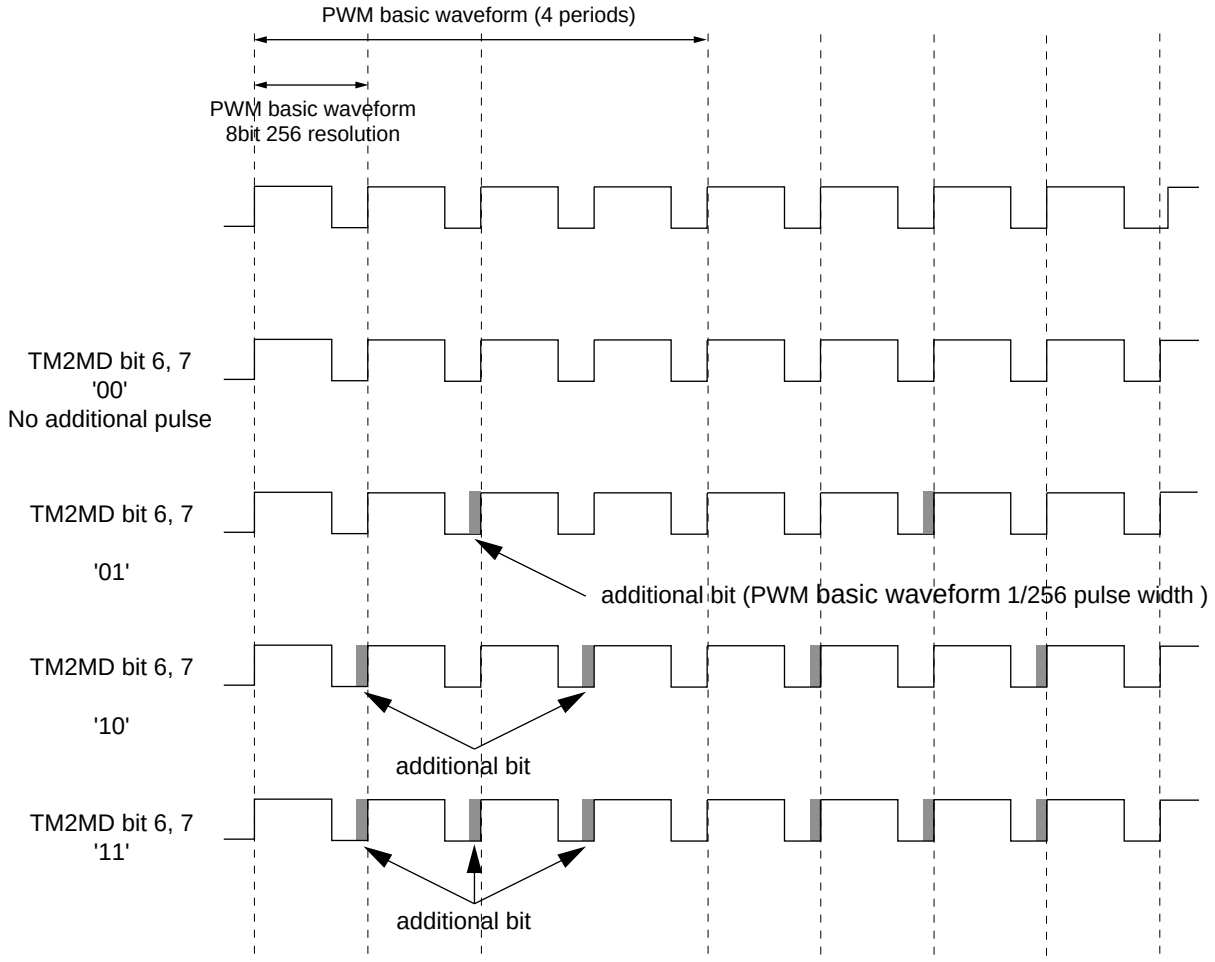
In the additional pulse method, an additional bit is added to the 8-bit basic PWM output.
The bit0 to3 can be added during 4 cycle of basic PWM output.
Whether or not, and to which the additional bit is added during 4 cycles of basic PWM output can be controlled with the Timer 2 mode register (TM2MD bit 6, 7).

■Setting the position of the Additional Pulses

The positions of the additional pulse is set in the Timer 2 mode register (TM2MD) at bits 6 and 7. When TM2MD bits 6 and 7 are set as '00', no additional pulse is added to the basic PWM cycle. When set as '11', 3 out of the 4 periods in the basic PWM cycle are each added with an additional bit pulse.
Table 6-6-3 shows the relationship between the values TM2MD bits 6 and 7, and the additional pulses.
Figure 6-6-5 shows the relationship between values of TM2MD bits 6 and 7, and the positions of the additional pulses.

Table 6-6-3

TM2MD register set value		Additional Pulse position PWM basic wave form(4-periods)
bit7	bit6	
0	0	No additional Pulse
0	1	2 period
1	0	1 and 3 period
1	1	1, 2 and 3 period



During 4 cycles of the PWM basic waveform, additional pulses(1/256 pulse width of PWM basic waveform) can be added in any of the periods 0 to 3.

Figure 6-6-5

6-7 Synchronous Output

6-7-1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latch data is output from port 4 at the next count clock.

■Synchronous Output Operation by 8-bit timer (Timer 1, Timer 2)

The port 4 latched data is output from the output pin in synchronization with the interrupt request generation by the match of the binary counter and the compare register.

Only port 4 can perform synchronous output operation, and individual bits can be set. 8-bit timers that have synchronous output operation are timer 1 and timer 2.

Table 6-7-1 Synchronous Output Port (Timer 1, Timer 2)

	Timer 1	Timer 2
Synchronous output port	Port 4	Port 4

■Timing of Synchronous Output (Timer 1, Timer 2)

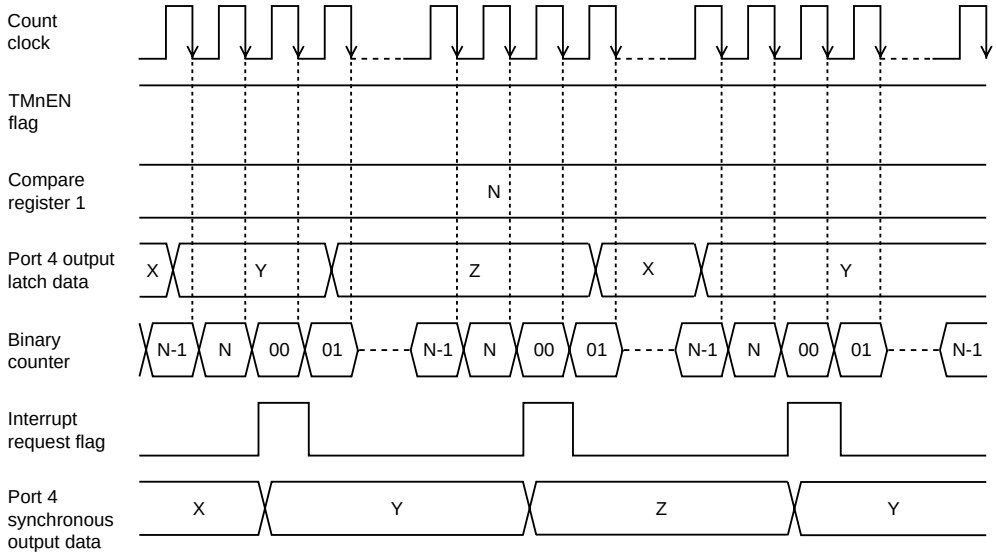


Figure 6-7-1 Timing of Synchronous Output (Timer 1, Timer2)

The port 4 output latched data is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

6-7-2 Setup Example

■Synchronous Output Setup Example (Timer 1, Timer 2)

Setup example that latch data of port 4 is output constantly (100 µs) by using timer 2 from the synchronous output pin is shown below. The clock source of timer 2 is selected fs/4 (fosc=8 MHz at operation). A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Start the counter. TM2MD (x'3F5C') bp3 :TM2EN = 0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(2) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 :SYOEVS1-0 = 10	(2) Set the SYOEVS1-0 flag of the pin control register (FLOAT) to "10" to set the synchronous output event to timer 2 interrupt.
(3) Set the synchronous output pin. P4SYO (x'3F1F') = x'FF' P4DIR (x'3F3D') = x'FF'	(3) Set the port 4 synchronous output control register (P4SYO) to x'FF' to set the synchronous output pin. (P47 to P40 are synchronous output pin.) Set the port 4 direction control register (P4DIR) to x'FF' to set port 4 to output mode. Add pull-up resistor, if necessary. [☞ Chapter 4. I/O Ports]
(4) Select the normal timer operation. TM2MD (x'3F5C') bp4 :TM2PWM = 0 bp5 :TM2MOD = 0	(4) Set the TM2PWM flag and TM2MOD flag of the TM2MD register to "0" to select the normal timer operation.
(5) Select the count clock source. TM2MD (x'3F5C') bp2-0 :TM2CK2-0 = 001	(5) Select the prescaler output for clock source by TM2CK2-0 flag of the TM2MD register.
(6) Select the prescaler output and enable counting. CK2MD (x'3F5E') bp2-1 :TM2PSC1-0 = 01 bp0 :TM2BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(6) Select fs/4 for the prescaler output by TM2BAS flag, TM2PSC1-0 of the timer 2 prescaler selection register (CK2MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.

Setup Procedure	Description
(7) Set the synchronous output event generation cycle. TM2OC (x'3F5A') = x'63'	(7) Set the synchronous output generation cycle to the timer 2 compare register (TM2OC). The setting value is set to 100-1=99(x'63'), because 1 MHz is divided by 10 kHz. At that time, the timer 2 binary counter (TM2BC) is initialized to x'00'.
(8) Start the timer operation. TM2MD (x'3F5C') bp3 :TM2EN = 1	(8) Set the TM2EN flag of the TM2MD register to "1" to start timer 2.

TM2BC counts up from x'00'. If any data is written to the port 4 output register (P4OUT), the data of port 4 is output from the synchronous output pin in every time an interrupt request is generated by the match of TM2BC and the set value of the TM2OC register.

6-8 Serial Transfer Clock Output

6-8-1 Operation

Serial transfer clock can be created by using the timer output signal.

■Serial Transfer Clock Operation by 8-bit Timer (Timer 3)
Timer 3 output can be used as a transfer clock source for serial interface 0, serial interface 2.

Table 6-8-1 Operation Timer for Serial Transfer Clock

Serial transfer clock	Timer 3
Serial interface 0	√
Serial interface 2	√

■Timing of Serial Transfer Clock (Timer 3)

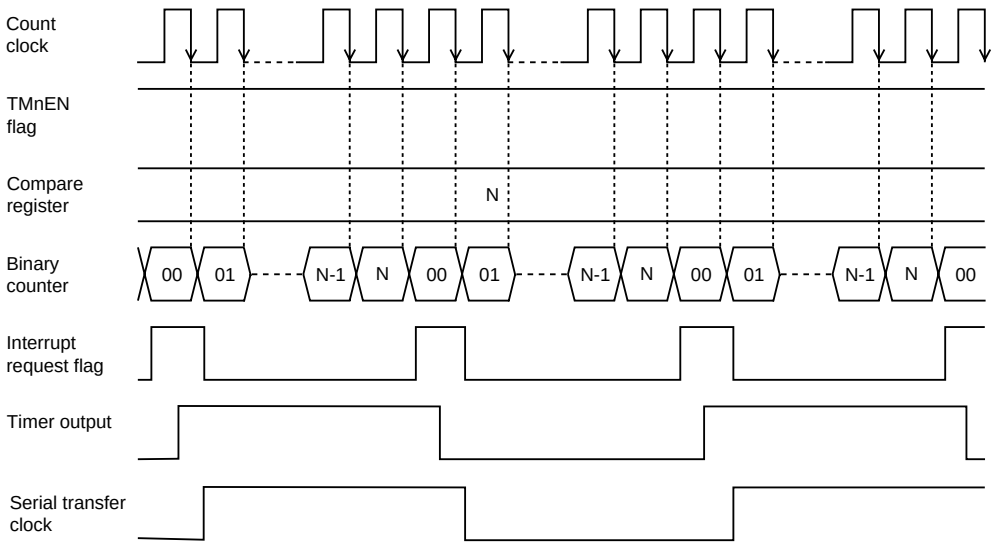


Figure 6-8-1 Timing of Serial Transfer Clock (Timer 3)

The timer output is synchronized to the serial transfer clock by the timer count clock, and its frequency is 1/2 of the set frequency set by the compare register.
Other count timings are same as the timing of timer operation. For the baud rate calculation and the serial interface setup, refer to chapter 11. Serial Interface 0 and chapter 12. Serial Interface 2.

6-8-2 Setup Example

■Serial Transfer Clock Setup Example (Timer 3)

How to create a transfer clock for half duplex UART (Serial 0) using with timer 3 is shown below. The baud rate is selected to be 300 bps, the source clock of timer 3 is selected to be fs/4 (at fosc=8 MHz). An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM3MD (x'3F5D') bp3 :TM3EN = 0	(1) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop timer 3 counting.
(2) Select the normal timer operation. TM3MD (x'3F5D') bp4 :TM3CAS = 0	(2) Set the TM3CAS flag flag of the TM3MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM3MD (x'3F5D') bp2-0 :TM3CK2-0 = 001	(3) Select the clock source to prescaler output by the TM3CK2-0 flag of the TM3MD register.
(4) Select the prescaler output and enable counting. CK3MD (x'3F5F') bp2-1 :TM3PSC1-0 = 01 bp0 :TM3BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(4) Select the prescaler output to fs/8 by the TM3PSC1-0, TM3BAS flag of the timer 3 prescaler selection register (CK3MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.
(5) Set the baud rate. TM3OC (x'3F5B') = x'67'	(5) Set the timer 3 compare register (TM3OC) such a value that baud rate comes to 300 bps. [☞ Chapter 11. Table 11-3-23] At that time, the timer 3 binary counter (TM3BC) is initialized to x'00'.
(6) Start the timer operation TM3MD (x'3F5D') bp3 :TM4EN = 1	(6) Set the TM3EN flag of the TM3MD register to "1" to start timer 3.

TM3BC counts up from x'00'. Timer 3 output is the clock of the serial interface 0 at transmission and reception.
For the compare register setup value and the serial operation setup, refer to chapter 11. Serial Interface 0.

6-9 Simple Pulse Width Measurement

6-9-1 Operation

Timer measures the "L" duration of the pulse signal input from the external interrupt pin.

■Simple Pulse Width Measurement Operation by 8-bit Timer (Timers 0, and 2)
When the input signal of the external interrupt pin (simple pulse width) is "L", the binary counter of the timer counts up. Pulse width "L" period can be measured by reading the count of timer. 8-bit timers that have the simple pulse width measurement function are timers 0, and 2.

Table 6-9-1 Simple Pulse Width Measurement Able Pins (Timers 0, and 2)

	Timer 0	Timer 2
Simple pulse width measurement enable pin	External interrupt 0 (P20/IRQ0)	External interrupt 2 (P22/IRQ2)

■Count Timing of Simple Pulse Width Measurement (Timer 0, Timer 2)

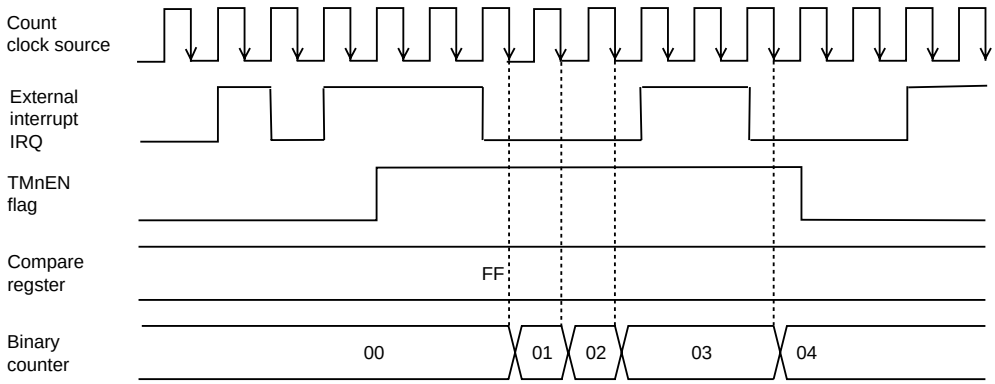


Figure 6-9-1 Count Timing at Measurement of Simple Pulse Width (Timer 0, Timer 2)

When the input signal of the external interrupt pin for simple pulse width measurement is "L" at TMnEN flag operation is ("1"), timer counts up.

6-9-2 Setup Example

■Set up Example of Simple Pulse Width Measurement by 8-bit Timer (Timers 0, and 2)
The pulse width of 'L" period of the external interrupt 0 (IRQ0) input signal is measured by timer 0. The clock source of timer 0 is selected to fosc.
A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to stop timer 0 counting.
(2) Set the pulse width measurement operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 1	(2) Set the TM0PWM flag of the TM0MD register to "0" and TM0MOD flag to "1" to enable the timer operation during "L" period to be measured.
(3) Select the count clock source. TM0MD (x'3F54') bp2-0 : TM0CK2-0 = 000	(3) Set the clock source to fosc by the TM0CK2-0 flag of the TM0MD register.
(4) Set the compare register. TM0OC (X'3F52') = x'FF'	(4) Set the timer 0 compare register (TM0OC) to the bigger value than the cycle of fosc / "L" period of measured pulse width. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(5) Set the interrupt level IRQ0ICR (x'3FE2') bp7-6 :IRQ0LV1-0 = 10	(5) Set the interrupt level by the IRQ0LV1-0 flag of the external interrupt 0 control register (IRQ0ICR). If interrupt request flag is already set, clear all interrupt request flags. [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]
(6) Set the interrupt valid edge. IRQ0ICR (x'3FE2') bp5 :REDG0 = 1	(6) Set the REDG0 flag of the IRQ0ICR register to "1" to specify the interrupt valid edge to the rising edge.

Setup Procedure	Description
(7) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 :IRQ0IE = 1	(7) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
(8) Enable the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to "1" to enable timer 0 operation.

TM0BC starts to count up with negative edge of the external interrupt 0 (IRQ0) input as a trigger. Timer 0 continues to count up during "L" period of IRQ0 input, then stop the counting with positive edge of IRQ0 input as a trigger. At the same time, reading the value of TM0BC by interrupt handling can detects "L" period.

6-10 Cascade Connection

6-10-1 Operation

Cascading timers 0 and 1, or timer 2 and 3 forms a 16-bit timer.

■8-bit Timer Cascade Connection Operation (Timer 0 + Timer 1, Timer 2 + Timer 3)
Timer 0 and timer 1, or timer 2 and timer 3 are combined to be a 16-bit timer. Cascading timer is operated at clock source of timer 0 or timer 2 which are lower 8 bits.

Table 6-10-1 Timer Functions at Cascade Connection

	Timer 0 + Timer 1 (16 bit)	Timer 2 + Timer 3 (16 bit)
Interrupt source	TM1IRQ	TM3IRQ
Timer operation	√	√
Event count	√ (TM0IO input)	√ (TM2IO input)
Timer pulse output	√ (TM1IO output)	√ (TM3IO output)
PWM output	-	-
Synchronous output	√	-
Serial transfer clock output	-	√ (TM3IO output)
Pulse width measurement	√	√
Remote control carrier output	-	√
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM2IO input
fosc : Machine clock (High frequency oscillation) fx : Machine clock (Low frequency oscillation) fs : System clock [☞Chapter 2 2-5 Clock Switching]		

At cascade connection, the binary counter and the compare register are operated as a 16 bit register. At operation, set the TMnEN flag of the upper and lower 8-bit timers to "1" to be operated. Also, select the clock source by the lower 8-bit timer.
Other setup and count timing is the same to the 8-bit timer at independently operation.

When timer 0 and timer 1 are used in cascade connection, timer 1 is used as an interrupt request flag. Timer pulse output of timer 0 is "L" fixed output.
An interrupt request of timer 0 is not generated, but the timer 0 interrupt should be disabled.

When timer 2 and timer 3 are used in cascade connection, timer 3 is used as an interrupt request flag. Timer pulse output of timer 2 is "L" fixed output.
An interrupt request of timer 2 is not generated, but the timer 2 interrupt should be disabled.

6-10-2 Setup Example

■Cascade Connection Timer Setup Example (Timer 0 + Timer 1, Timer 2 + Timer 3)
Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 0 and timer 1, as a 16-bit timer is shown. An interrupt is generated 2500 times every 1 ms by selecting source clock to fs/4 (fosx=20 MHz at operation).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0 TM1MD (x'3F55') bp3 :TM1EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0", the TM1EN flag of the timer 1 mode register to "0" to stop timer 0 and timer 1 counting.
(2) Select the normal lower timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(2) Set both of the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer 0 operation.
(3) Set the cascade connection. TM1MD (x'3F55') bp4 :TM1CAS = 1	(3) Set the TM1CAS flag of the TM1MD register to "1" to connect timer 1 and timer 0 in cascade connection.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 001	(4) Set the clock source to prescaler output by the TM0CK2-0 flag of the TM0MD register.
(5) Select the prescaler output and enable counting. CK0MD (x'3F56') bp2-1 :TM0PSC1-0= 01 bp0 :TM0BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(5) Set the prescaler output to fs/4 by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.
(6) Set the interrupt generation cycle. TMnOC(x'3F53', x'3F52')=x'09C3'	(6) Set the timer 1 compare register + timer 0 compare register (TM1OC + TM0OC) to the interrupt generation cycle (x'09C3' : 2500 cycles - 1). At that time, timer 1 binary counter + timer 0 binary counter (TM1BC + TM0BC) are initialized to x'0000'.

Setup Procedure	Description
(7) Disable the lower timer interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 0	(7) Set the TM0IE flag of the timer 0 interrupt control register (TM0ICR) to "0" to disable the interrupt.
(8) Set the level of the upper timer interrupt. TM1ICR (x'3FEA') bp7-6 :TM1LV1-0 = 10	(8) Set the interrupt level by the TM1LV1-0 flag of the timer 1 interrupt control register (TM1ICR). If any interrupt request flag may be already set, clear all request flags. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the upper timer interrupt. TM1ICR (x'3FEA') bp1 :TM1IE = 1	(9) Set the TM1IE flag of the TM1ICR register to "1" to enable the interrupt.
(10) Start the upper timer operation. TM1MD (x'3F55') bp3 :TM1EN = 1	(10) Set the TM1EN flag of the TM1MD register to "1" to start timer 1.
(11) Start the lower timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(11) Set the TM0EN flag of the TM0MD register to "1" to start timer 0.

TM1BC + TM0BC counts up from x'0000' as a 16-bit timer. When TM1BC + TM0BC reaches the set value of TM1OC + TM0OC register, the timer 1 interrupt request flag is set at the next count clock, and the value of TM1BC + TM0BC becomes x'0000' and restarts count up.

Use a 16-bit access instruction to set the (TM1OC + TM0OC) register.

Start the upper timer operation before the lower timer operation.

6-11 Remote Control Carrier Output

6-11-1 Operation

Carrier pulse for remote control can be generated.

■Operation of Remote Control Carrier Output (Timer 0, Timer 3)
Remote control carrier pulse is generated with output signal of timer 0 or timer 3. Duty rate is selected from 1/2, 1/3. RMOUT (P10) outputs remote control carrier output signal.

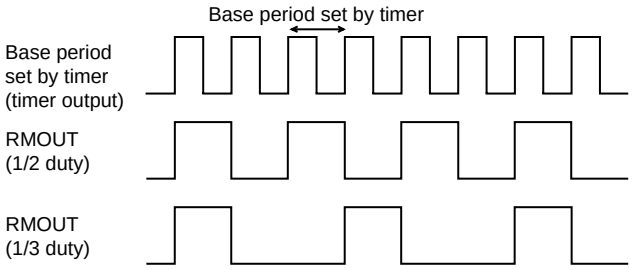


Figure 6-11-1 Duty Rate of Remote Control Carrier Output Signal

■Count Timing of Remote Control Carrier Output (Timer 0, Timer 3)

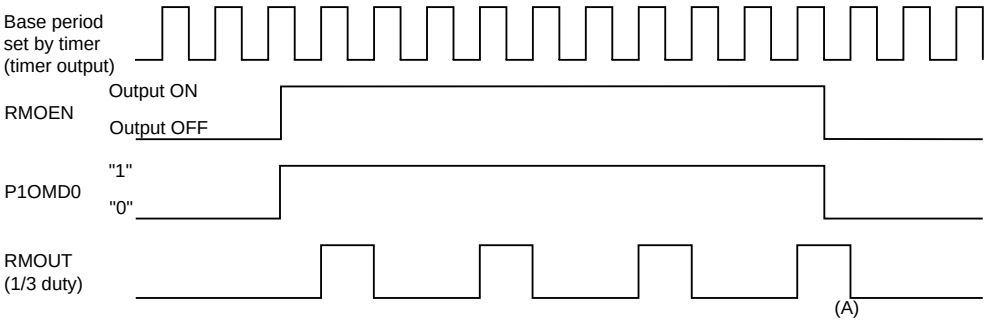


Figure 6-11-2 Count Timing of Remote Control Carrier Output Function (Timer 0, Timer 3)

(A) Even if the RMOEN flag is off when the carrier output is high, the carrier waveform is held by the synchronous circuit.

When the RMOEN flag is switched to on, set the P1OMD0 flag to "1". When it is switched to off, set it to "0".

When the RMOEN flag is changed, do not change the base cycle and its duty at the same time. If they are changed at the same time, the carrier wave form is not output properly.

6-11-2 Setup Example

■Remote Control Carrier Output Setup Example (Timer 0, Timer 3)
Here is the setting example that the RMOUT pin outputs the 1/3 duty carrier pulse signal with "H" period of 36.7 kHz, by using timer 0. The source clock of timer 0 is set to fosc (8 MHz at operation).
An example setup procedure, with a description of each step is shown below.

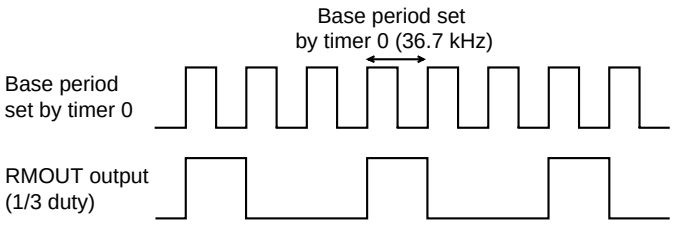


Figure 6-11-3 Output Wave Form of RMOUT Output Pin

Setup Procedure	Description
(1) Disable the remote control carrier output. RMCTR (x'3F6E') bp3 : RMOEN = 0	(1) Set the RMOEN flag of the remote control carrier output control register (RMCTR) to "0" to disable the remote control carrier output.
(2) Select the base cycle setting timer. RMCTR (x'3F6E') bp0 : RMBTMS = 0	(2) Set the RMBTMS flag of the RMCTR register to "0" to set the timer as a base cycle setting timer.
(3) Select the carrier output duty. RMCTR (x'3F6E') bp1 : RMDTY0 = 1	(3) Set the RMDTY0 flag of the RMCTR register to "1" to select 1/3 duty.
(4) Stop the counter. TM0MD (x'3F54') bp3 : TM0EN = 0	(4) Set the TM0EN flag of the timer 0 mode register (TM0MD) to stop the timer 0 counting.
(5) Set the remote control carrier output of the special function pin. P1OMD (x'3F2F') bp0 : P1OMD0 = 1 P1DIR (x'3F31') bp0 : P1DIR0 = 1 RMCTR (x'3F6E') bp4 :TM0RM = 1	(5) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin as a special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for output mode. Set the TM0RM flag of the RMCTR register to "1" to select the remote control carrier output.

Setup Procedure	Description
(6) Select the normal timer operation. TM0MD (x'3F54') bp4 : TM0PWM = 0 bp5 : TM0MOD = 0	(6) Set both of the TM0MOD flag and TM0PWM flag of the TM0MD register to "0" to select normal timer operation.
(7) Select the count clock source. TM0MD (x'3F54') bp2-0 : TM0CK2-0 = 000	(7) Select fosc to clock source by the TM0CK2-0 flag of the TM0MD register.
(8) Set the base cycle of remote control carrier. TM0OC (x'3F52') = x'6C'	(8) Set the base cycle of remote control carrier by writing x'6C' to the timer 0 compare register (TM0OC). The set value should be (8 MHz/ 73.4 kHz) - 1 = 108(x'6C') 8 MHz is divided to be 73.4 kHz, 2 times 36.7 kHz.
(9) Start the timer operation. TM0MD (x'3F54') bp3 : TM0EN = 1	(9) Set the TM0EN flag of the TM0MD register to "1" to stop the timer 0 counting.
(10) Enable the remote control carrier output. RMCTR (x'3F6E') bp3 : RMOEN = 1	(10) Set the RMOEN flag of the RMCTR register to "1" to enable the remote control carrier output.

TM0BC counts up from x'00'. Timer 0 outputs the base cycle pulse set in TM0OC. Then, the 1/3 duty remote control carrier pulse signal is output. If the RMOEN flag of the RMCTR register is "0", the remote control carrier pulse signal output is stopped.

Chapter 7 16-bit Timers

7

7-1 Overview

This LSI contains two general-purpose 16-bit timers (Timer 7,Timer 8). The 16-bit timer has compare register with double buffer. High precision 16-bit timer has 2 sets of compare registers with double buffering.

7-1-1 Functions

Table 7-1-1 shows the functions of timer 7 and timer 8.

Table 7-1-1 16-bit Timer Functions

	Timer 7	Timer 8
Interrupt source	TM7IRQ1, TM7IRQ2	TM8IRQ1, TM8IRQ2
Timer operation	√	√
Event count	√ (Edge selectable)	√ (Edge selectable)
Timer pulse output	√	√
PWM output (duty is changeable)	√	√
High precision PWM output (duty and cycle are changeable)	√	√
IGBT output (duty is changeable)	√	–
High precision IGBT output (duty and cycle are changeable)	√	–
Synchronous output	√	–
Capture function	√	√
Pulse width measurement	√	√
32-bit cascade connection (Timer cycle, Event count. Standard PWM output, High precision PWM output capture)	√	
Clock source	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16	fosc fosc/2 fosc/4 fosc/16 fosc/128 fs fs/2 fs/4 fs/16 fs/128 TM8IO input TM8IO input/2 TM8IO input/4 TM8IO input/16 TM8IO input/128
fosc : Machine clock (High frequency oscillation) fx: : Machine clock (Low frequency oscillation) fs : System clock [☞ Chapter 2 2-5 Clock Switching]		

7-1-2 Block Diagram

■Timer 7 Block Diagram

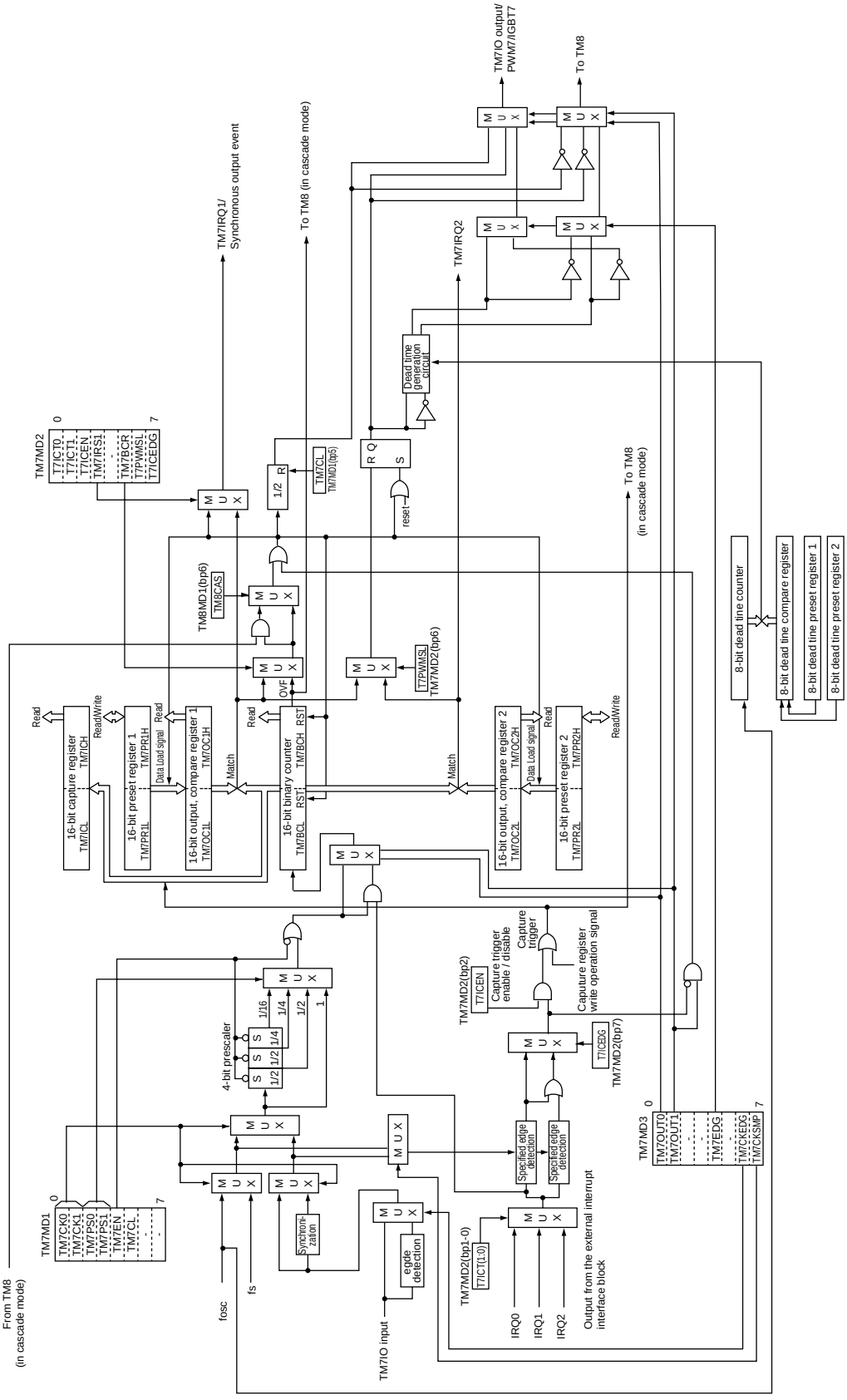


Figure 7-1-1 Timer 7 Block Diagram

■Timer 8 Block Diagram

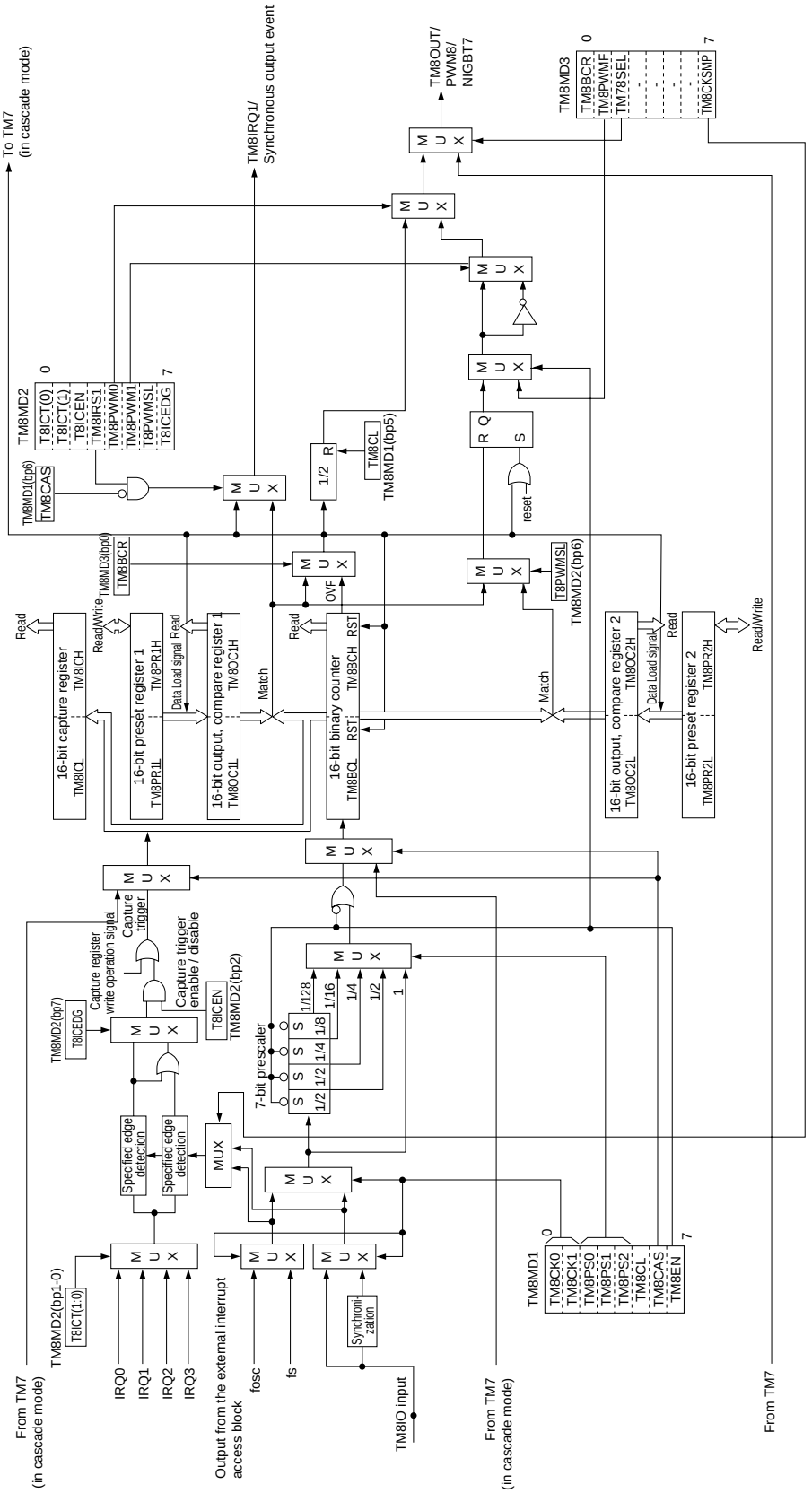


Figure 7-1-2 Timer 8 Block Diagram

7-2 Control Registers

Timer 7 contains the binary counter (TM7BC), the compare register 1 (TM7OC1) with its double buffer preset register 1 (TM7PR1), the compare register 2 (TM7OC2) with its double buffer preset register 2 (TM7PR2), the input capture register (TM7IC) and the dead time preset register 1 (TM7DEADPR1), the dead time preset register 2 (TM7DEADPR2). The mode register 1 (TM7MD1), the mode register 2 (TM7MD2) and the mode register 3 (TM7MD3) control timer 7. Timer 8 contains the binary counter (TM8BC), the compare register 1 (TM8OC1) with its double buffer preset register 1 (TM8PR1), the compare register 2 (TM8OC2) with its double buffer preset register 2 (TM8PR2), and the input capture register (TM8IC). The mode register 1 (TM8MD1), the mode register 2 (TM8MD2) and the mode register 3 (TM8MD3) control timer 8.

7-2-1 Registers

Table 7-2-1 shows the registers that control timer 7.

Table 7-2-1 16-bit Timer Control Registers(1/2)

	Register	Address	R/W	Function	Page
Timer 7	TM7BCL	x'03F70'	R	Timer 7 binary counter (lower 8 bits)	VII - 11
	TM7BCH	x'03F71'	R	Timer 7 binary counter (upper 8 bits)	VII - 11
	TM7OC1L	x'03F72'	R	Timer 7 compare register 1 (lower 8 bits)	VII - 7
	TM7OC1H	x'03F73'	R	Timer 7 compare register 1 (upper 8 bits)	VII - 7
	TM7PR1L	x'03F74'	R/W	Timer 7 preset register 1 (lower 8 bits)	VII - 9
	TM7PR1H	x'03F75'	R/W	Timer 7 preset register 1 (upper 8 bits)	VII - 9
	TM7ICL	x'03F76'	R	Timer 7 input capture regsiter (lower 8 bits)	VII - 12
	TM7ICH	x'03F77'	R	Timer 7 input capture register (upper 8 bits)	VII - 12
	TM7MD1	x'03F78'	R/W	Timer 7 mode register 1	VII - 13
	TM7MD2	x'03F79'	R/W	Timer 7 mode register 2	VII - 14
	TM7MD3	x'03F6C'	R/W	Timer 7 mode register 3	VII - 15
	TM7OC2L	x'03F7A'	R	Timer 7 compare register 2 (lower 8 bits)	VII - 7
	TM7OC2H	x'03F7B'	R	Timer 7 compare register 2 (upper 8 bits)	VII - 7
	TM7PR2L	x'03F7C'	R/W	Timer 7 preset register 2 (lower 8 bits)	VII - 9
	TM7PR2H	x'03F7D'	R/W	Timer 7 preset register 2 (upper 8 bits)	VII - 9
	TM7DEADPR1	x'03F7E'	R/W	Timer 7 Dead time Preset register	VII - 12
	TM7DEADPR2	x'03F7F'	R/W	Timer 7 Dead time Preset register	VII - 13
	TM7ICR	x'03FF1'	R/W	Timer 7 interrupt control register	III - 32
	T7OC2ICR	x'03FF2'	R/W	Timer 7 compare register 2 match interrupt control register	III - 33
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 15
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 14

R/W : Readable/Writable
R : Readable only

Table 7-2-1 16-bit Timer Control Registers(2/2)

	Register	Address	R/W	Function	Page
Timer 8	TM8BCL	x'03F80'	R	Timer 8 binary counter (lower 8 bits)	VII - 11
	TM8BCH	x'03F81'	R	Timer 8 binary counter (upper 8 bits)	VII - 11
	TM8OC1L	x'03F82'	R	Timer 8 compare register 1 (lower 8 bits)	VII - 8
	TM8OC1H	x'03F83'	R	Timer 8 compare register 1 (upper 8 bits)	VII - 8
	TM8PR1L	x'03F84'	R/W	Timer 8 preset register 1 (lower 8 bits)	VII - 10
	TM8PR1H	x'03F85'	R/W	Timer 8 preset register 1 (upper 8 bits)	VII - 10
	TM8ICL	x'03F86'	R	Timer 8 input capture regsiter (lower 8 bits)	VII - 12
	TM8ICH	x'03F87'	R	Timer 8 input capture register (upper 8 bits)	VII - 12
	TM8MD1	x'03F88'	R/W	Timer 8 mode register 1	VII - 16
	TM8MD2	x'03F89'	R/W	Timer 8 mode register 2	VII - 17
	TM8MD3	x'03F6D'	R/W	Timer 8 mode register 3	VII - 18
	TM8OC2L	x'03F8A'	R	Timer 8 compare register 2 (lower 8 bits)	VII - 8
	TM8OC2H	x'03F8B'	R	Timer 8 compare register 2 (upper 8 bits)	VII - 8
	TM8PR2L	x'03F8C'	R/W	Timer 8 preset register 2 (lower 8 bits)	VII - 10
	TM8PR2H	x'03F8D'	R/W	Timer 8 preset register 2 (upper 8 bits)	VII - 10
	TM8ICR	x'03FF3'	R/W	Timer 8 interrupt control register	III - 34
	T8OC2ICR	x'03FF4'	R/W	Timer 8 compare register 2 match interrupt control register	III - 35
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 15
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 14

R/W : Readable/Writable

R : Readable only

7-2-2 Programmable Timer Registers

Timer 7 and Timer 8 each have a set of 16-bit programmable timer registers, which contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate these registers by 16-bit access.

A compare register is a 16-bit register which stores comparative value of compare register and binary counter. Comparative value written to the preset register in advance is loaded to the register.

■Timer 7 Compare Register 1 (TM7OC1)

	7	6	5	4	3	2	1	0	
TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	(At reset : X X X X X X X X)

Figure 7-2-1 Timer 7 Compare Register 1 Lower 8 bits (TM7OC1L : x'03F72', R)

	7	6	5	4	3	2	1	0	
TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	(At reset : X X X X X X X X)

Figure 7-2-2 Timer 7 Compare Register 1 Upper 8 bits (TM7OC1H : x'03F73', R)

■Timer 7 Compare Register 2 (TM7OC2)

	7	6	5	4	3	2	1	0	
TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	(At reset : X X X X X X X X)

Figure 7-2-3 Timer 7 Compare Register 2 Lower 8 bits (TM7OC2L : x'03F7A', R)

	7	6	5	4	3	2	1	0	
TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	(At reset : X X X X X X X X)

Figure 7-2-4 Timer 7 Compare Register 2 Upper 8 bits (TM7OC2H : x'03F7B', R)

■Timer 8 Compare Register 1 (TM8OC1)

	7	6	5	4	3	2	1	0	
TM8OC1L	TM8OC1L7	TM8OC1L6	TM8OC1L5	TM8OC1L4	TM8OC1L3	TM8OC1L2	TM8OC1L1	TM8OC1L0	(At reset : X X X X X X X X)

Figure 7-2-5 Timer 8 Compare Register 1 Lower 8 bits (TM8OC1L : x'03F82', R)

	7	6	5	4	3	2	1	0	
TM8OC1H	TM8OC1H7	TM8OC1H6	TM8OC1H5	TM8OC1H4	TM8OC1H3	TM8OC1H2	TM8OC1H1	TM8OC1H0	(At reset : X X X X X X X X)

Figure 7-2-6 Timer 8 Compare Register 1 Upper 8 bits (TM8OC1H : x'03F83', R)

■Timer 8 Compare Register 2 (TM8OC2)

	7	6	5	4	3	2	1	0	
TM8OC2L	TM8OC2L7	TM8OC2L6	TM8OC2L5	TM8OC2L4	TM8OC2L3	TM8OC2L2	TM8OC2L1	TM8OC2L0	(At reset : X X X X X X X X)

Figure 7-2-7 Timer 8 Compare Register 2 Lower 8 bits (TM8OC2L : x'03F8A', R)

	7	6	5	4	3	2	1	0	
TM8OC2H	TM8OC2H7	TM8OC2H6	TM8OC2H5	TM8OC2H4	TM8OC2H3	TM8OC2H2	TM8OC2H1	TM8OC2H0	(At reset : X X X X X X X X)

Figure 7-2-8 Timer 8 Compare Register 2 Upper 8 bits (TM8OC2H : x'03F8B', R)

The timer7 and timer 8 preset registers 1 and 2 are buffer registers of the compare registers 1, 2 of timer 7 and 8. If the set value is written to the timer 7 and timer 8 preset registers 1, 2 when the counting is stopped, the same set value is loaded to timer 7 and timer 8 compare registers 1, 2. If the set value is written to timer 7 and timer 8 preset registers 1, 2 during counting, the set value of timer 7 and timer 8 preset registers 1, 2 is loaded to timer 7 and timer 8 compare registers 1, 2 at the timing that the timer 7 and timer 8 binary counters are cleared.
Write data to the preset register in 16-bit unit by MOVW instruction.

■Timer 7 Preset Register 1 (TM7PR1)

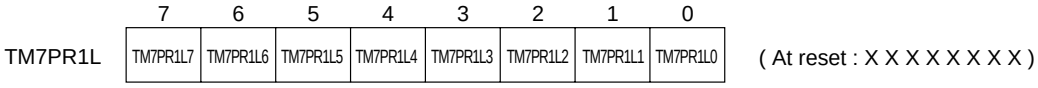


Figure 7-2-9 Timer 7 Preset Register 1 Lower 8 bits (TM7PR1L : x'03F74', R/W)

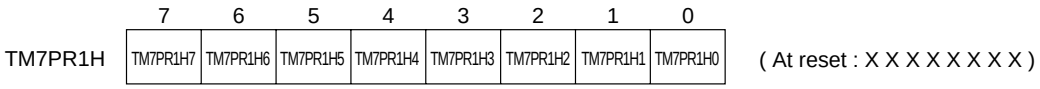


Figure 7-2-10 Timer 7 Preset Register 1 Upper 8 bits (TM7PR1H : x'03F75', R/W)

■Timer 7 Preset Register 2 (TM7PR2)

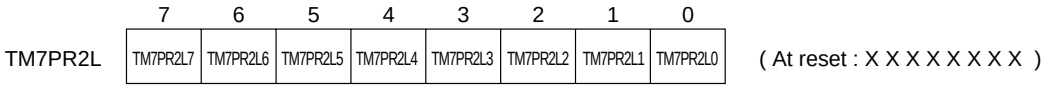


Figure 7-2-11 Timer 7 Preset Register 2 Lower 8 bits (TM7PR2L : x'03F7C', R/W)

Figure 7-2-12 Timer 7 Preset Register 2 Upper 8 bits (TM7PR2H : x'03F7D', R/W)

■Timer 8 Preset Register 1 (TM8PR1)

	7	6	5	4	3	2	1	0	
TM8PR1L	TM8PR1L7	TM8PR1L6	TM8PR1L5	TM8PR1L4	TM8PR13L	TM8PR1L2	TM8PR1L1	TM8PR1L0	(At reset : X X X X X X X X)

Figure 7-2-13 Timer 8 Preset Register 1 Lower 8 bits (TM8PR1L : x'03F84', R/W)

	7	6	5	4	3	2	1	0	
TM8PR1H	TM8PR1H7	TM8PR1H6	TM8PR1H5	TM8PR1H4	TM8PR1H3	TM8PR1H2	TM8PR1H1	TM8PR1H0	(At reset : X X X X X X X X)

Figure 7-2-14 Timer 8 Preset Register 1 Upper 8 bits (TM8PR1H : x'03F85', R/W)

■Timer 8 Preset Register 2 (TM8PR2)

	7	6	5	4	3	2	1	0	
TM8PR2L	TM8PR2L7	TM8PR2L6	TM8PR2L5	TM8PR2L4	TM8PR2L3	TM8PR2L2	TM8PR2L1	TM8PR2L0	(At reset : X X X X X X X X)

Figure 7-2-15 Timer 7 Preset Register 2 Lower 8 bits (TM8PR2L : x'03F8C', R/W)

	7	6	5	4	3	2	1	0	
TM8PR2H	TM8PR2H7	TM8PR2H6	TM8PR2H5	TM8PR2H4	TM8PR2H3	TM8PR2H2	TM8PR2H1	TM8PR2H0	(At reset : X X X X X X X X)

Figure 7-2-16 Timer 8 Preset Register 2 Upper 8 bits (TM8PR2H : x'03F8D', R/W)

Binary counter is a 16-bit up counter. If any data is written to a preset register when the counting is stopped, the binary counter is cleared to x'0000'.

■Timer 7 Binary Counter (TM7BC)

	7	6	5	4	3	2	1	0	
TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	(At reset : X X X X X X X X)

Figure 7-2-17 Timer 7 Binary Counter Lower 8 bits (TM7BCL : x'03F70', R)

	7	6	5	4	3	2	1	0	
TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	(At reset : X X X X X X X X)

Figure 7-2-18 Timer 7 Binary Counter Upper 8 bits (TM7BCH : x'03F71', R)

■Timer 8 Binary Counter (TM8BC)

	7	6	5	4	3	2	1	0	
TM8BCL	TM8BCL7	TM8BCL6	TM8BCL5	TM8BCL4	TM8BCL3	TM8BCL2	TM8BCL1	TM8BCL0	(At reset : X X X X X X X X)

Figure 7-2-19 Timer 8 Binary Counter Lower 8 bits (TM8BCL : x'03F80', R)

	7	6	5	4	3	2	1	0	
TM8BCH	TM8BCH7	TM8BCH6	TM8BCH5	TM8BCH4	TM8BCH3	TM8BCH2	TM8BCH1	TM8BCH0	(At reset : X X X X X X X X)

Figure 7-2-20 Timer 8 Binary Counter Upper 8 bits (TM8BCH : x'03F81', R)

Input capture register is a register that holds the value loaded from a binary counter by a capture trigger. A capture trigger is generated by an input signal from an external interrupt pin, and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disabled.).

■Timer 7 Input Capture Register (TM7IC)

	7	6	5	4	3	2	1	0	
TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	(At reset : X X X X X X X X)

Figure 7-2-21 Timer 7 Input Capture Register Lower 8 bits (TM7ICL : x'03F76', R)

	7	6	5	4	3	2	1	0	
TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	(At reset : X X X X X X X X)

Figure 7-2-22 Timer 7 Input Capture Register Upper 8 bits (TM7ICH : x'03F77', R)

■Timer 8 Input Capture Register (TM8IC)

	7	6	5	4	3	2	1	0	
TM8ICL	TM8ICL7	TM8ICL6	TM8ICL5	TM8ICL4	TM8ICL3	TM8ICL2	TM8ICL1	TM8ICL0	(At reset : X X X X X X X X)

Figure 7-2-23 Timer 8 Input Capture Register Lower 8 bits (TM8ICL : x'03F86', R)

	7	6	5	4	3	2	1	0	
TM8ICH	TM8ICH7	TM8ICH6	TM8ICH5	TM8ICH4	TM8ICH3	TM8ICH2	TM8ICH1	TM8ICH0	(At reset : X X X X X X X X)

Figure 7-2-24 Timer 8 Input Capture Register Upper 8 bits (TM8ICH : x'03F87', R)

Timer 7 dead timer preset register 1 and 2 are 8-bit registers that set the dead time, and are enabled only when the IGBT control output function with dead time is used. When falling edge is selected as a standard edge, write the period between falling of TM8IO and rising of TM7IO to the timer 7 dead time register 1 and write the period between falling of TM7IO and rising of TM8IO to the timer 7 dead time register 2 to set the dead time.
If data is written while counting is halted, the value of the timer 7 dead time preset register 1 is loaded into the dead time circuit. And if data is written during counting, TM70C1 or TM70C2 compare matching is occurred. In correspond to these matching, data of the timer 7 dead time preset register 1 or 2 is loaded to the dead time generation circuit.

■Timer 7 Dead Time Preset Register (TM7DEADPR1)

	7	6	5	4	3	2	1	0	
TM7DEADPR1	TM7DEADPR17	TM7DEADPR16	TM7DEADPR15	TM7DEADPR14	TM7DEADPR13	TM7DEADPR12	TM7DEADPR11	TM7DEADPR10	(At reset : 0 0 0 0 0 0 0 0)

Figure 7-2-25 Timer 7 Dead Time Preset Register 1 (TM7DEADPR1 : x'03F7E', W/R)

■Timer 7 Dead Time Preset Register 2 (TM7DEADPR2)

	7	6	5	4	3	2	1	0	
TM7DEADPR2	TM7DEADPR27	TM7DEADPR26	TM7DEADPR25	TM7DEADPR24	TM7DEADPR23	TM7DEADPR22	TM7DEADPR21	TM7DEADPR20	(At reset : 0 0 0 0 0 0 0 0)

Figure 7-2-26 Timer 7 Dead Time Preset Register 2 (TM7DEADPR2 : x'03F7F', W/R)

7-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 7.

■Timer 7 Mode Register 1 (TM7MD1)

	7	6	5	4	3	2	1	0	
TM7MD1	RESERVED	RESERVED	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0	(At reset : 0 0 1 0 0 0 0 0)

TM7CK1	TM7CK0	Clock source selection
0	0	fosc
	1	fs
1	0	TM7IO input
	1	Synchronous TM7IO input

TM7PS1	TM7PS0	Count clock selection
0	0	1/1 of clock
	1	1/2 of clock
1	0	1/4 of clock
	1	1/16 of clock

TM7EN	Timer 7 count control
0	Halt the count
1	Operate the count

TM7CL	Timer output reset control
0	Operate timer output
1	Disable timer output (reset)

RESERVED	Set always "0".

Figure 7-2-27 Timer 7 Mode Register 1 (TM7MD1 : x'03F78', R/W)

■Timer 7 Mode Register 2 (TM7MD2)

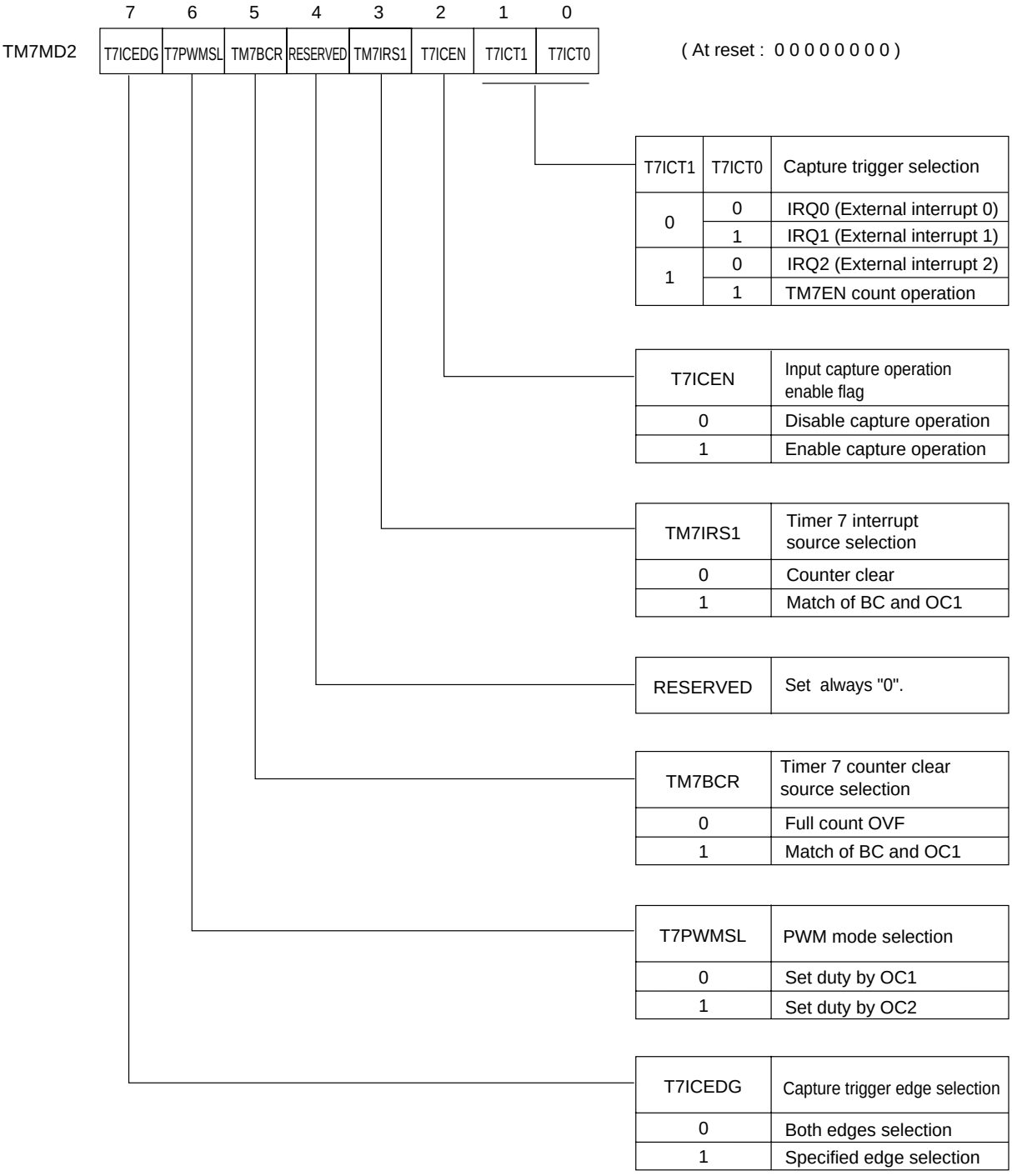

7 6 5 4 3 2 1 0
TM7MD2
T7ICEDG T7PWMSL TM7BCR RESERVED TM7IRS1 T7ICEN T7ICT1 T7ICT0
(At reset : 0 0 0 0 0 0 0 0)
T7ICT1 T7ICT0 Capture trigger selection
0 0 IRQ0 (External interrupt 0)
1 IRQ1 (External interrupt 1)
1 0 IRQ2 (External interrupt 2)
1 TM7EN count operation
T7ICEN Input capture operation enable flag
0 Disable capture operation
1 Enable capture operation
TM7IRS1 Timer 7 interrupt source selection
0 Counter clear
1 Match of BC and OC1
RESERVED Set always "0".
TM7BCR Timer 7 counter clear source selection
0 Full count OVF
1 Match of BC and OC1
T7PWMSL PWM mode selection
0 Set duty by OC1
1 Set duty by OC2
T7ICEDG Capture trigger edge selection
0 Both edges selection
1 Specified edge selection

Figure 7-2-28 Timer 7 Mode Register 2 (TM7MD2 : x'03F79', R/W)

■Timer 7 Mode Register 3 (TM7MD3)

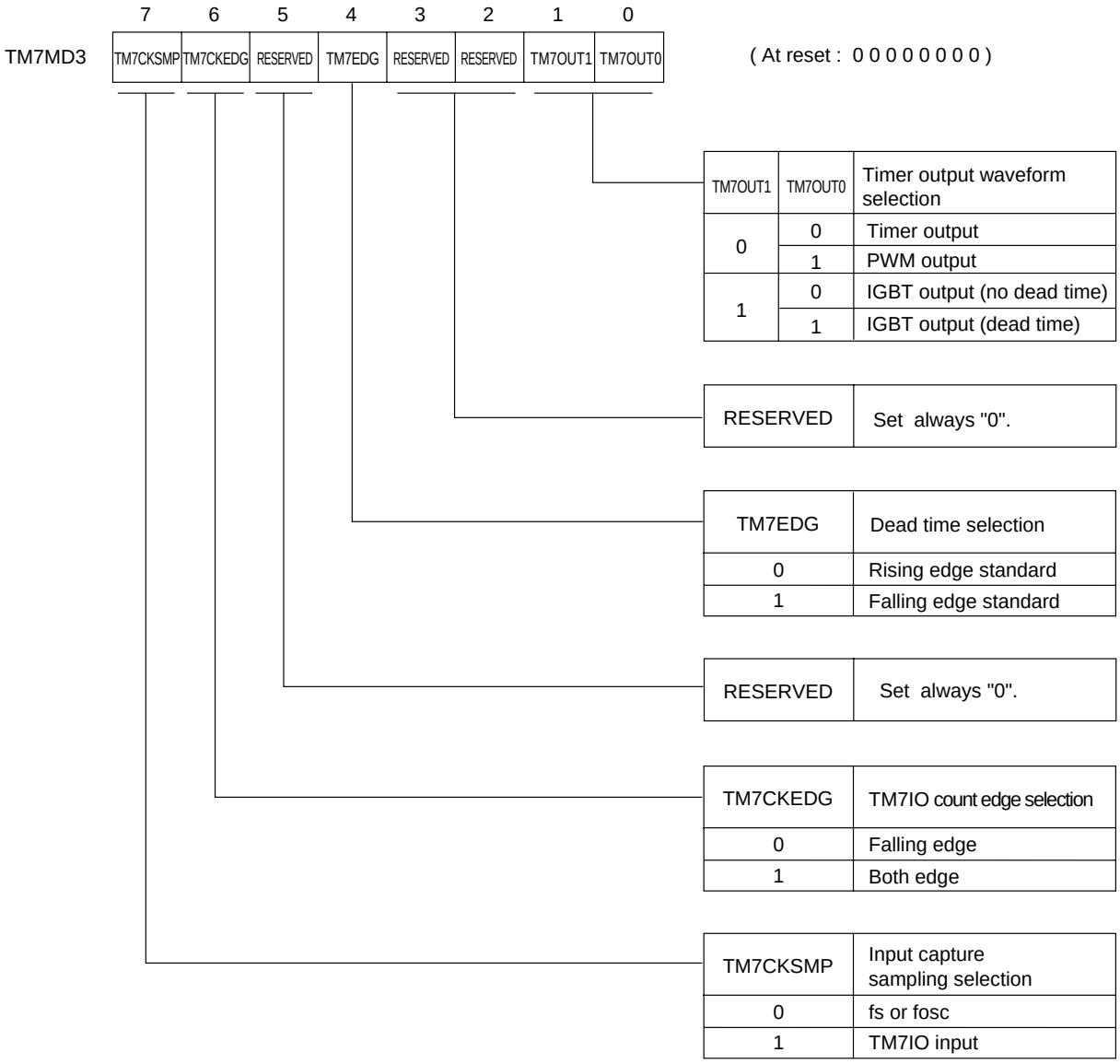

7 6 5 4 3 2 1 0
TM7MD3
TM7CKSMP TM7CKEDG RESERVED TM7EDG RESERVED RESERVED TM7OUT1 TM7OUT0
(At reset : 0 0 0 0 0 0 0 0)
TM7OUT1 TM7OUT0 Timer output waveform selection
0 0 Timer output
1 PWM output
1 0 IGBT output (no dead time)
1 IGBT output (dead time)
RESERVED Set always "0".
TM7EDG Dead time selection
0 Rising edge standard
1 Falling edge standard
RESERVED Set always "0".
TM7CKEDG TM7IO count edge selection
0 Falling edge
1 Both edge
TM7CKSMP Input capture sampling selection
0 fs or fosc
1 TM7IO input

Figure 7-2-29 Timer 7 Mode Register 3 (TM7MD3 : x'03F6C', R/W)

■Timer 8 Mode Register 1 (TM8MD1)

	7	6	5	4	3	2	1	0
TM8MD1	TM8EN	TM8CAS	TM8CL	TM8PS2	TM8PS1	TM8PS0	TM8CK1	TM8CK0

(At reset : 0 0 1 0 0 0 0 0)

TM8CK1	TM8CK0	Clock source selection
0	0	fosc
	1	fs
1	0	TM8IO input
	1	Synchronous TM8IO input

TM8PS2	TM8PS1	TM8PS0	Count clock selection
0	0	0	1/1 clock
		1	1/2 clock
	1	0	1/4 clock
		1	1/16 clock
1	0	0	1/128 clock

TM8CL	Timer output reset control
0	Operate timer output
1	Reset

TM8CAS	Timer 7, 8 cascade connection control
0	Timer 7, 8 singularity operation
1	Timer 7, 8 cascade connection operation

TM8EN	Timer 8 count control
0	Halt
1	Operation

Figure 7-2-30 Timer 8 Mode Register 1 (TM8MD1 : x'03F88', R/W)

■Timer 8 Mode Register 2 (TM8MD2)

	7	6	5	4	3	2	1	0
TM8MD2	T8ICEDG	T8PWMSL	TM8PWM1	TM8PWM0	TM8IRS1	T8ICEN	T8ICT1	T8ICT0

(At reset : 0 0 0 0 0 0 0 0)

T8ICT1	T8ICT0	Capture trigger selection
0	0	IRQ0 (External interrupt 0)
	1	IRQ1 (External interrupt 1)
1	0	IRQ2 (External interrupt 2)
	1	IRQ3 (External interrupt 3)

T8ICEN	Input capture operation enable flag
0	Disable capture operation
1	Enable capture operation

TM8IRS1	Timer 8 interrupt source selection
0	Counter clear
1	Match of BC and OC1

TM8PWM0	Timer output waveform selection
0	Timer output
1	PWM output

TM8PWM1	PWM waveform selection
0	Normal PWM output
1	Converted PWM output

T8PWMSL	PWM mode selection
0	Set duty by OC1
1	Set duty by OC2

T8ICEDG	Capture trigger edge selection
0	Both edges
1	Specified edge

Figure 7-2-31 Timer 8 Mode Register 2 (TM8MD2 : x'03F89', R/W)

■Timer 8 Mode Register 3 (TM8MD3)

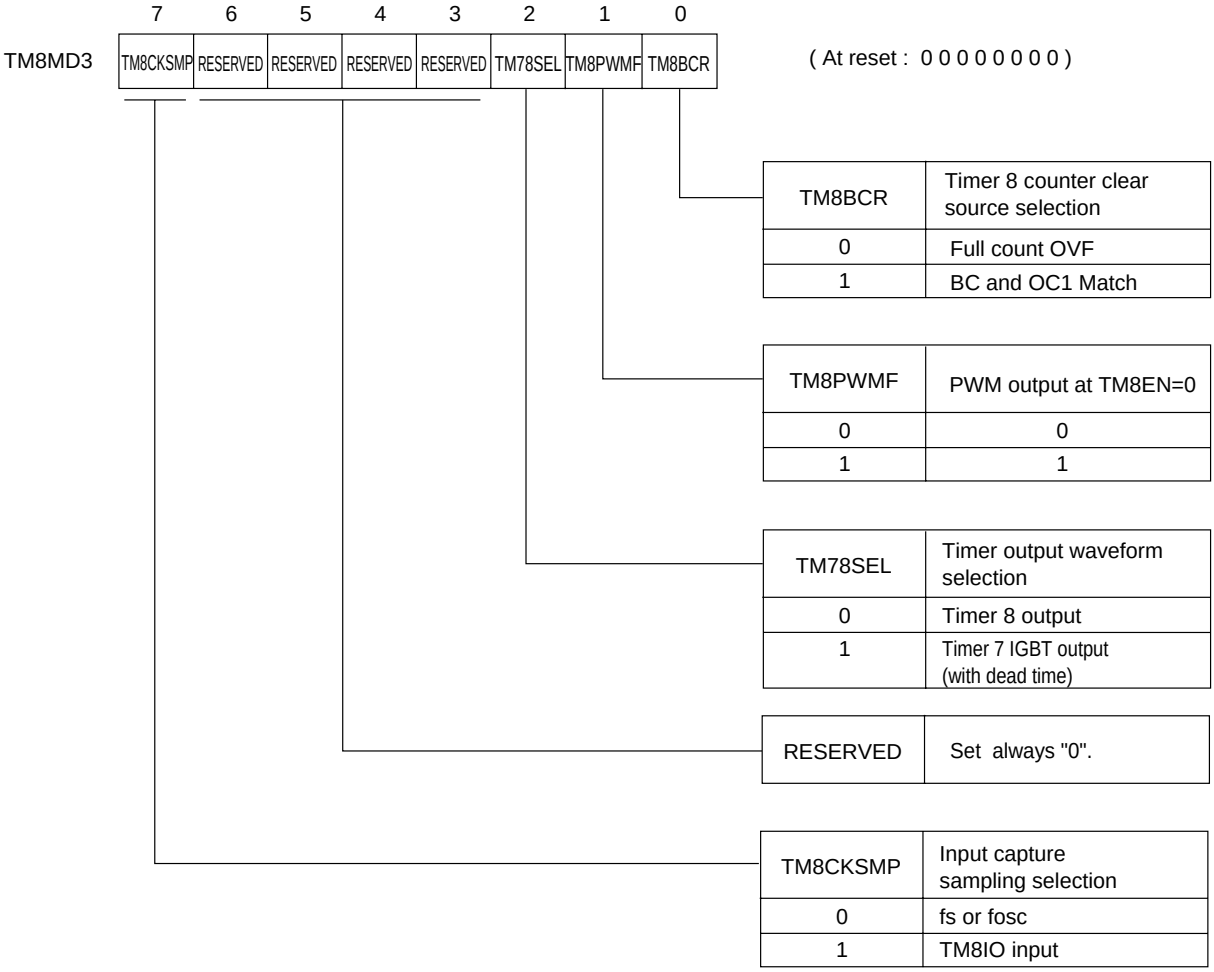

7 6 5 4 3 2 1 0
TM8MD3
TM8CKSMP RESERVED RESERVED RESERVED RESERVED TM78SEL TM8PWMF TM8BCR
(At reset : 0 0 0 0 0 0 0 0)
TM8BCR | Timer 8 counter clear source selection
0 | Full count OVF
1 | BC and OC1 Match
TM8PWMF | PWM output at TM8EN=0
0 | 0
1 | 1
TM78SEL | Timer output waveform selection
0 | Timer 8 output
1 | Timer 7 IGBT output (with dead time)
RESERVED | Set always "0".
TM8CKSMP | Input capture sampling selection
0 | fs or fosc
1 | TM8IO input

Figure 7-2-32 Timer8 Mode Register 3 (TM8MD3 : x'03F6D', R/W)

7-3 Operation

7-3-1 Operation

The timer operation can constantly generate interrupts.

■16-bit Timer Operation (Timer 7,Timer 8)
The generation cycle of an timer interrupt is set by the clock source selection and the set value of the compare register 1 (TMnOC1), in advance. When the binary counter (TMnBC) reaches the set value of the compare register 1, an interrupt is generated at the next count clock. There are 2 sources to be selected to clear the binary counter; the TMnOC1 compare match and the full count overflow. After the binary counter is cleared, the counting up is restarted from x'0000'.

Table 7-3-1 16-bit Timer Interrupt Source and Binary Counter Clear Source (Timer 7, Timer 8)

TMnMD2 register		Interrupt source	Binary counter clear source
TMnIRS1 flag	TMnBCR flag		
1	1	TM7nOC1 compare match	TMnOC1 compare match
0	1	TMnOC1 compare match	TMnOC1 compare match
1	0	TMnOC1 compare match	full count overflow
0	0	full count overflow	full count overflow

Timer 7 and timer 8 can generate another set of an independent interrupt (timer 7 and timer 8 compare register 2 match interrupt) by the set value of the timer 7 and timer 8 compare registers (TM7OC2, TM8OC2). At the time of the interrupt, the binary counter is cleared as the above setup.

The compare register is double buffer type. So, when the value of the preset register is changed during the counting, the changed value is stored to the compare register when the binary counter is cleared. This function can change the compare register value constantly, without disturbing the cycle during timer operation (Reload function).

When the CPU reads the 16-bit binary counter (TMnBC), the read data is handled in 8-bits units even if it is a 16-bit MOVW instruction. As a result, it will read the data incorrectly if a carry from the lower 8 bits to the upper 8 bits occurs during counting operation.

To read the correct value of the 16-bit counting (TMnBC), use the writing program function to the input capture register (TMnIC). By writing to the TMnIC, the counting data of TMnBC can be stored to TMnIC to read out the correct counting value during timer operation.

[☞ Chapter 7-12-1. Operation (p.VII-63)]

Table 7-3-2 shows the clock source that can be selected.

Table 7-3-2 Clock Source at Timer Operation (Timer 7, Timer 8)

Clock source	1 count time
fosc	50 ns
fosc/2	100 ns
fosc/4	200 ns
fosc/16	800 ns
fosc/128 ∗	6.4 µs
fs	100 ns
fs/2	200 ns
fs/4	400 ns
fs/16	1.6 µs
fs/128 ∗	12.8 µs
as fosc = 20 MHz, fs = fosc/2 = 10 MHz	

∗ Only for Timer 8

■Count Timing of Timer Operation (Timer 7, Timer 8)

The binary counter counts up with the selected clock source as the count clock.

The basic operation of whole 16-bit timer functions is as bellow.

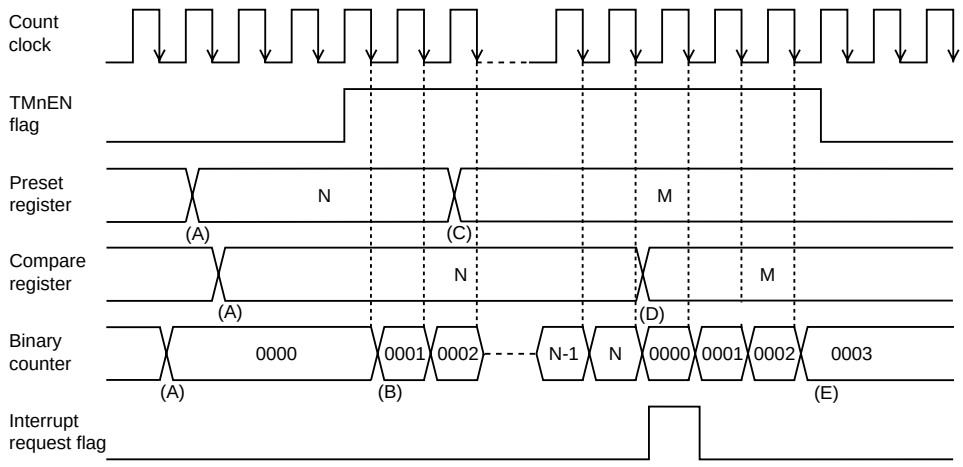


Figure 7-3-1 Count Timing of Timer Operation (Timer 7,Timer 8)

(A) When a data is written to the preset register while the TMnEN flag is stopped ("0"), the same value is loaded during the writing cycle and the binary counter is cleared to x'0000'.

(B) When TMnEN flag is ("1"), the binary counter starts counting. The counting starts at the falling edge of the count clock.

(C) Even if the preset register is rewritten when the TMnEN flag is ("1"), the binary counter is not changed.

(D) When the binary counter reaches value of compare register 1, the set value of the preset register is loaded to the compare register at the next count clock. And the interrupt request flag is set at the next count clock, and the binary counter is cleared to x'0000' to restart counting up.

(E) When the TMnEN flag is ("0"), the binary counter is stopped.

When the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, and the binary counter is cleared. So set the compare register as;
(the set value of the compare register) = (the counts till the interrupt generation - 1)

When timer n compare register 2 match interrupt is generated and TMnOC1 compare match is selected as a binary counter clear source, the set value of the compare register 2 should be smaller than the set value of the compare register 1.

On the interrupt service routine, clear the timer interrupt request flag before the timer is started.

At TMnOC=x'0000', x'0001', the timer n interrupt request generation has the same waveform.

When more than 2 waits is set at access to the special register area by the IOW1, IOW0 flag of the MEMCTR register, write the same value 2 times at setup of the preset register when the timer is stopped. When 1 wait or no wait is set, there is no need to do this.
(This is for the functions of a 16-bit timer.)
[☞ Chapter 2 2-3-2. Control Registers]

Write data in 16-bit unit to the preset registers with MOVW instruction. If data is written in 8-bit unit, correct value may not be loaded into the compare register.

7-3-2 Setup Example

■Timer Operation Setup Example (Timer 7,Timer 8)
Timer 7 generates an interrupt constantly for timer function. Fosc/2 (fosc=20 MHz at operation) is selected as a clock source to generate an interrupt every 1000 cycles (100 µs).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the timer clear source. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(2) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a binary counter clear source.
(3) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(3) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also select 1/2 fosc as a count clock source by TM7PS1-0 flag.
(4) Set the interrupt generation cycle. TM7PR1 (x'3F75', x'3F74')=x'03E7	(4) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The cycle is 1000. The set value should be 1000-1=999(x'03E7'). At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(5) Set the interrupt level. TM7ICR (x'3FF1') bp7-6 : TM7LV1-0 = 10	(5) Set the interrupt level by the TM7LV1-0 flag of the timer 7 interrupt control register (TM7ICR). If the interrupt request flag may be already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM7ICR (x'3FF1') bp1 : TM7IE = 1	(6) Set the TM7IE flag of the TM7ICR register to "1" to enable the interrupt.

Setup Procedure	Description
(7) Start the timer operation. TM7MD1 (x'3F78) bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. When TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock and the TM7BC becomes x'0000' and counts up, again.

When the TMnEN flag of the TMnMD register is changed with other bits, the binary counter may count up by switching operation.

7-4 16-bit Event Count

7-4-1 Operation

Event count operation has 2 types; TMnIO input and synchronous TMnIO input. These can be selected as the count clock. Each type can select 1/1, 1/2, 1/4, 1/16 or 1/128 (Timer 8 only) as a count clock source. Timer 7 can also select the count edge (falling or both edges).

■16-bit Event Count Operation (Timer 7, Timer 8)
The binary counter (TMnBC) counts the external signal input to the TMnIO pin. If the binary counter reaches the set value of the compare register (TMnOC), an interrupt can be generated at the next count clock.

Table 7-4-1 Event Count Input Clock Source

	Timer 7	Timer 8
Event input	TM7IO input (P14)	TM8IO input (P15)
	Synchronous TM7IO input	Synchronous TM8IO input

As an actual count clock, a signal divided by 1, 2, 4, 16 or 128 (Timer 8 only) is selected.

■Count Timing of TMnIO Input (When falling edge is selected, Timer 7,Timer 8)
When TMnIO input is selected, TMnIO input signal is input to the timer n count clock. The binary counter counts up at the falling edge of the TMnIO input signal or TMnIO input signal that passed the divider.

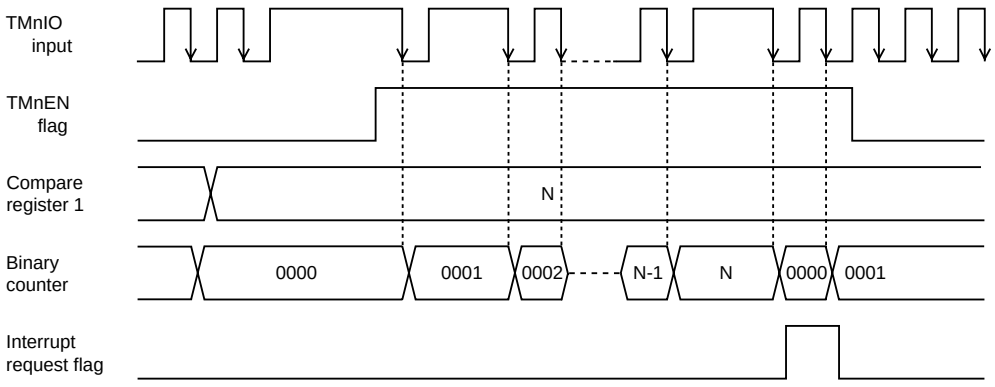


Figure 7-4-1 Count Timing TMnIO Input (Timer 7,Timer 8)

If the binary counter is read out during operation, incorrect data at counting up may be read. To prevent this, use the event count by the synchronous TMnIO input, which is shown in the following page.

■Count Timing of Synchronous TMnIO Input (When falling edge is selected, Timer 7, Timer 8)

If the synchronous TMnIO input is selected, the synchronizing circuit output signal is input to the timer n count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TMnIO input signal is changed. The binary counter counts up at the falling edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the division circuit.

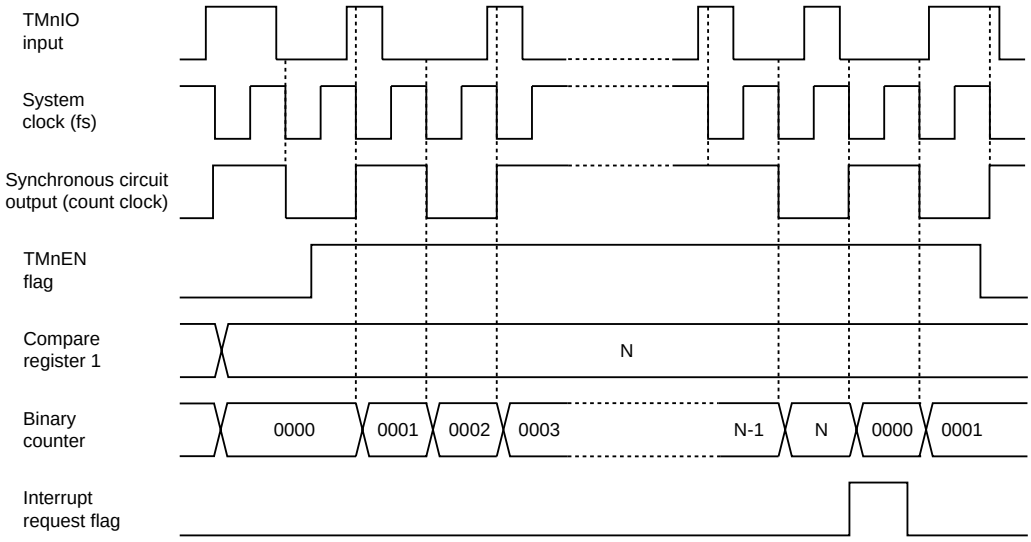


Figure 7-4-2 Count Timing of Synchronous TMnIO Input (Timer 7, Timer 8)

The timer n binary counter counts up the binary counter at the signal in synchronization with the system clock so that correct value is read out from the timer n binary counter. The return from STOP/HALT mode is not possible by the synchronous TMnIO input. And Waveform shorter than the system clock cycle may not be counted as TMnIO input is synchronized with the system clock.

■Count Timing of TM7IO Input (When both edges are selected, Timer 7)

When the TM7IO input is selected, the TM7IO input signal is input to the timer 7 count clock. The binary counter counts up at falling edge or rising edge of the TM7IO input signal that passed through the division circuit.

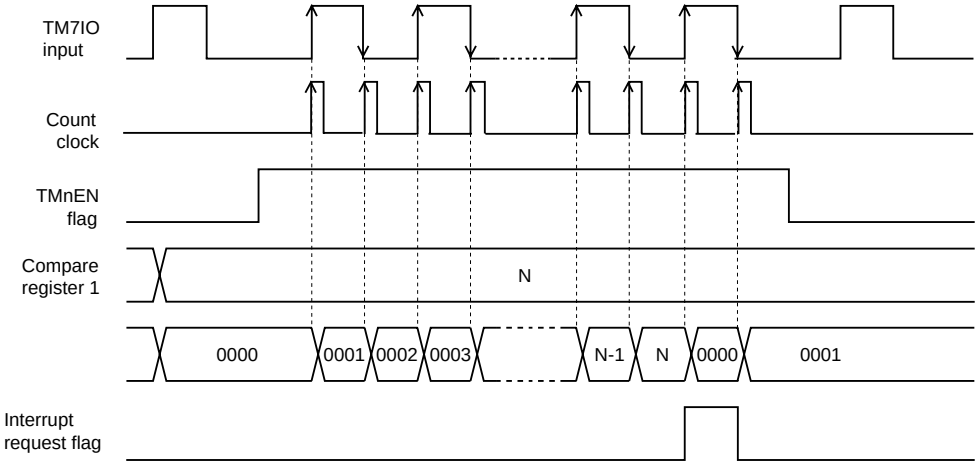


Figure 7-4-3 Count Timing of TM7IO Input (Timer 7)

■Count Timing of Synchronous TM7IO Input (When both edges are selected, Timer 7)

When the synchronous TM7IO input is selected, the synchronizing circuit output signal is input to the timer 7 count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TM7IO input signal is changed. The binary counter counts up at falling edge or rising edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the division circuit.

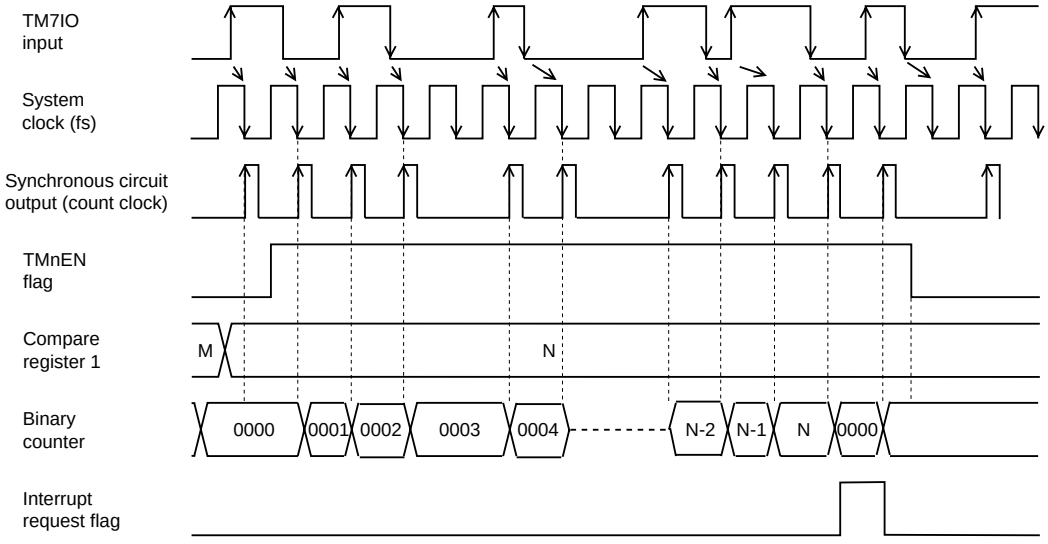


Figure 7-4-4 Count Timing of Synchronous TM7IO Input (Timer 7)

7-4-2 Setup Example

■Event Count Setup Example (Timer 7, Timer 8)

When the falling edge of the TM7IO input pin signal is detected 5 times using timer 7, an interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to input mode. P1DIR (x'3F31') bp4 : P1DIR4 = 0	(2) Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "0" to set P14 pin to input mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(3) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a clear source for the binary counter.
(4) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 10 bp3-2 : TM7PS1-0 = 00	(4) Select the TM7IO input as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1(no division) as a count clock source by the TM7PS1-0 flag.
(5) Set the interrupt generation cycle. TM7PR1 (x'3F75', x'3F74')=x'0004'	(5) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The set value should be 4, because the counting is 5 times. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.

Setup Procedure	Description
(6) Set the interrupt level. TM7ICR (x'3FF1') bp7-6 :TM7LV1-0 = 10	(6) Set the interrupt level by the TM7LV1-0 flag of the timer 7 interrupt control register (TM7ICR). If any interrupt request flag is already set, clear those request flags. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(7) Enable the interrupt. TM7ICR (x'3FF1') bp1 : TM7IE = 1	(7) Set the TM7IE flag of the TM7ICR register to "1" to enable interrupt.
(8) Start the event count. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

Every time TM7BC detects the falling edge of the TM7IO input, it counts up from x'0000'. When the TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock, and the value of TM7BC becomes x'0000' to restart counting up.

7-5 16-bit Timer Pulse Output

7-5-1 Operation

TMnIO pin can output a pulse signal with an arbitrary frequency. The TMnO pin (large current pin) can output it, too.

■16-bit Timer Pulse Output Operation (Timer 7,Timer 8)
These timers can output 2 x cycle signal, compared with the set value of the compare register 1 (TMnOC1) and the 16-bit full count.
Output pins are as follows.

Table 7-5-1 Timer Pulse Output Pin

	Timer 7	Timer 8
Pulse output pin	TM7IO output (P14)	TM8IO output (P15)
	TM7O output (P51)	TM8O output (P53)

Table 7-5-2 shows the timer interrupt generation sources and the flags that control the timer pulse output cycle.

Table 7-5-2 16-bit Timer Interrupt Generation Source and Timer Pulse Output Cycle (Timer 7, Timer 8)

TMnMD2 register		Interrupt source	Timer pulse output cycle
TMnIRS1 flag	TMnBCR flag		
1	1	TMnOC1 compare match	set value of TMnOC1 x 2
0	1	TMnOC1 compare match	set value of TMnOC1 x 2
1	0	TMnOC1 compare match	full count of TMnBC x 2
0	0	full count overflow	full count of TMnBC x 2

■Count Timing of Timer Pulse Output by Compare Match (Timer 7,Timer 8)

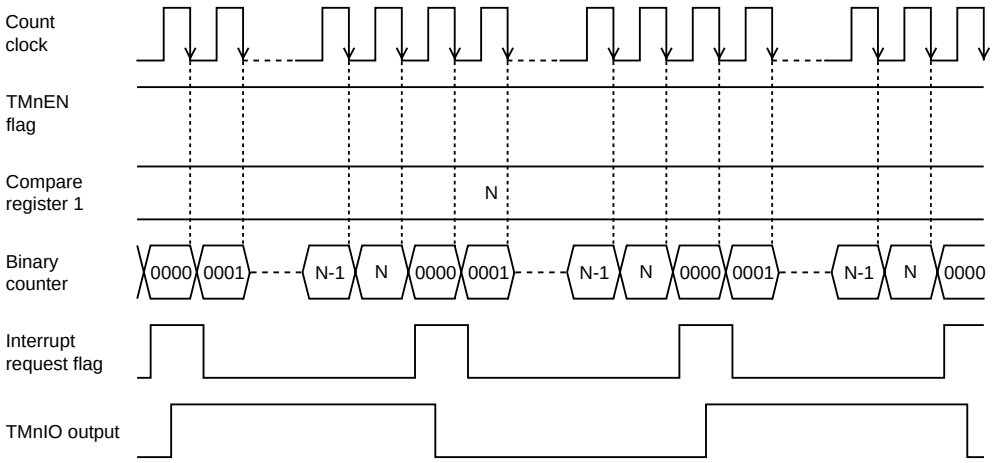


Figure 7-5-1 Count Timing of Timer Pulse Output (Timer 7, Timer 8)

TMnIO output pin outputs 2 x cycle, compared with the value of Compare Register 1 and the full-count-overflow signal. If the binary counter reaches the compare value or full count overflow is occurred, the binary counter is cleared to x'0000', and the TMnIO output (timer output) is inverted. The inversion of the timer output is changed at the count clock at the rising edge. These form the correct output signal and internal waveform.

In the initial state after releasing reset, the timer pulse output is reset, and low output is fixed. Therefore, release the reset of the timer pulse output by setting the TMnCL flag of the TMnMD1 register to "0".

7-5-2 Setup Example

■Timer Pulse Output Setup Example (Timer 7, Timer 8)

TM7IO output pin outputs a 50 kHz pulse using timer 7. For this, select fosc as the clock source and set 1/2 cycle (100 kHz) to the timer 7 compare register (at fosc=20 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set P14 pin as the special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the timer pulse output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0= 00	(3) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "00" to select the timer pulse output.
(4) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as a clear source of a binary counter .
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(5) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 frequency as the count clock source by the TM7PS1-0 flag.

Setup Procedure	Description
(6) Set the timer pulse output cycle. TM7PR1 (X'3F75', X'3F74')=x'00C7'	(6) Set 1/2 cycle of the timer pulse output to the timer 7 preset register 1(TM7PR1). To set 100 kHz by dividing 20 MHz, set as follows: 200 - 1 = 199 (x'C7') The same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Release the reset of the timer pulse output. TM7MD1 (x'3F78') bp5 : TM7CL = 0	(7) Set the TN7CL flag of the TM7MD1 register to "0" to enable the timer pulse output.
(8) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. If TM7BC reaches the set value of the TM7OC1 register and TM7BC is cleared to x'0000', the signal of the TM7IO output is inverted and TM7BC counts up from x'0000', again.

To output the timer pulse output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) to "1" at the setup example (2), to set the P51 pin as a special function pin and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

At TMnOC1 = x'0000' and x'0001', the timer pulse output have the same waveform.

Regardless of whether the binary counter is stopped or operated, the timer output is "L", when the TMnCL flag of the TMnMD1 register is set to "1".

7-6 16-bit Standard PWM Output

(Only duty can be changed consecutively)

The TMnIO pin outputs the standard PWM output, which is determined by the overflow timing of the binary counter, and the match timing of the timer binary counter and the compare register.
It can also be output from the TMnO high current pin.

7-6-1 Operation

■16-bit Standard PWM Output (Timer 7, Timer 8)
PWM waveform with an arbitrary duty is generated by setting a duty of PWM "H" period to the compare register 1 (TMnOC1). Its cycle is the time of the 16-bit timer full count overflow.
Table 7-6-1 shows the PWM output pin.

Table 7-6-1 PWM Output Pin

	Timer 7	Timer 8
PWM output pin	TM7IO output pin (P14)	TM8IO output pin (P15)
	TM7IO output pin (P51)	TM8IO output pin (P53)

■Count Timing of Standard PWM Output (at Normal)(Timer 7, Timer 8)

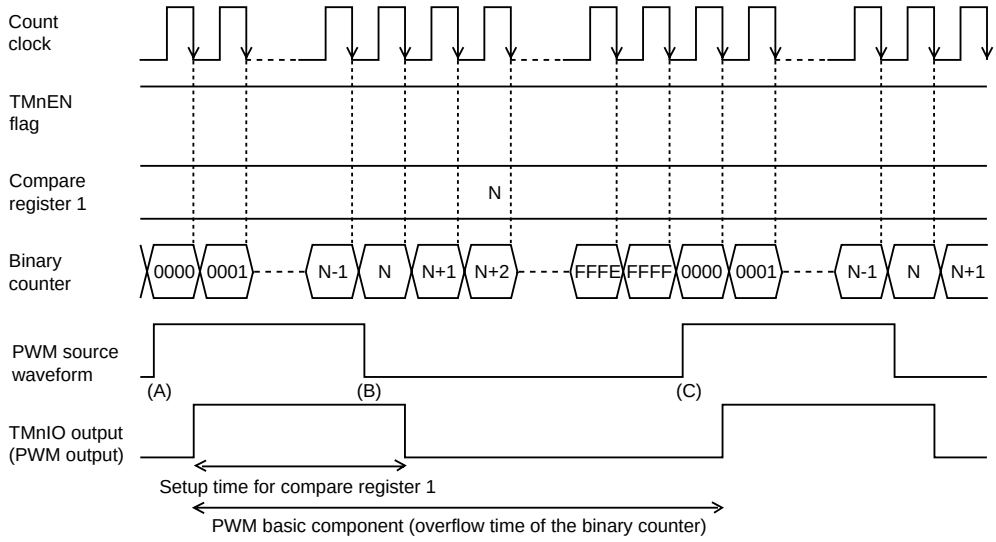


Figure 7-6-1 Count Timing of Standard PWM Output (at Normal)

PWM source waveform,

(A) shows "H" until the binary counter reaches the compare register value from x'0000'.

(B) shows "L" after the compare match, then the binary counter counts up till the overflow.

(C) shows "H" again if the binary counter overflow.

The PWM output form pin is 1 count clock delay of PWM source waveform. This is happened to form waveform inside the microcontroller to correct the output cycle.

■Count Timing of Standard PWM Output (when Compare Register 1 is x'0000')(Timer 7, Timer 8)
Here is the count timing at setting x'0000' to the compare register 1.

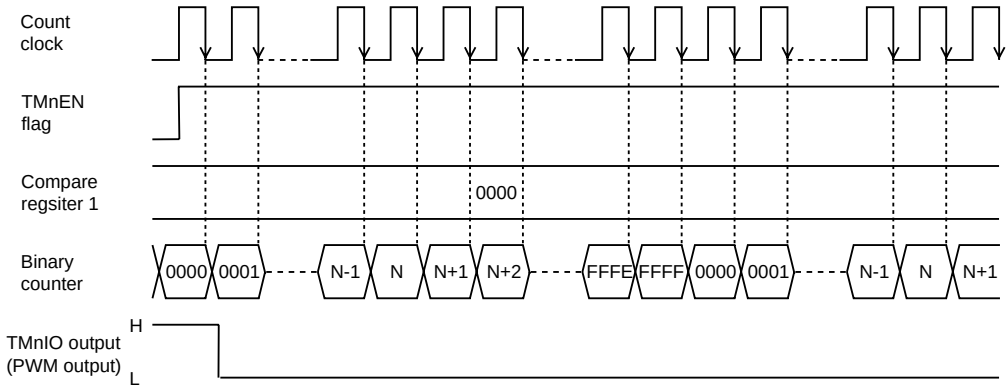


Figure 7-6-2 Count Timing of Standard PWM Output (when Compare Register 1 is x'0000')

PWM output shows "H", when TMnEN flag is stopped (at "0"). But either "L" or "H" is selectable in timer 8.

■Count Timing of Standard PWM Output (when Compare Register 1 is x'FFFF')(Timer 7,Timer 8)
Here is the count timing at setting x'FFFF' to the compare register 1.

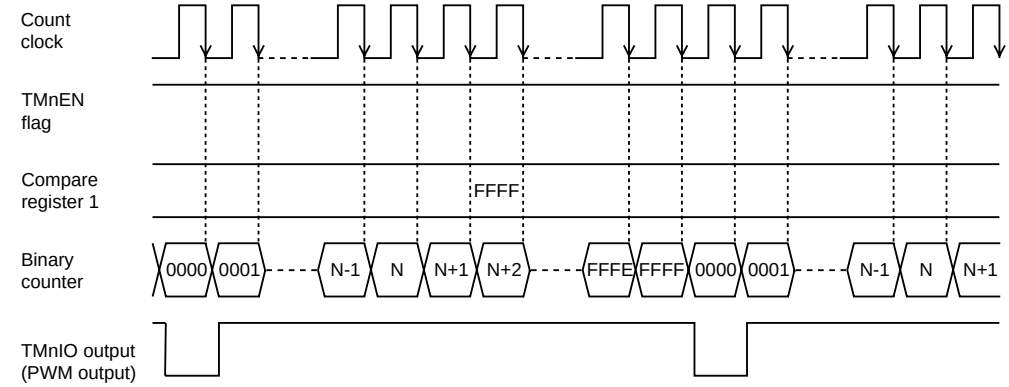


Figure 7-6-3 Count Timing of Standard PWM Output (when Compare Register 1 is x'FFFF')

To output the standard PWM output, set the TMnBCR flag of the TM7MD2 or TM8MO3 register to "0" to select the full count overflow as the binary counter clear source and the PWM output set ("H" output) source.

The TMnOC1 compare match or the TMnOC2 compare match can be selected as a PWM output reset ("L" output) source with the TnPWMSL flag of the TMnMD2 register.

7-6-2 Setup Example

■Standard PWM Output Setup Example (Timer 7,Timer 8)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 305.18 Hz with timer 7 (at the high frequency oscillation, fosc=20 MHz). One cycle of the PWM output waveform is decided by the overflow of a binary counter. "H" period of the PWM output waveform is decided by the set value of a compare register 1.

An example setup procedure, with a description of each step is shown below.

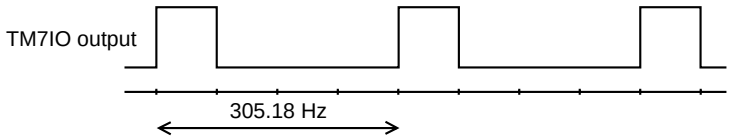


Figure 7-6-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the PWM output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0 = 1	(3) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "01" to select the PWM output.
(4) Set the standard PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 0	(4) Set the TM7BCR flag of the TM7MD2 register to "0" to select the full count overflow as the binary counter clear source.

Setup Procedure	Description
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(5) Select fosc as the clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 frequency (no division) at count clock source by the TM7PS1-0 flag.
(6) Set "H" period of the PWM output. TM7PR1 (x'3F75', x'3F74')=x'4000'	(6) Set "H" period of the PWM output to the timer 7 preset register 1 (TM7PR1). To be a 1/4 duty of the full count (65536), set as follows: 65536 / 4 = 16384 (x'4000') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The PWM source waveform outputs "H" until TM7BC reaches the set value of the TM7OC1 register, then, after the match it outputs "L". After that, TM7BC continues to count up. Once a overflow occurs, the PWM source waveform outputs "H" again, and TM7BC counts up from x'0000', again. TM7IO pin outputs one count clock delay of the PWM source waveform.

To output the timer pulse output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) to "1" at the setup example (2), to set the P51 pin as a special function pin, and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

In the initial state of the PWM output, it is changed to "H" output from "L" output at the timing that the PWM operation is selected with the TM7OUT1-0 flag of the TM7MD3 register.
As for timer 8, it can be selected with the TM8PWMF flag of TM8MD3.

7-7 16-bit High Precision PWM Output

(Cycle/Duty can be changed consecutively)

The TMnIO pin outputs high precision PWM output, which is determined by the match timing of the timer binary counter and the compare register 1, and match timing of the binary counter and the compare register 2. It can be also output from the TMnO high current pin.

7-7-1 Operation

■16-bit High Precision PWM Output Operation (Timer 7, Timer 8)

The PWM waveform of an any cycle/duty is generated by setting the cycle of PWM to the compare register 1 (TMnOC1) and setting the duty of the "H" period to the compare register 2 (TMnOC2).

■Count Timing of High Precision PWM Output (at Normal) (Timer 7, Timer 8)

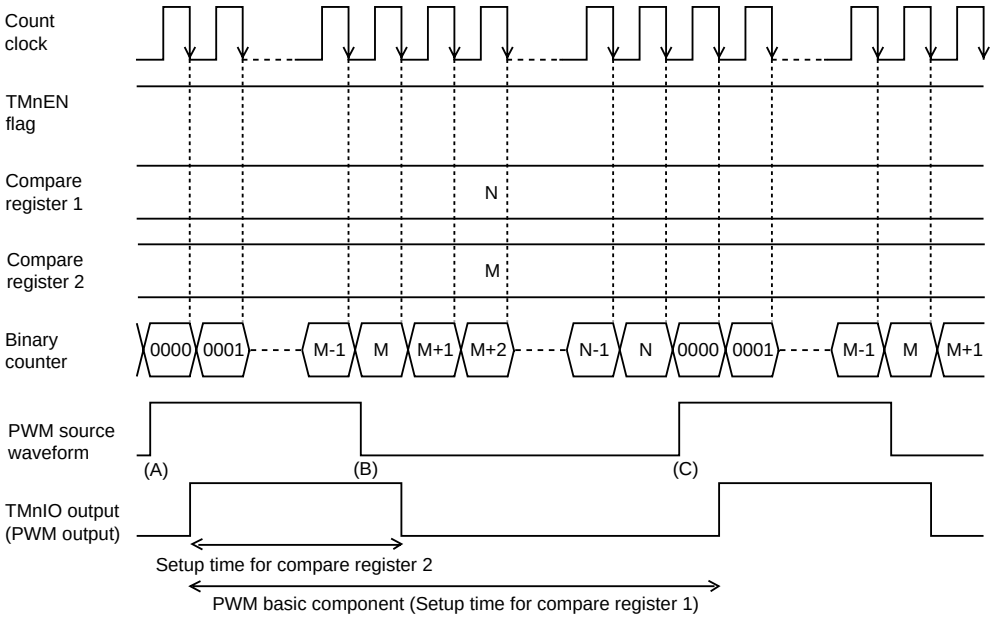


Figure 7-7-1 Count Timing of High Precision PWM Output (at Normal)

PWM source waveform,

(A) shows "H" until the binary counter reaches the compare register from x'0000'.

(B) shows "L" after the TMnOC2 compare match, the binary counter then counts up until the binary counter reaches the TMnOC1 compare register is cleared.

(C) shows "H" again when the binary counter is cleared.

The PWM output from pin is 1 count clock delay of PWM source waveform. This is happened to form waveform inside microcontroller to correct the output cycle.

■Count Timing of High Precision PWM Output (When compare register 2 is x'0000') (Timer 7, Timer 8)
Here is the count timing as the compare register 2 is set to x'0000';

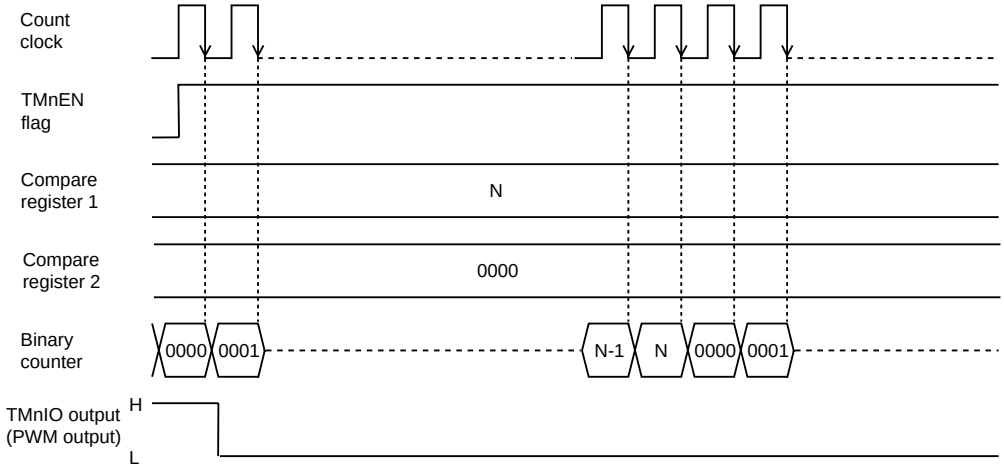


Figure 7-7-2 Count Timing of High Precision PWM Output (When compare register 2 is x'0000')

When the TMnEN flag is stopped (at "0"), the PWM output shows "H". In Timer 8, either "L" or "H" can be selected.

■Count Timing of High Precision PWM Output (at compare register 2 = compare register 1) (Timer 7, Timer 8)
Here is the count timing as the compare register 2 is set the same value to the compare register 1;

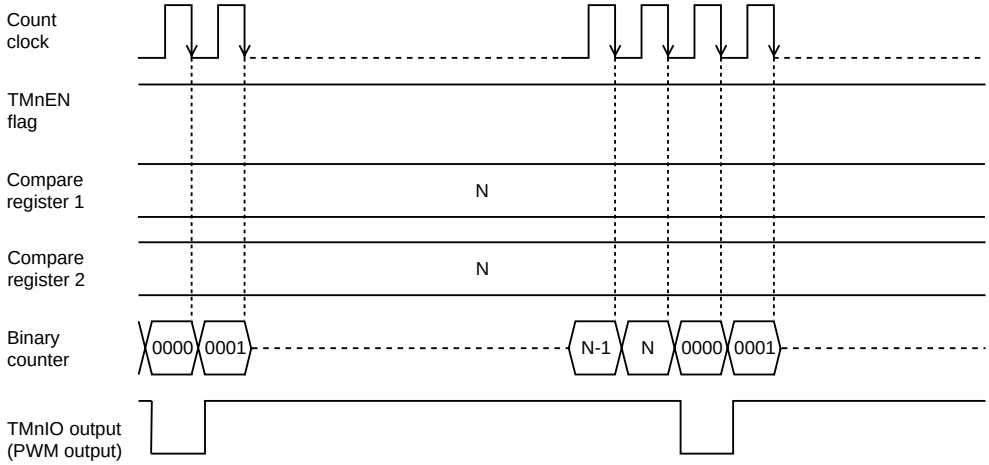


Figure 7-7-3 Count Timing of High Precision PWM Output (at compare register 2=compare register 1)

To output the high precision PWM output, set the TMnBCR flag of the TM7MD2 register or TM8MD3 register to "1" to select the TMnOC1 compare match as the clear source for the binary counter, and the set ("H" output) source of the PWM output. Also, set the TnPWMSL flag to "1" to select the TMnOC2 compare match as the reset ("L" output) source of the PWM output.

7-7-2 Setup Example

■High Precision PWM Output Setup Example (Timer 7,Timer 8)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 400 Hz with timer 7. Select fosc/2 (at fosc = 20 MHz) as the clock source. One cycle of the PWM output waveform is decided by the set value of a compare register 1. "H" period of the PWM output waveform is decided by the set value of a compare register 2.

An example setup procedure, with a description of each step is shown below.

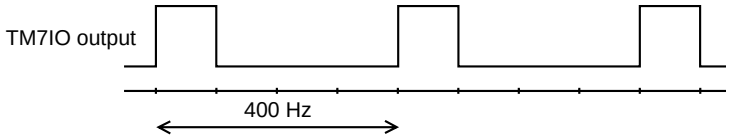


Figure 7-7-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 :P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port1 output mode register (P1OMD) to "1" to set the p14 pin as a special function pin. Set the P1DIR4 flag of the port1 direction control register (P1DIR) to "1" for output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the PWM output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0 = 1	(3) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "01" to select the PWM output.
(4) Set the high precision PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1 bp6 : T7PWMSL = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as a clear source of binary counter. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a duty select source of the PWM output.

Setup Procedure	Description
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(5) Select fosc as the clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/2 dividing as count clock source by the TM7PS1-0 flag.
(6) Set the PWM output cycle. TM7PR1 (x'3F75',x'3F74') = x'61a7'	(6) Set the PWM output cycle to the timer 7 preset register 1 (TM7PR1). To be 400 Hz by dividing 10 MHz, set as follows: 25000 - 1 = 24999 (x'61a7') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Set the "H" period of the PWM output. TM7PR2 (x'3F7D',x'3F7C')=x'186a'	(7) Set the "H" period of the PWM output to the timer 7 preset register 2 (TM7PR2). To be a 1/4 duty of 25000 dividing, set as follows: 25000 / 4 = 6250 (x'186a') At that time, the same value is loaded to the timer 7 compare register 2 (TM7OC2).
(8) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The PWM source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up. Once TM7BC matches the TM7OC1 register to be cleared, the PWM source waveform outputs "H" again and TM7BC counts up from x'0000' again. TM7IO pin outputs one count clock delay of the PWM source waveform.

To output the timer pulse output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) at the setup example(2), to "1" to set the P51 pin as a special function pin, and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

In the initial state of the PWM output, it is changed to "H" output from "L" output at the timing that the PWM operation is selected with the TM7OUT1-0 flag of the TM7MD3 register. As for timer 8, it can be selected with the TN8PWMF flag of TM8MD3.

Set as the set value of TMnOC2 ≤ the set value of TMnOC1. If it is set as the set value of TMnOC2 > the set value of TMnOC1, the PWM output is a "H" fixed output.

7-8 16-bit Standard IGBT Output

(Duty can be changed consectively)

A trigger factor of the standard IGBT output activation can be selected from among external interrupt pins 0 to 2, or timer 7 count operation. Once started, the count operation is same as that of the standard PWM output.

7-8-1 Operation

■IGBT trigger selection

IGBT trigger can be selected from among IRQ0, IRQ1, IRQ2 and start of timer 7 operation with TM7ICT0 and 1 flag of the TM7MD2 register. To control the activation externally, select one of IRQ0 to IRQ2 and set "1" (designation edge) to the T7ICEDG flag of the TM7MD2 register. This trigger detects the input level before activation. Either "H" or "L" level can be selected with the REGn flag of the IRQnICR register. When "1" (rising edge) is selected, count operation continues while the trigger pin is "H". When "0" (falling edge) is selected, count operation continues while the trigger pin is "L".

To control the activation with instruction, select the TM7EN count operation. And timer count operation and IGBT output can be controlled with the TM7EN flag of the TM7MD1 register. If "1" (count operation) is selected, count operation continues untill "0" (count stop) is set. Set always T7ICT0,1 of the TM7MD2 register before operate TM7EN of the TM7MD1 register.

■16-bit Standard IGBT Output Operation (Timer 7)

Set the duty of IGBT "H" period to compare register 1 (TM7OC1), and detect the trigger generated by external interrupt, which passed through external interrupt interface block. And then any IGBT waveform can be formed. The IGBT cycle is full-count overflow duration of the 16-bit timer. The standard IGBT output function can be used with only timer 7 among 16-bit timers.

Table 7-8-1 IGBT Output Pin

	Timer 7
IGBT output pin	TM7IO output pin (P14)
	TM7IO output pin (P51)

Table 7-8-2 IGBT Trigger

	Timer 7 mode register 2		External interrupt n control register (IRQnICR)
	T7ICT1-0	T7ICEDG	REDGn (bp5)
IRQ0 falling edge	00 (IRQ0)	1	0
IRQ0 rising edge	00 (IRQ0)	1	1
IRQ1 falling edge	01 (IRQ1)	1	0
IRQ1 rising edge	01 (IRQ1)	1	1
IRQ2 falling edge	10 (IRQ2)	1	0
IRQ2 rising edge	10 (IRQ2)	1	1
TM7EN count operation	11	1	-

■Count Timing of Standard IGBT Output (at Normal)(Timer 7)

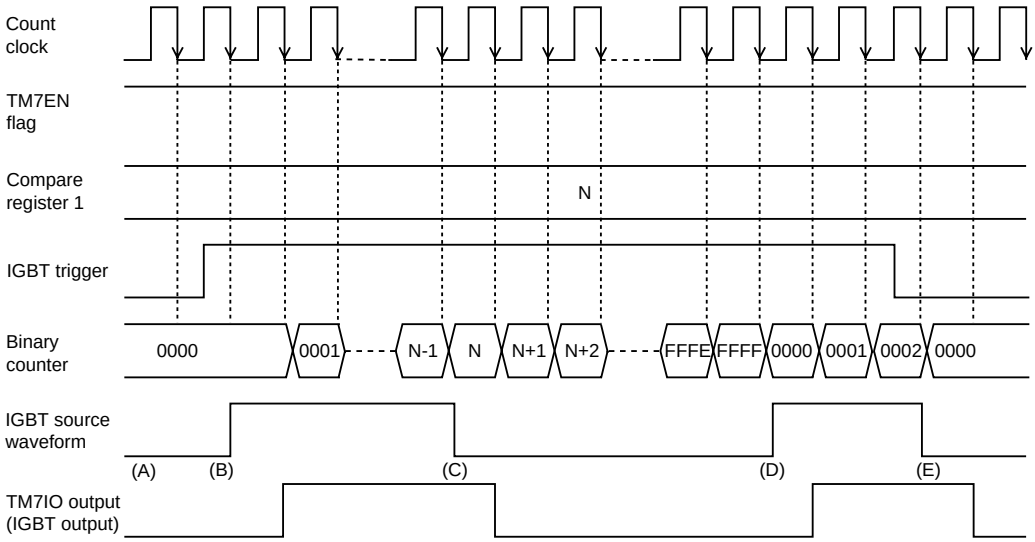


Figure 7-8-1 Count Timing of Standard IGBT Output (at Normal)

IGBT source waveform

(A) shows “L” until the IGBT trigger is input and becomes valid.

(B) shows “H” at the valid trigger, during the period when the binary counter value increases from X’0000’ until the compare register value.

(C) shows “L” after the compare match. The binary counter continues to count up until the binary counter overflows.

(D) show “H” again when the binary counter overflows.

(E) When the IGBT becomes invalid, the timer is initialized. The waveform is forced to “L”.

The IGBT output form pins has 1 count clock delay of IGBT source waveform. This is happened to form waveform inside the microcontroller to correct the output cycle.

■Count Timing of Standard IGBT Output (When compare register 1 is x'0000') (Timer 7)
Here is the count timing as the compare register 1 is set to x'0000';

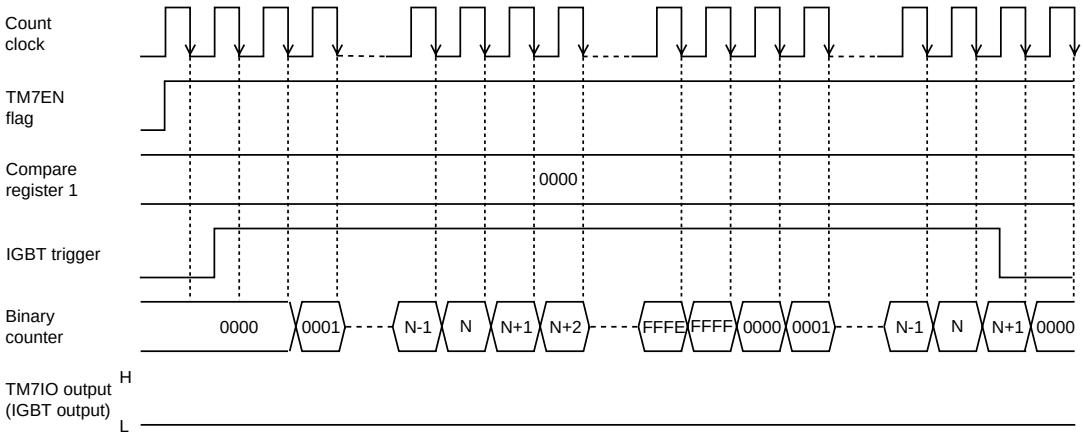


Figure 7-8-2 Count Timing of Standard IGBT Output (When compare register 1 is x'0000')

When the TM7EN flag is stopped (at "0"), the IGBT output shows "L".

■Count Timing of Standard IGBT Output (When compare register 1 is x'FFFF') (Timer 7)
Here is the count timing as the compare register 1 is set to x'FFFF';

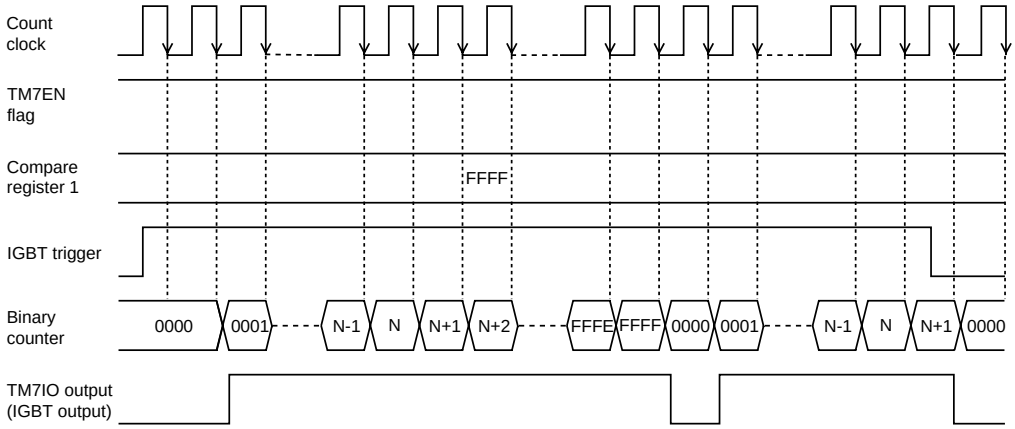


Figure 7-8-3 Count Timing of Standard IGBT Output (When compare register 1 is x'FFFF')

When the standard IGBT output is operated, set the TM7BCR flag of the TM7MD2 register to "0" to select the full count overflow as the binary counter clear source and the IGBT output set ("H" output) source.

With the T7PWMSL flag of the TM7MD2 register, the TM7OC1 compare match or the TM7OC2 compare match can be selected as the IGBT output reset ("L" output) source.

7-8-2 Setup Example

■ Standard IGBT Output Setting Example (Timer 7)

With timer 7, at the interrupt generation edge of the external interrupt 0 input signal, the TM7IO output pin outputs IGBT output waveform at 305.18 Hz, 1/4 duty (at fosc=20 MHz). The binary counter overflow duration determines the IGBT output waveform's cycle. The value set in compare register 1 determines the IGBT waveform "H" period.

An example setup procedure, with the descriptions for each step, is shown bellow.

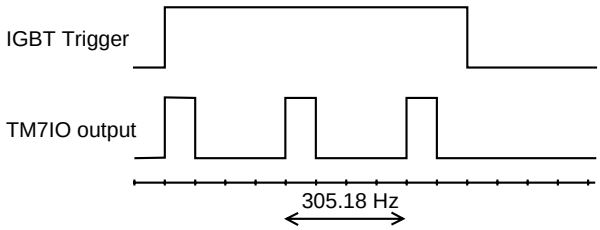


Figure 7-8-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the IGBT output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0= 10	(3) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "10" to select the IGBT output.
(4) Set the standard precision IGBT output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "0" to select the overflow as the clear source of the binary counter.

Setup Procedure	Description
(5) Select the TM7MD2 (x'3F79') bp1-0 : T7ICT1-0 = 00	(5) Select the external interrupt 0 (IRQ0) input as the IGBT trigger source by T7ICT1-0 flag of the TM7MD2 register.
(6) Select the Interrupt generation valid edge IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(6) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as a the Interrupt generation valid edge.
(7) Select the IGBT trigger generation edge TM7MD2 (x'3F79') bp7 : T7ICEDG = 1	(7) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the IGBT trigger source as the specified edge of the external interrupt signal.
(8) Select the delay time. TM7MD3 (x'3F6C') bp3-2 : TRGDLT1-0= 00	(8) Set the TRGLT1-0 flag of the TM7MD3 register to "00" to select no dead time.
(9) Set the interruput level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(9) Set the interrupt level by the IRQ0LV1-0 flag of the IRQ0ICR register. If any interrupt request flag is already set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(10) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(10) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
(11) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(11) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 dividing (no dividing) as a count clock source by the TM7PS1-0 flag.

Setup Procedure	Description
(12) Set the "H" period of the IGBT output. TM7PR1 (x'3F75',x'3F74')=x'4000'	(12) Set the "H" period of the IGBT output to the timer 7 preset register 1 (TM7PR1). To set a 1/4 duty of full count (65536), set as; 65536 / 4 = 16384 (x'4000') At the same time, the same value is loaded into the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(13) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(13) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

When the trigger is valid, TM7BC counts up from x'0000'. The IGBT source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up, and if it overflows, the IGBT source waveform outputs "H" and TM7BC counts up from x'0000' again. When the trigger becomes invalid, the output become "L". TM7IO pin outputs IGBT source waveform one count clock delay.

To output IGBT output from the TM7O large current pin, set the P5OMD1 flag of the port 5 output mode register (P5OMD) to "1" at the setup example (2), to set the P51 pin as a special function pin, and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

In the initial state of the IGBT output, it is changed from "L" output to "H" output as the IGBT output is selected with the TM7OUT1-0 flag of the TM7MD3 register.

To output the standard IGBT output, set the T7ICEDG flag of the TM7MD2 register to "1".

7-9 16-bit High Precision IGBT Output

(Cycle/Duty can be changed consecutively)

The high precision IGBT output starts count up triggered by external interrupt input signal. As an activation trigger, external interrupt 0 to 2, or timer 7 count operation can be selected. Once started, the operation is same as that of the high precision PWM output.

7-9-1 Operation

■IGBT trigger selection

IGBT trigger can be selected from among IRQ0, IRQ1, IRQ2 and start of timer 7 operation with TM7ICT0 and 1 flag of the TM7MD2 register. To control the activation externally, select one of IRQ0 to IRQ2 and set "1" (specified edge) to the T7ICEDG flag of the TM7MD2 register. This trigger detects the input level before activation. Either "H" or "L" level can be selected with the REGn flag of the IRQnICR register. When "1" (rising edge) is selected, count operation continues while the trigger pin is "H". When "0" (falling edge) is selected, count operation continues while the trigger pin is "L".

To control the activation with instruction, select the TM7EN count operation. And timer count operation and IGBT output can be controlled with the TM7EN flag of the TM7MD1 register. If "1" (count operation) is selected, count operation continues untill "0" (count stop) is set. Set always T7ICT0,1 of the TM7MD2 register before operate TM7EN of the TM7MD1 register.

■16-bit High Precision IGBT Output Operation (Timer 7)

To form IGBT waveform of any cycle/duty, set the IGBT cycle to the compare register 1 (TM7OC1), and set the duty of IGBT “H” period to compare register 2 (TM7OC2). The high precision IGBT output function can be used only with timer 7 among 16-bit timers.

■Count Timing of High Precision IGBT Output (at Normal) (Timer 7)

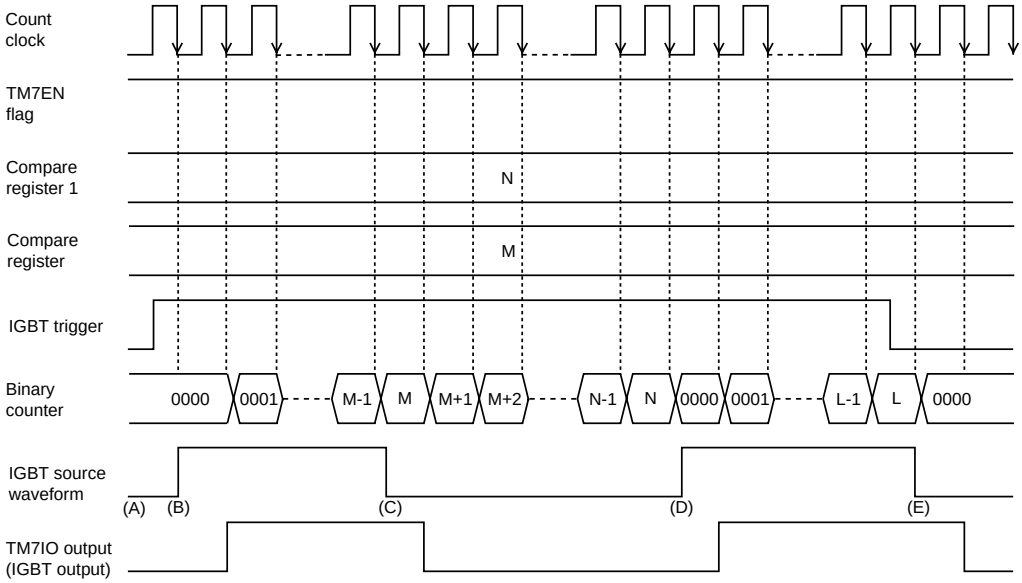


Figure 7-9-1 Count Timing of High Precision IGBT Output (at Normal)

IGBT source waveform

(A) shows “L” until the IGBT trigger is input and becomes valid.

(B) shows “H” when the IGBT trigger is valid and untill the binary counter value reaches to the compare register value of theTMOC2 from X’0000’.

(C) shows “L” after the TMOC2 compare match. The binary counter continues to count up until the binary counter value reaches TM7OC1 register value to be cleared.

(D) show “H” again when the binary counter is cleared.

(E) When the IGBT becomes invalid, the timer is initialized. The waveform is forced to be “L”.

The IGBT output form pin is 1 count clock delay of IGBT source waveform. This is happened to form waveform inside the microcontroller to correct the output cycle.

■Count Timing of High Precision IGBT Output (When the value of compare register 2 is x'0000') (Timer 7)

Here is the count timing as the compare register 2 is set to x'0000';

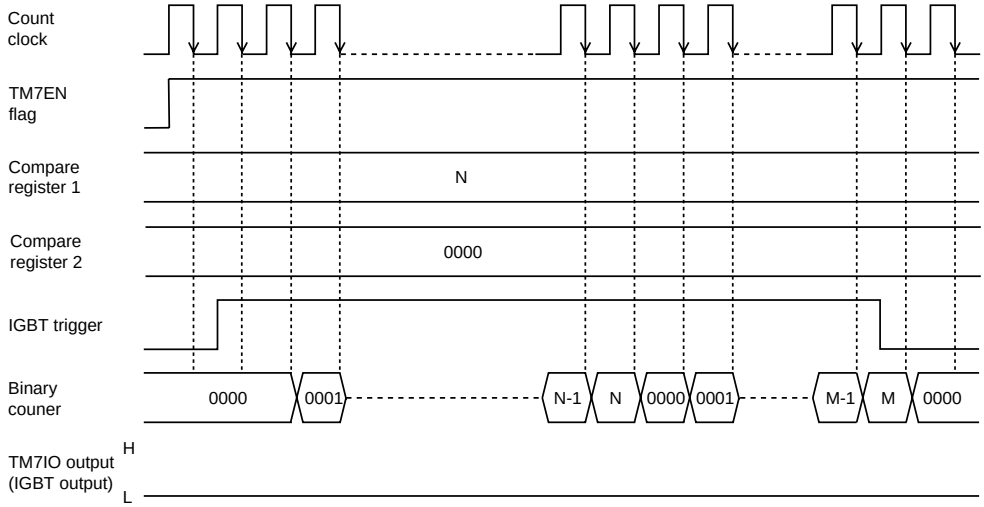


Figure 7-9-2 Count Timing of High Precision IGBT Output (When the value of compare register 2 is x'0000')

When the TM7EN flag is stopped (at "0"), the IGBT output shows "H".

■Count Timing of High Precision PWM Output

(When the value of compare register 2 is same as that of compare register 1) (Timer 7)

Here is the count timing as the compare register 2 is set the same value as the compare register 1;

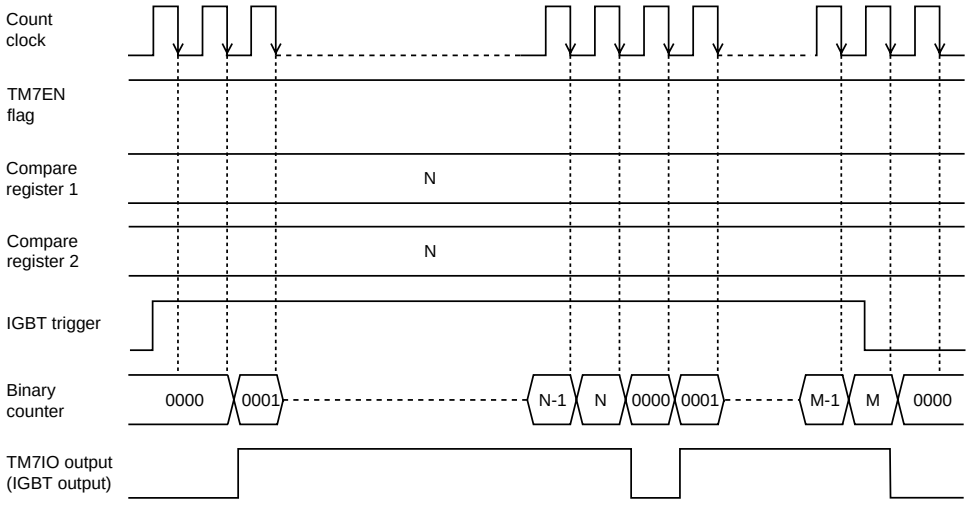


Figure 7-9-3 Count Timing of High Precision IGBT Output (When the value of compare register 2 is same as that of compare register 1)

To output the high precision IGBT output, set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the clear source of the binary counter and as a setup source of the IGBT output ("H" output). Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a reset ("L" output) source of the IGBT output.

7-9-2 Setup Example

■High Precision IGBT Output Setup Example (Timer 7)

At the interrupt generation edge of the external interrupt 0 input signal, TM7IO output pin outputs the 1/4 duty IGBT waveform at 400 Hz using timer 7. Select fosc/2 (at fosc = 20 MHz) as a clock source. Required period for one IGBT output waveform cycle depends on the set value of the compare register 1. "H" period of IGBT output standard waveform depends on the set value of the compare register 2. An example setup procedure, with a description of each step is shown below.

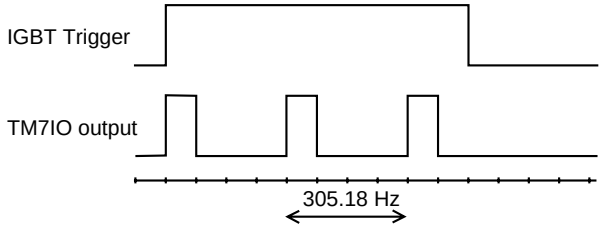


Figure 7-9-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the IGBT output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0= 10	(3) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "10" to select the IGBT output.
(4) Set the high precision IGBT output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the clear source for the binary counter. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as the source for the IGBT output's duty.

Setup Procedure	Description
(5) Select the IGBT trigger source TM7MD2 (x'3F79') bp1-0 : T7ICT1-0 = 00	(5) Select the external interrupt 0 (IRQ0) input as a IGBT trigger source with the T7ICT1-0 flag of the TM7MD2 register.
(6) Select the Interrupt generation valid edge IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(6) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as a the interrupt generation valid edge.
(7) Select the IGBT trigger generation edge TM7MD2 (x'3F79') bp7 : T7ICEDG = 1	(7) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the IGBT trigger factor as the specified edge of the external interrupt.
(8) Select the interruput level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(8) Set the interrupt level by the IRQ0LV1-0 flag of the IRQ0ICR register. If any interrupt request flag is already set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(9) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
(10) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(10) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/2 dividing as a count clock source by the TM7PS1-0 flag.
(11) Set the IGBT output cycle. TM7PR1 (x'3F75',x'3F74') = x'61a7'	(11) Set the IGBT output cycle to the timer 7 preset register 1 (TM7PR1). To be 400 Hz by dividing 10 MHz, set as; 25000 - 1 = 24999 (x'61a7') At this time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.

Setup Procedure	Description
(12) Set the "H" period of the IGBT output. TM7PR2 (x'3F7D',x'3F7C')=x'186a'	(12) Set the "H" period of the IGBT output to the timer 7 preset register 2 (TM7PR2). To set 1/4 duty of 25000 dividing, set as; 25000 / 4 = 6250 (x'186a') At the same time, the same value is loaded tothe timer 7 compare register 2 (TM7OC2).
(13) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(13) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The IGBT source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up; Once TM7BC matches the TM7OC1 register to be cleared, the IGBT source waveform outputs "H" and TM7BC counts up from x'0000' again. TM7IO pin outputs IGBT source waveform of one count clock delay.

To output IGBT output from TM7O, set the P5OMD1 flag of the port 5 output mode register (P5OMD) to "1" at the setup example(2), to set the P51 pin as a special function pin, and set the P5DIR1 flag of the port 5 direction control register to "1" to set output mode.

In the initial state of the IGBT output, it is changed from "L" output to "H" output as the IGBT output is selected by the TM7OUT1-0 flag of the TM7MD3 register.

Set as the set value of TM7OC2 ≤ the set value of TM7OC1. If it is set as the set value of TM7OC2 > the set value of TM7OC1, the IGBT output is a "H" fixed output.

7-10 Dead Time IGBT Output

The IGBT output with dead time generates the waveform, inclusive ON or OFF time delay, during the standard IGBT signal inversion. And the formed waveform is output through TM7IO and TM8IO pins. Each external interrupt 0 to 2 and timer 7 count operation can be selected as the activation trigger.

7-10-1 Operation

■Dead Time IGBT Output Operation (Timer 7)

Dead time is controlled through the TM7OUT1, 2 flags of the timer 7 mode register 3 (TM7MD3). It can be set to the preset register 1, 2 (TMDEADPR1, 2). Dead time IGBT output function is used with timer 7.

■IGBT trigger selection

IGBT trigger can be selected from among IRQ0, IRQ1, IRQ2 and start of timer 7 operation. To control the activation externally, select one of IRQ0 to IRQ2 and set "1" (specified edge) to the T7ICEDG flag of the TM7MD2 register. This trigger detects the input level before activation. Either "H" or "L" level can be selected with the REGn flag of the IRQnICR register. When "1" (rising edge) is selected, count operation continues while the trigger pin is "H". When "0" (falling edge) is selected, count operation continues while the trigger pin is "L".

To control the activation with instruction, select the TM7EN count operation. And timer count operation and IGBT output can be controlled with the TM7EN flag of the TM7MD1 register. If "1" (count operation) is selected, count operation continues untill "0" (count stop) is set. Set always T7ICT0,1 of the TM7MD2 register before operate TM7EN of the TM7MD1 register.

■Count Timing of Dead Time IGBT Output (Timer 7)

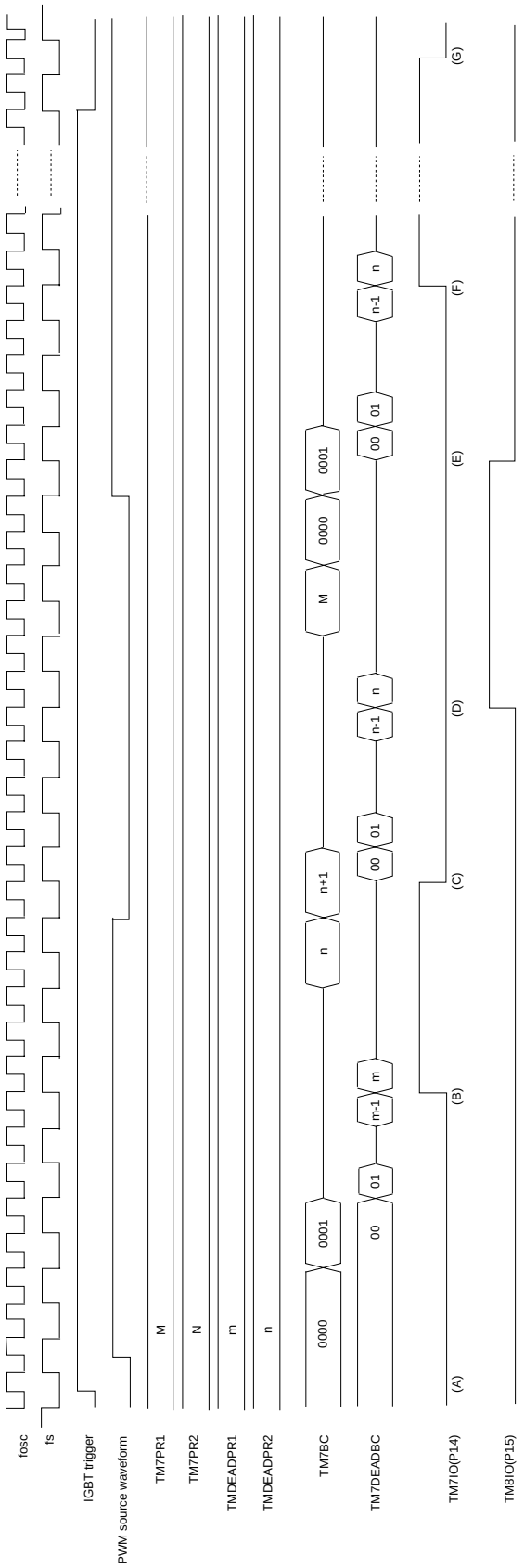


Figure 7-10-1 Count Timing of Dead Time IGBT Output (Timer 7)

Output waveform of the IGBT with dead time (at falling-edge standard)

(A) TM7IO = “L”, TM8IO = “L” until the IGBT trigger is input and becomes valid.

(B) After the trigger is input, and after 1 count clock at the falling edge of the next count clock + fosc x (value of the dead time preset register1 + 1) output voltage of TM7IO is increased.

(C) After the compare matching (the value of the binary counter matches that of TM7OC2), and after 1 count clock + 1 fosc clock, output voltage of TM7IO is decreased.

(D) After TM7IO output voltage is decreased, and after fosc x (value of the dead time preset register 2), output voltage of TM8IO is increased.

(D) After the compare matching (the value of the binary counter matches that of TM7OC1), and after 2 count clock + 1 fosc clock, output voltage of TM8IO is decreased.

(F) After TM8IO output voltage is decreased, and after fosc x (value of the dead time preset register1), output voltage of TM7IO is increased.

(G) When IGBT trigger becomes invalid, both TM7IO and TM8IO become “L” at the falling edge of the next count clock.

7-10-2 Setup Example

■Dead time IGBT Output Setup Example (Timer 7)

At the interrupt generation edge of the external interrupt 1 input signal, TM7IO and TM8IO output pins output the waveforms of 1/4 duty IGBT waveform at 200 Hz with 0.01ms, 0.02 ms dead time using timer 7. Select fosc/1 (at fosc = 8.0 MHz) as the clock source. Required period for one IGBT output waveform cycle depends on the set value of the compare register 1. "H" period of IGBT output standard waveform depends on the set value of a compare register 2. Dead time period depends on the value of the dead time preset register1, 2. An example setup procedure, with a description of each step is shown below.

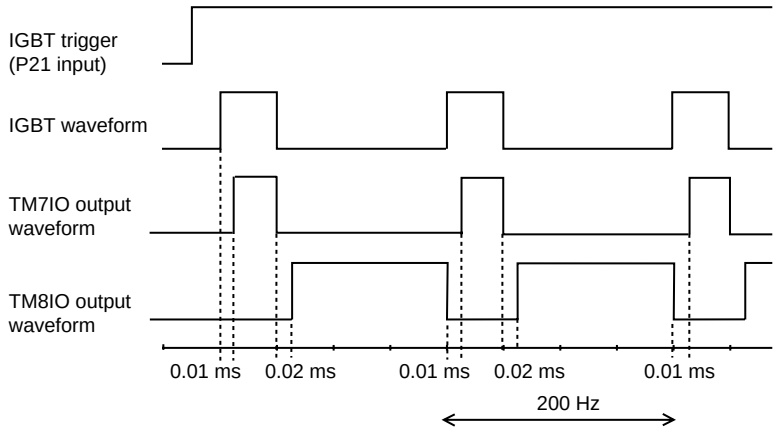


Figure 7-10-2 Output Waveform of TM7IO Output Pin and TM8IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the IGBT output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0= 11 TM8MD3 (x'3F6D') bp2 : TM78SEL = 1	(2) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "11" to select the dead time IGBT output. Set the TM78SEL flag of the timer 8 mode register 3 (TM8MD3) to "1" to select the timer 7 IGBT output.
(3) Set the dead time IGBT output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1 bp6 : T7PWMSL = 1	(3) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the source to clear binary counter. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a duty decision source of the IGBT output.

Setup Procedure	Description
(4) Select the IGBT trigger source TM7MD2 (x'3F79') bp1-0 : T7ICT1-0 = 00	(4) Select the external interrupt 1 (IRQ1) input as the generation source of the IGBT trigger by T7ICT1-0 flag of the TM7MD2 register.
(5) Select the Interrupt generation valid edge IRQ1ICR (x'3FE3') bp5 : REDG1 = 1	(5) Set the REDG1 flag of the external interrupt 1 control register (IRQ1ICR) to "1" to select the rising edge as a Interrupt generation valid edge.
(6) Select the IGBT trigger generation edge TM7MD2 (x'3F79') bp7 : T7ICEDG = 1	(6) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the IGBT trigger event as the specified edge of the external interrupt signal.
(7) Set the dead time edge. TM7MD3 (x'3F6C') bp4 : TM7EDG = 0	(7) Set the TM7EDG flag of the TM7MD3 register to "1" to select falling edge standard as the dead time edge.
(8) Set the interruput level. IRQ1ICR (x'3FE3') bp7-6 : IRQ1LV1-0= 10	(8) Set the interrupt level by the IRQ1LV1-0 flag of the IRQ1ICR register. If any interrupt request flag is already set, clear it.
(9) Enable the interrupt. IRQ1ICR (x'3FE3') bp1 : IRQ1IE = 1	(9) Set the IRQ1IE flag of the IRQ1ICR register to "1" to enable the interrupt.
(10) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(10) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 dividing as a count clock source by the TM7PS1-0 flag.
(11) Set the IGBT output cycle. TM7PR1 (x'3F75',x'3F74') = x'9C3F'	(11) Set the IGBT output cycle to the timer 7 preset register 1 (TM7PR1). To set 200 Hz by dividing 8.0 MHz, set as; 40000 - 1 = 39999 (x'9C3F') At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.

Setup Procedure	Description
(12) Set the "H" period of the IGBT output. TM7PR2 (x'3F7D',x'3F7C')= x'2710'	(12) Set the "H" period of the IGBT output to the timer 7 preset register 2 (TM7PR2). To set 1/4 duty of 40000 dividing, set as; 40000 / 4 = 10000 (x'2710') At the same time, the same value is loaded to the timer 7 compare register 2 (TM7OC2).
(13) Set the dead time. TM7DEADPR1 (x'3F7E') = x'50' TM7DEADPR2 (x'3F7F') = x'A0'	(13) Set the period between TM8IO falling to TM7IO rising to the timer 7 dead time preset register1(TM7DEAPR1), and set the period between TM7IO falling toTM8IO rising to the timer 7 dead time preset register2 (TM7DEAPR2). Set x'50' to the timer 7 dead time preset register1 for the period between TM7IO falling to TM8IO rising to be 0.02 ms. Set x'A0' to the timer 7 dead time preset register2 for the time between TM8IO falling to TM7IO rising to be 0.01 ms.
(14) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 bp5 : P1OMD5 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1 bp5 : P1DIR5 = 1	(14) Set the P1OMD4 and P1OMD5 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 and P15 pins as the special function pins. Set the P1DIR4 and P1DIR5 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports] Set P14, P15 as special function pins after setup (11) to (13).
(15) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(15) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7. After being "H" input to P21, IGBT waveform is output from P14, P15.

TM7BC counts up from x'0000'. The IGBT source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up. Once TM7BC value matches the TM7OC1 register value to be cleared, the IGBT source waveform outputs "H" and TM7BC counts up from x'0000' again. TM7IO pin outputs IGBT source waveform of one count clock delay . TM8IO pin outputs inverted IGBT source waveform of one count clock delay.

To output the IGBT output waveform from the large current pin TM7O, set the special function pin to output mode as follows (reffer ro setup example(2)). Set each of P5OMD1 flag and P5OMD3 flag of the port 5 output mode register (P5OMD) to "1" to select P51 pin and P53 pin as special function pins. Set P5DIR1and P5DIR3 flag of the port 5 direction control register to "1" to set output mode.

Set as TM7OC2 value ≤ TM7OC1 value.
When TM7OC2 value > TM7OC1 value, the IGBT output waveform is fixed as P14 = "H", P15 = "L" at falling edge standard.

7-11 16-bit Timer Synchronous Output

7-11-1 Operation

If the binary counter of the timer reaches the set value of the compare register, port 4 outputs the port 4 output latched data at the next count clock.

■16-bit Timer Synchronous Output Operation (Timer 7)
Port 4 outputs the port 4 output latched data at a TM7OC1 compare register reaches a binary counter or at an interrupt request generation by the full count overflow. Only port 4 can be used in this operation, and each bit can be set individually.

■Count Timing of Synchronous Output (Timer 7)

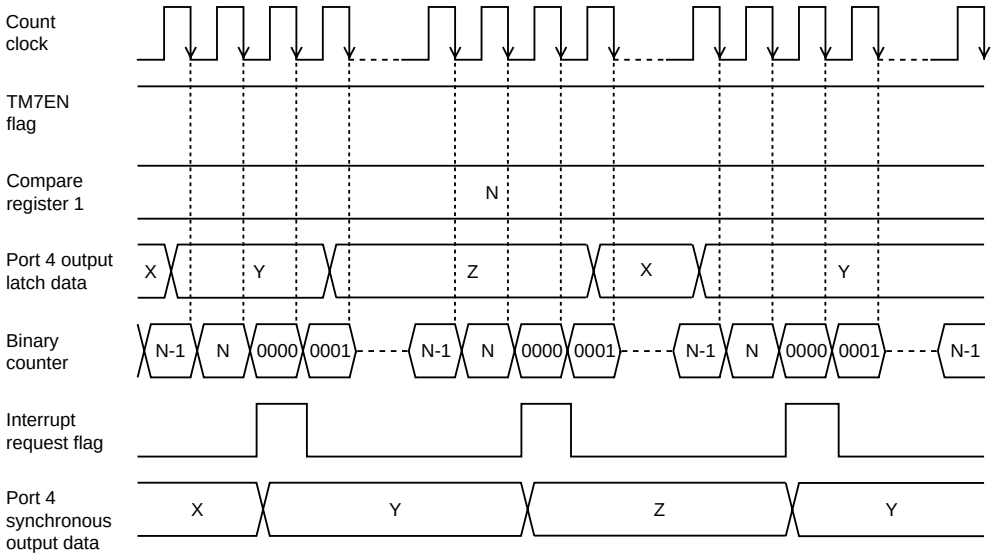


Figure 7-11-1 Count Timing of Synchronous Output (Timer 7)

Output pin outputs the port 4 output latch data at an interrupt request generation by the match of a binary counter and a compare register 1.

7-11-2 Setup Example

■Synchronous Output Setup Example (Timer 7)

Here is an example to output the port 4 latch data from the synchronous output pin constantly (in every 100 µs) with timer 7. As a clock source of timer 7, fs/4 (fosc=8 MHz) is selected.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 : SYOEVS1-0 = 01	(2) Set the SYOEVS1-0 flag of the pin control register (FLOAT) to "01" to set the synchronous output event to the timer 7 interrupt.
(3) Set the synchronous output pin. P4SYO (x'3F1E') = x'FF' P4DIR (x'3F34') = x'FF'	(3) Set the port 4 synchronous output control register (P4SYO) to x'FF' to set the synchronous output pin. (P47 to P40 : Synchronous output pin) Set the port4 direction control register (P4DIR) to x'FF' to set port 4 to output pin. Add pull-up resistor, if necessary. [☞ Chapter 4 I/O Ports]
(4) Select the timer clear factor. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the clear source for the binary counter.
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 01 bp3-2 : TM7PS1-0 = 10	(5) Select fs as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/4 dividing as a clock source by the TM7PS1-0 flag.
(6) Set the synchronous output event generation cycle. TM7PR1 (x'3F75',x'3F74')=x'0063'	(6) Set the synchronous output event generation cycle to the timer 7 preset register 1 (TM7PR1). To set 10 kHz by dividing 1 MHz, set as; 100 - 1 = 99 (x'0063') At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and TM7BC is initialized to x'0000'.

Setup Procedure	Description
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. If any data is written to the port 4 output register (P4OUT), TM7BC is set to the set value of TM7OC1 register and the synchronous output pin outputs data of port 4 in every time an interrupt request is generated.

7-12 16-bit Timer Capture

7-12-1 Operation

The value of binary counter is read out at the timing of the external interrupt input signal, or at the timing of the writing operation with an any value to the capture register.

■Capture Operation with External Interrupt Signal as a Trigger (Timer 7, Timer 8)
Input capture trigger is generated at the external interrupt signal that passed through the external interrupt interface block. The capture trigger is selected by the timer n mode register 2 (TMnMD2) and the external interrupt control register (IRQ0ICR, IRQ1ICR, IRQ2ICR, IRQ3ICR).
Selectable capture triggers and the interrupt flag setup are shown below.
Timer 7 can select the trigger from IRQ0 to 2, and timer 8 can select the trigger from IRQ0 to 3.

Table 7-12-1 Capture Trigger (timer 7)

Capture trigger source	Timer 7 mode register 2		External interrupt n control register (IRQnICR)	Both edges interrupt control register (EDGDT)		Interrupt activation edge of external interrupt n
	T7ICT1-0	T7ICEDG	REDGn (bp5)	EDGSEL3	EDGSEL2	
IRQ0 falling edge	00(IRQ0)	1	0	-	-	IRQ0 falling edge
IRQ0 rising edge	00(IRQ0)	1	1	-	-	IRQ0 rising edge
IRQ0 both edge	00(IRQ0)	0	0	-	-	IRQ0 falling edge
			1	-	-	IRQ0 rising edge
IRQ1 falling edge	01(IRQ1)	1	0	-	-	IRQ1 falling edge
IRQ1 rising edge	01(IRQ1)	1	1	-	-	IRQ1 rising edge
IRQ1 both edge	01(IRQ1)	0	0	-	-	IRQ1 falling edge
			1	-	-	IRQ1 rising edge
IRQ2 falling edge	10(IRQ2)	1	0	-	0	IRQ2 falling edge
IRQ2 rising edge	10(IRQ2)	1	1	-	0	IRQ2 rising edge
IRQ2 both edge(*)	10(IRQ2)	0	0	-	0	IRQ2 falling edge
			1	-	0	IRQ2 rising edge

Table 7-12-2 Capture Trigger (timer 8)

Capture trigger source	Timer 7 mode register 2		External interrupt n control register (IRQnICR)	Both edges interrupt control register (EDGDT)		Interrupt activation edge of external interrupt n
	T7ICT1-0	T7ICEDG	REDGn (bp5)	EDGSEL3	EDGSEL2	
IRQ0 falling edge	00(IRQ0)	1	0	-	-	IRQ0 falling edge
IRQ0 rising edge	00(IRQ0)	1	1	-	-	IRQ0 rising edge
IRQ0 both edge	00(IRQ0)	0	0	-	-	IRQ0 falling edge
			1	-	-	IRQ0 rising edge
IRQ1 falling edge	01(IRQ1)	1	0	-	-	IRQ1 falling edge
IRQ1 rising edge	01(IRQ1)	1	1	-	-	IRQ1 rising edge
IRQ1 both edge	01(IRQ1)	0	0	-	-	IRQ1 falling edge
			1	-	-	IRQ1 rising edge
IRQ2 falling edge	10(IRQ2)	1	0	-	0	IRQ2 falling edge
IRQ2 rising edge	10(IRQ2)	1	1	-	0	IRQ2 rising edge
IRQ2 both edge(*)	10(IRQ2)	0	0	-	0	IRQ2 falling edge
			1	-	0	IRQ2 rising edge
IRQ3 falling edge	11(IRQ3)	1	0	0	-	IRQ3 falling edge
IRQ3 rising edge	11(IRQ3)	1	1	0	-	IRQ3 rising edge
IRQ3 both edge(*)	11(IRQ3)	0	0	0	-	IRQ3 falling edge
			1	0	-	IRQ3 rising edge

The external interrupt 2, 3 (IRQ2, IRQ3) have the function of both edges interrupt. However, input capture can not be used together with both edges interrupt. [table 7-12-1, 7-12-2(*)]

Input capture signals of the 16-bit timers 7 and 8 are generated by fosc or fs. (When the timer's clock source is fosc, they are generated by fosc. Other than that, they are generated by fs.) Therefore, set TMnIO to TMnCKSMP of the TMnMD3 register when external event frequency (TMnIO input) is counted with event frequency higher than fs. As this setting cannnot count accurately if TMnIO is used as a clock count, set TMnCK1 and TMnCK0 of the TMnMD1 register to be TMnIO.

Switching the clock source to use fs as a system clock by dividing oscillation clock fosc requires extra attention.

When setup is as following (1), (2), and external interrupt valid edge is switched by program, interrupt request and capture trigger are generated.

(1) at switching the valid edge from the falling to the rising, when the interrupt pin is "H" level.

(2) at switching the valid edge from the rising to the falling, when the interrupt pin is "L" level.

This does not happen, if the interrupt edge is switched after the generation of an valid edge interrupt set in advance. But when the both edges interrupt function is used, this could happen. The noise influence should be considered when operating the interrupt flag on program.

[☞ Chapter 3 3-3-4. Specified Polarity Edge Interrupt]

■Capture Count Timing as a Both Edges of External Interrupt Signal is selected as a Trigger (Timer 7)

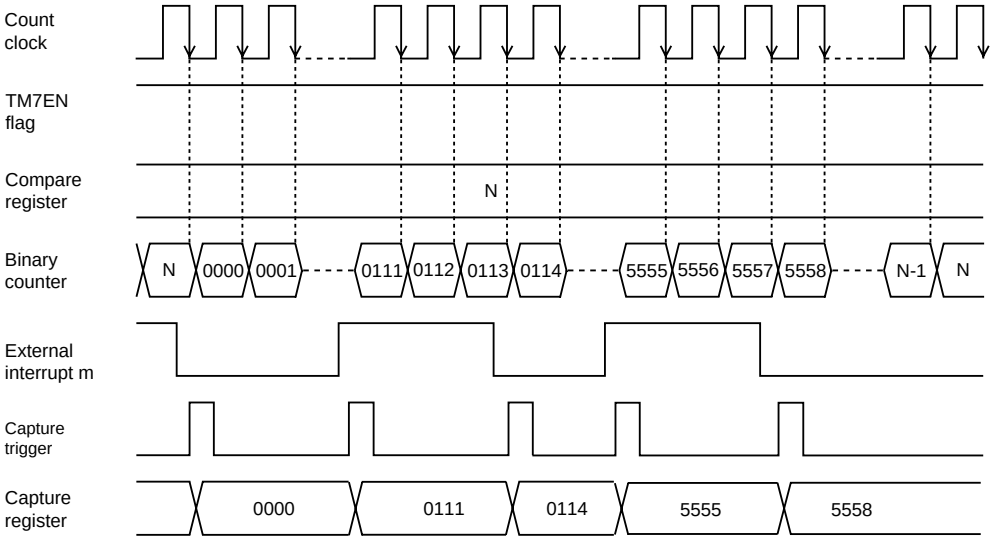


Figure 7-9-1 Capture Count Timing as an External Interrupt Signal is selected as a Trigger (Timer 7, Timer 8)

A capture trigger is generated at the both edges of the external interrupt m input signal. In synchronized with this capture trigger, the value of binary counter is loaded to the input capture register. The value loaded to the capture register is depending on the value of a binary counter at the falling edge of a capture trigger. When the specified edge is selected as a capture trigger source, a capture trigger is generated only at that edge. The other count timing is same as the count timing of the timer operation.

When the binary counter is used as a free counter which counts x'0000' to x'FFFF', set the compare register 1 to x'FFFF', or set the TMnBCR flag of the TM7MD2 or TM8MD3 register to "0".

Even if an event is generated before the value of the input capture register is read out, the value of the input capture register can be rewritten.

In the initial state after releasing the reset, the generation of trigger by the external interrupt signal is disabled. Set the TnICEN flag of the TMnMD2 register to "1" to enable the trigger generation.

■Capture Operation triggered by writing software (Timer 7, Timer 8)

A capture trigger can be generated by writing an arbitrary value to the input capture register (TMnIC). In synchronized with this capture trigger, the value of the binary counter is loaded to the input capture register.

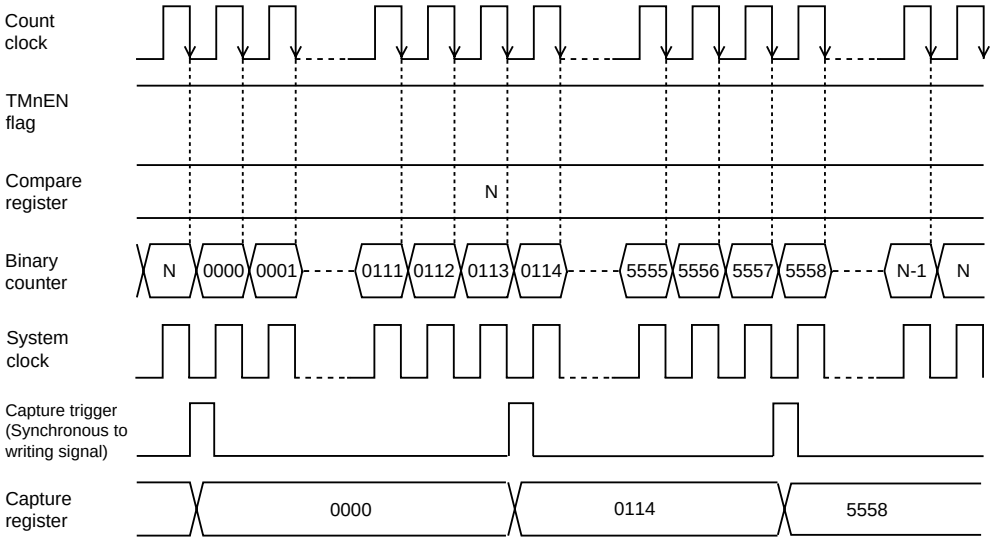


Figure 7-12-2 Capture Count Timing Triggered by Writing Software (Timer 7, Timer 8)

A capture trigger is generated at the writing signal to the input capture register. The writing signal is generated at the last cycle of the writing instruction. In synchronized with this capture trigger, the value of the binary counter is loaded to the input capture register. That value is depending on the value of the binary counter at the falling edge of the capture trigger. The other timing is the same as the timer operation.

The writing to the input capture register to generate a capture trigger should be done with a 8-bit access instruction of the TMnICL register or the TMnICH register.
At this time, data is not actually written to the TMnIC register.

On hardware, there is no flag to disable the capture operation triggered by writing software. Capture operation is enabled regardless of the TnICEN flag of the TMnMD2 register.

7-12-2 Setup Example

■Capture Function Setup Example (Timer 7, Timer 8)
Pulse width measurement is enabled by loading the value of the binary counter to the capture register at the interrupt generation edge of the external interrupt 0 input signal with timer 7. In the example setup procedure shown below, rising edge is selected to be an interrupt generation edge.

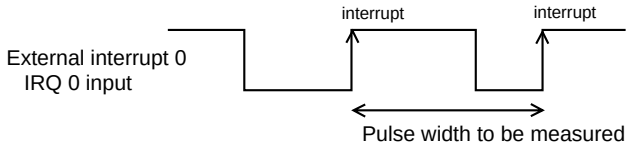


Figure 7-12-3 Pulse Width Measurement of External Interrupt 0

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the timer clear condition. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(2) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as the source to clear the binary counter.
(3) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(3) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. And select 1/1 (no dividing) of fosc as the count clock source by the TM7PS1-0 flag.
(4) Select the capture trigger interrupt source. TM7MD2 (x'3F79') bp1-0 : T7ICT1-0 = 00	(4) Select the external interrupt 0 (IRQ0) input as the generation source of capture trigger by the T7ICT1-0 flag of the TM7MD2 register.
(5) Select the interrupt generation valid edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(5) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as the interrupt generation valid edge.

Setup Procedure	Description
(6) Select the capture trigger generation edge. TM7MD2 (x'3F79') bp7 : T7ICEDG = 1	(6) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the external interrupt valid edge as a capture trigger source.
(7) Set the compare register. TM7PR1(x'3F75',x'3F74') = x'FFFF'	(7) Set the timer 7 preset register 1 (TM7PR1) to x'FFFF'. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(8) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(8) Set the interrupt level by the IRQ0LV1-0 flag of the IRQ0IR register. If any interrupt request flag is set already, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(9) Enable the interrupt by setting the IRQ1IE flag of the IRQ0ICR register to "1".
(10) Enable the capture trigger generation. TM7MD2 (x'3F79') bp2 : T7ICEN = 1	(10) Enable the capture trigger generation by setting the T7ICEN flag of the TM7MD2 register to "1".
(11) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. At the timing of the rising edge of the external interrupt 0 input signal, the value of TM7BC is loaded to the TM7IC register. At that time, the pulse width between rising edge of the external interrupt input signal can be measured by reading the value of TM7IC register through interrupt service routine, and calculating the difference between the capture values.

7-13 Cascade Connection

7-13-1 Operation

Cascading timers 7 and 8 forms a 32-bit timer.

■16-bit Timer Cascade Connection Operation (Timer 7 + Timer 8)
Timer 7 and timer 8 are combined to be a 32-bit timer. Cascading timer is operated at clock source of timer 7 which are lower 16 bits.

Table 7-13-1 Timer Functions at Cascade Connection

	Timer 7 + Timer 8 (32 bit)
Interrupt source	TM8IRQ1, TM8IRQ2
Timer operation	√
Event count	√ (TM7IO input)
Timer pulse output	√ (TM8IO output)
PWM output	√
Synchronous output	-
Capture function	√
Pulse width measurement	√
Clock source	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16
fosc : Machine clock (High frequency oscillation) fs : System clock [☞Chapter 2 2-5 Clock Switching]	

* At cascade connection, timer 8 interrupt factor is only counter-clear.

At cascade connection, the binary counter and the compare register are operated as a 32 bit register. At operation, set the TM7EN flag of the lower 16-bit timers to "1" to be operated. Also, select the clock source with the lower 16-bit timer.
Other setup and count timing are the same as the 16-bit timer at independently operation.

When timer 7 and timer 8 are used in cascade connection, timer 8 is used as an interrupt request flag. Timer pulse output of timer 7 is "L" fixed output.
Timer 7 interrupt should be disabled as interrupt request of timer 7 is generated.

7-13-2 Setup Example (Timer Operation)

■Cascade Connection Timer Setup Example (Timer 7+ Timer 8)

Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 7 and timer 8, as a 32-bit timer is shown. An interrupt is generated in every 100000 cycles (40 ms) by selecting source clock to fs/4 (fosc=20 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 :TM7EN = 0 TM8MD1 (x'3F88') bp7 :TM8EN = 0	(1) Set the TM7EN flag of the timer 7 mode register (TM7MD1) to "0", the TM8EN flag of the timer 8 mode register to "0" to stop timer 7 and timer 8 counting.
(2) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 :TM7BCR = 1	(2) Set the TM7BCR flag of TM7MD2 register to "1" to select compare match as a clear source of the binary counter.
(3) Select the normal lower timer operation. TM7MD2 (x'3F79') bp2 :TM7CEN = 0 TM7MD3 (x'3F6C') bp1-0 :TM7OUT1-0= 00	(3) Set the TM7ICEN flag of the TM7MD2 register to "0", the TM7OUT1-0 flag of TM7MD3 register to "00" to select normal timer operation.
(4) Set the cascade connection. TM8MD1 (x'3F88') bp6 :TM8CAS = 1	(4) Set the TM8CAS flag of the TM8MD1 register to "1" to connect timer 7 and timer 8 in cascade connection.
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 :TM7CK1-0 = 01 bp3-2 :TM7PS1-0 = 10	(5) Select fs as the clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/4 dividing of fs as the count clock source by the TM7PS1-0 flag.
(6) Set the interrupt generation cycle. TM7PR1(x'3F75', x'3F74')=x'869F' TM8PR1(x'3F85', x'3F84')=x'0001'	(6) Set the timer 7 preset register 1 (TM7PR1) and timer 8 preset register 1 (TM8PR1) to the interrupt generation cycle (100000 cycles - 1). At that time, the same values as the preset registers are loaded to the timer compare register1 (TM7OC1) and timer 8 compare register 1(TM8OC1), and the binary counters are initialized to x'0000'.

Setup Procedure	Description
(7) Disable the lower timer interrupt. TM7ICR (x'3FF1') bp1 :TM7IE = 0	(7) Set the TM7IE flag of the timer 7 interrupt control register (TM7ICR) to "0" to disable the interrupt.
(8) Set the level of the upper timer interrupt. TM8ICR (x'3FF3') bp7-6 :TM8LV1-0 = 10	(8) Set the interrupt level by the TM8LV1-0 flag of the timer 8 interrupt control register (TM8ICR). If any interrupt request flag is already set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the upper timer interrupt. TM8ICR (x'3FF3') bp1 :TM8IE = 1	(9) Set the TM8IE flag of the TM8ICR register to "1" to enable the interrupt.
(10) Start the lower timer operation. TM7MD1 (x'3F78') bp4 :TM7EN = 1	(10) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BCL + TM7BCH + TM8BCL + TM8BCH counts up from x'00000000' as a 32-bit timer.
When TM7BCL + TM7BCH + TM8BCL + TM8BCH reaches the set value of TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H register, the timer 8 interrupt request flag is set at the next count clock, and the value of TM7BCL + TM7BCH + TM8BCL + TM8BCH becomes x'00000000' to restarts count up.

7-13-3 Setup Example (PWM Operation)

■Cascade Connection PWM Output Setup Example (Timer 7+ Timer 8)

The TM8IO output pin outputs the 1/10 duty PWM output waveform at 1/60 Hz with the cascade connection of timer 7 and timer 8, as a 32-bit timer. Select fosc/1 (fosc = 8 MHz, at operation) as a clock source. One cycle of the PWM output waveform is depending on the set value of the compare register 1. "H" period of the PWM output waveform is depending on the set value of the compare register 2.

An example setup procedure, with a description of each step is shown below.

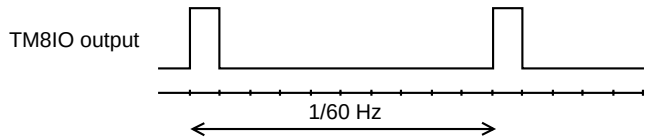


Figure 7-13-1 Output Waveform of TM8IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0 TM8MD1 (x'3F88') bp7 : TM8EN = 0	(1) Set the TM7EN flag of the timer 7 mode register (TM7MD1) to "0", the TM8EN flag of the timer 8 mode register (TM8MD1) to "0" to stop timer 7 and timer 8 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp5 :P1OMD5 = 1 P1DIR (x'3F31') bp5 : P1DIR5 = 1	(2) Set the P1OMD5 flag of the port 1 output mode register (P1OMD) to "1" to set the P15 pin as a special function pin. Set the P1DIR5 flag of the port 1 direction control register (P1DIR) to "1" for output mode. Add pull-up / pull-down resistor, if necessary. [☞ Chapter 4 I/O Ports]
(3) Set the cascade connection. TM8MD1 (x'3F88') bp6 :TM8CAS = 1	(3) Set the TM8CAS flag of the TM8MD1 register to "1" to connect timer 7 and timer 8 in cascade connection.
(4) Set the PWM output. TM7MD3 (x'3F6C') bp1-0 : TM7OUT1-0 = 01	(4) Set the TM7OUT1-0 flag of the timer 7 mode register 3 (TM7MD3) to "01" to select the PWM output.

Setup Procedure	Description
(5) Set the high precision PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1 bp6 : T7PWMSL = 1	(5) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as a clear source of binary counter. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a duty of PWM output.
(6) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(6) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 dividing as a count clock source by the TM7PS1-0 flag.
(7) Set the PWM output cycle. TM7PR1(x'3F75',x'3F74')= x'37FF' TM8PR1(x'3F85',x'3F84')= x'1C9C'	(7) Set the PWM output cycle to the timer 7 preset register 1 (TM7PR1), the timer 8 preset register 1 (TM8PR1). To set 1/60 Hz by dividing 8 MHz, set as; 480,000,000 - 1 = 479,999,999 (x'1C9C37FF') At the same time, the same values as the preset registers are loaded to the timer 7 compare register 1 (TM7OC1) and timer 8 compare register 1 (TM8OC1), and the timer 7 binary counter (TM7BC) and timer 8 binary counter (TM8BC) are initialized to x'0000'.
(8) Set the "H" period of the PWM output. TM7PR2 (x'3F7D',x'3F7C')=x'6C00' TM8PR2 (x'3F8D',x'3F8C')=x'02DC'	(8) Set the "H" period of the PWM output to the timer 7 preset register 2 (TM7PR2) and timer 8 preset register 2 (TM8PR2). To set 1/10 duty of 480,000,000 dividing, set as; 480,000,000 / 10 = 48,000,000 (x'02DC6C00') At the same time, the same values as the pre set registers are loaded to the timer 7 compare register 2 (TM7OC2) and the timer 8 compare register 2 (TM8OC2).
(9) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(9) Set the TM7EN flag of the TM7MD1 register to "1" to operate timer 7 and timer 8.

TM7BCL + TM7BCH + TM8BCL + TM8BCH counts up from x'00000000' as a 32-bit timer.
The PWM source waveform outputs "H" until TM7BCL + TM7BCH + TM8BCL + TM8BCH reaches the set value of the TM7OC2L + TM7OC2H + TM8OC2L + TM8OC2H register. Once they match, it outputs "L". After that, TM7BCL + TM7BCH + TM8BCL + TM8BCH continues to count up, once TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H reaches the TM7BCL + TM7BCH + TM8BCL + TM8BCH register to be cleared, the PWM source waveform outputs "H" again, and TM7BCL + TM7BCH + TM8BCL + TM8BCH counts up from x'00000000' again. TM8IO pin outputs one count clock delay of the PWM source waveform.

In the initial state of the PWM output, "L" output is changed to "H" output as the PWM output is selected by the TM7OUT1-0 flag of the TM7MD3 register.

Set value should be set as;
TM7OC2L + TM7OC2H + TM8OC2L + TM8OC2H ≤
TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H.
If it is set as;
TM7OC2L + TM7OC2H + TM8OC2L + TM8OC2H >
TM7OC1L + TM7OC1H + TM8OC1L + TM8OC1H,
the PWM output is a "H" fixed output.

Chapter 8 Time Base Timer / 8-bit Free-running Timer

8-1 Overview

This LSI has a time base timer and a 8-bit free-running timer (timer 6).
Time base timer is a 15-bit timer counter, which cannot stop operation, except with a 8-bit free running timer at stand-by mode (STOP mode).

8-1-1 Functions

Table 8-1-1 shows the clock sources and the interrupt generation cycles that timer 6 and time base timer can use.

Table 8-1-1 Clock Source and Generation Cycle

	Time base timer	Timer 6 (8-Bit free-running)
8-bit timer operation	-	√
Interrupts	TBIRQ	TM6IRQ
Clock source	fosc fx	fosc fx fs fosc X $1/2^{12}$ (*1) fosc X $1/2^{13}$ (*1) fx X $1/2^{12}$ (*2) fx X $1/2^{13}$ (*2)
Interrupt generation cycle	fosc X $1/2^{7}$ (*1) fosc X $1/2^{8}$ (*1) fosc X $1/2^{9}$ (*1) fosc X $1/2^{10}$ (*1) fosc X $1/2^{13}$ (*1) fosc X $1/2^{15}$ (*1) fx X $1/2^{7}$ (*2) fx X $1/2^{8}$ (*2) fx X $1/2^{9}$ (*2) fx X $1/2^{10}$ (*2) fx X $1/2^{13}$ (*2) fx X $1/2^{15}$ (*2)	The interrupt generation cycle is decided by the arbitrary value written to TM6OC.
fosc : Machine clock (High speed oscillation) fx : Machine clock (Low speed oscillation) fs : System clock [☞ Chapter 2 2-5. Clock Switching] - *1 can be used when a clock source of time base timer is selected to 'fosc'. - *2 can be used when a clock source of time base timer is selected to 'fx'. - Time base timer and timer 6 cannot stop timer 6 counting.		

8-1-2 Block Diagram

■Timer 6, Time Base Timer Block Diagram

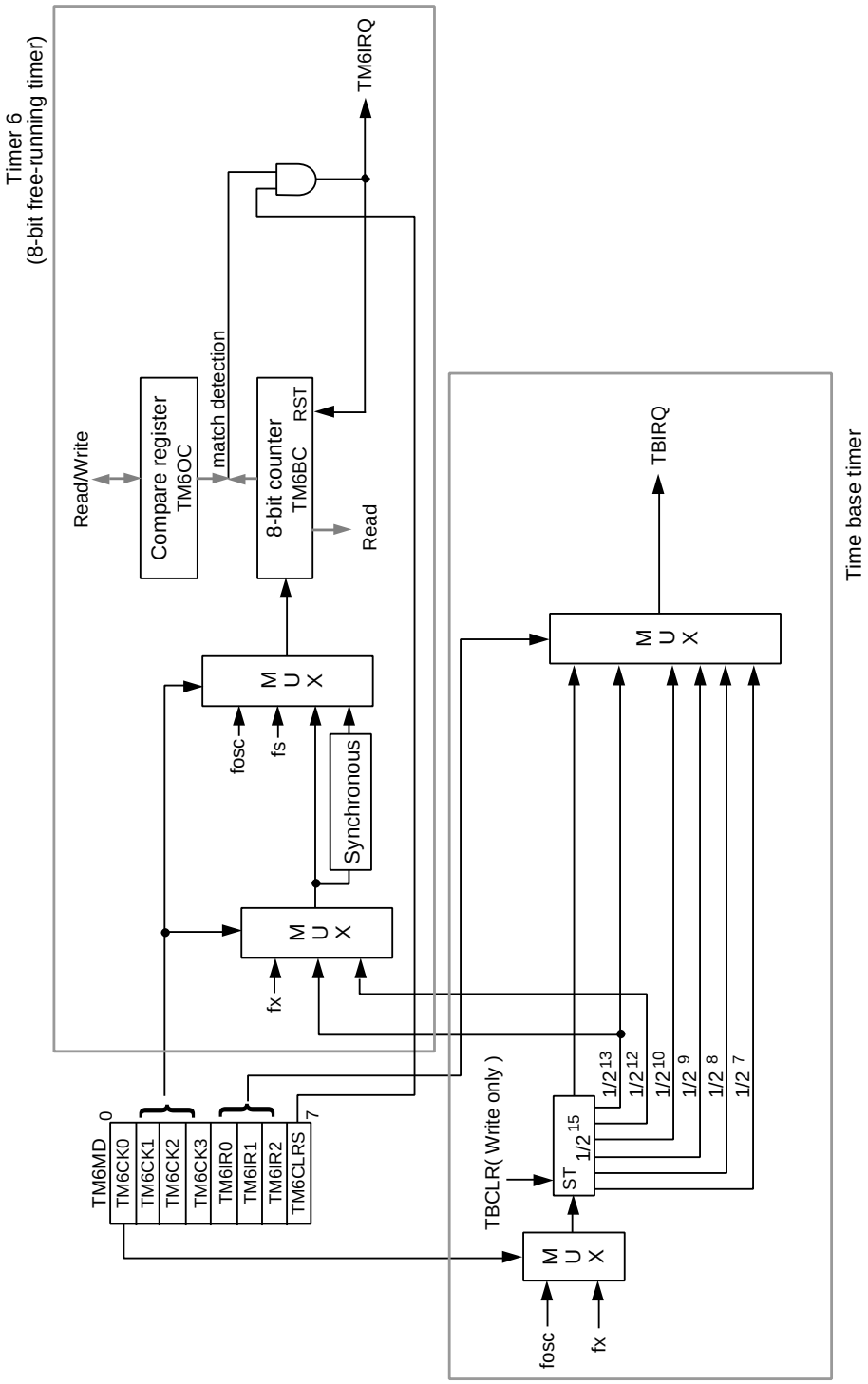


Figure 8-1-1 Block Diagram (Timer 6, Time Base Timer)

8-2 Control Registers

Timer 6 consists of binary counter (TM6BC), compare register (TM6OC), and is controlled by mode register (TM6MD). Time base timer is controlled by mode register (TM6MD) and time base timer clear register (TBCLR).

8-2-1 Control Registers

Table 8-2-1 shows the registers that control timer 6, time base timer.

Table 8-2-1 Control Registers

	Register	Address	R/W	Function	Page
Timer 6	TM6BC	x'03F68'	R	Timer 6 binary counter	VIII - 5
	TM6OC	x'03F69'	R/W	Timer 6 compare register	VIII - 5
	TM6MD	x'03F6A'	R/W	Timer 6 mode register	VIII - 6
	TM6ICR	x'03FEF'	R/W	Timer 6 interrupt control register	III - 30
Timer base timer	TM6MD	x'03F6A'	R/W	Timer 6 mode register	VIII - 6
	TBCLR	x'03F6B'	W	Time base timer clear control register	VIII - 5
	TBICR	x'03FF0'	R/W	Time base interrupt control register	III - 31

R/W : Readable / Writable
R : Readable only
W : Writable only

8-2-2 Programmable Timer Registers

Timer 6 is a 8-bit programmable counter.
Programmable counter consists of compare register (TM6OC) and binary counter (TM6BC).

Binary counter is a 8-bit up-counter. When the TM6CLRS flag of the timer 6 mode register (TM6MD) is "0" and the interrupt cycle data is written to the compare register (TM6OC), the timer 6 binary counter (TM6BC) is cleared to x'00'.

■Timer 6 Binary Counter (TM6BC)

	7	6	5	4	3	2	1	0	
TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	(At reset : X X X X X X X X)

Figure 8-2-1 Timer 6 Binary Counter (TM6BC : x'03F68', R)

■Timer 6 Compare Register (TM6OC)

	7	6	5	4	3	2	1	0	
TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	(At reset : X X X X X X X X)

Figure 8-2-2 Timer 6 Compare Register (TM6OC : x'03F69', R/W)

Time base timer cannot stop counting but the software can reset its operation. Time base timer can be cleared by writing an arbitrary value to the time base timer clear control register (TBCLR).

■Time Base Timer Clear Control Register (TBCLR)

	7	6	5	4	3	2	1	0	
TBCLR	-	-	-	-	-	-	-	-	(For writing only)

Figure 8-2-3 Time Base Timer Clear Control Register (TBCLR : x'03F6B')

8-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 6 and time base timer.

■Timer 6 Mode Register (TM6MD)

	7	6	5	4	3	2	1	0	
TM6MD	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0	(At reset : 0 0 0 0 0 0 0 0)

TM6CKS0	Time base timer clock source selection
0	fosc
1	fx

TM6CK3	TM6CK2	TM6CK1	Timer 6 clock source selection
0	0	0	fosc
		1	fs
	1	0	fx
		1	Synchronous fx
1	0	0	Time base selection clock × $1/2^{13}$
		1	Synchronous time base selection clock × $1/2^{13}$
	1	0	Time base selection clock ×$1/2^{12}$
		1	Synchronous time base selection clock × $1/2^{12}$

TM6IR2	TM6IR1	TM6IR0	Time base timer interrupt cycle selection
0	0	0	Time base selection clock × $1/2^{7}$
		1	Time base selection clock × $1/2^{8}$
	1	0	Time base selection clock × $1/2^{9}$
		1	Time base selection clock × $1/2^{10}$
1	0	-	Time base selection clock × $1/2^{13}$
	1		Time base selection clock × $1/2^{15}$

TM6CLRS	Timer 6 binary counter clear selection flag
0	Enable the initialization of TM6BC as TM6OC is written
1	Disable the initialization of TM6BC as TM6OC is written

* TM6IRQ is disable as TM6CLRS = 0,
TM6IRQ is enable as TM6CLRS = 1.

Figure 8-2-4 Timer 6 Mode Register (TM6MD : x'03F6A', R/W)

8-3 8-bit Free-running Timer

8-3-1 Operation

■8-bit Free-running Timer (Timer 6)

The generation cycle of the timer interrupt should be set in advance, by the set value of the compare register (TM6OC) and the clock source selection. When the binary counter (TM6BC) reaches the set value of the compare register, an interrupt request is generated at the next count clock and the binary counter is cleared to restart count up from x'00'.

Table 8-3-1 shows selectable clock sources.

Table 8-3-1 Clock Source at Timer Operation (Timer 6)

Clock source	One count time
fosc	50 ns
fx	30.5 µs
fs	100 ns
fosc X $1/2^{12}$	204.8 µs
fosc X $1/2^{13}$	409.6 µs
fx X $1/2^{12}$	125 ms
fx X $1/2^{13}$	250 ms
fosc = 20(MHz) fx = 32.768(kHz) fs = fosc/2 = 10 MHz	

Timer 6 cannot stop the operation.

■8-bit Free-running Timer as a 1 minute-timer, a 1 second-timer

Table 8-3-2 shows the clock source selection and the TM6OC register setup, when a 8-bit free-running timer is used as a 1 minute-timer, a 1 second-timer.

Table 8-3-2 1 minute-timer, 1 second-timer (Timer 6) Setup

Interrupt Generation Cycle	Clock Source	TM6OC Register
1 min	$fx \times 1/2^{13}$	X'EF'
1 s	$fx \times 1/2^{12}$	X'07'
	$fx \times 1/2^{13}$	X'03'
fx = 32.768(kHz)		

When the 1 minute-timer (1 m.) is set on Table 8-3-2., the bp1 waveform frequency (cycle) of the TM6BC register is 1 Hz (1 s.). So, that can be used for adjusting the seconds.

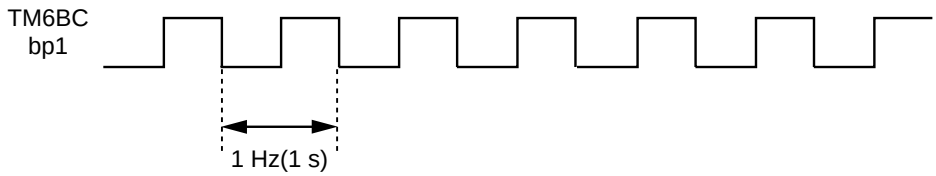


Figure 8-3-1 Waveform of TM6BC Register bp1 (Timer 6)

■Count Timing of Timer Operation (Timer 6)

Binary counter counts up with the selected clock source as a count clock.

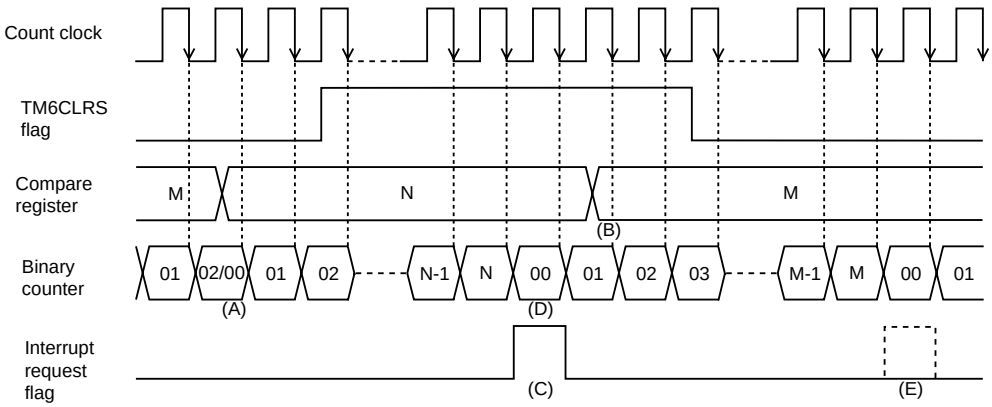


Figure 8-3-2 Count Timing of Timer Operation (Timer 6)

(A) When any data is written to the compare register as the TM6CLRS flag is "0", the binary counter is cleared to x'00'.

(B) Even if any data is written to the compare register as the TM6CLRS flag is "1", the binary counter is not changed.

(C) When the binary counter reaches the value of the compare register as the TM6CLRS flag is "1", an interrupt request flag is set at the next count clock.

(D) When an interrupt request flag is set, the binary counter is cleared to x'00' and restarts the counting.

(E) Even if the binary counter reaches the value of the compare register as the TM6CLRS flag is "0", no interrupt request flag is set.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared at the next count clock.
So set the compare register as :

Compare register setting = (count till the interrupt request -1)

If the fx input is selected as a clock source and the value of timer 6 binary counter is read out at operation, an incorrect value could be read out. To prevent this, select a synchronous fx as the count clock source. But if the synchronous fx is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

If the smaller value than the binary counter is set to the compare register at counting operation, the binary counter continues counting till overflow.

8-3-2 Setup Example

■Timer Operation Setup (Timer 6)

Timer 6 generates interrupts constantly for timer function. Interrupts are generated in every 250 dividing (25 µs) by selecting fs (fosc = 20 MHz at operation) as clock source.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Enable the binary counter initialization. TM6MD (x'3F6A') bp7 : TM6CLRS = 0	(1) Set the TM6CLRS flag of the timer 6 mode register (TM6MD) to "0". At that time, the initialization of the timer 6 binary counter (TM6BC) is enabled.
(2) Select the clock source. TM6MD (x'3F6A') bp3-1 : TM6CK3-1 = 001	(2) Clock source can be selected by the TM6CK3-1 flag of the TM6MD register. Actually, fx is selected.
(3) Set the interrupt generation cycle. TM6OC (X'3F69') = x'F9'	(3) Set the interrupt generation cycle to the timer 6 compare register (TM6OC). At that time, TM6BC is initialized to x'00'.
(4) Enable the interrupt request generation. TM6MD (x'3F6A') bp7 : TM6CLRS = 1	(4) Set the TM6CLRS flag of the TM6MD register to "1" to enable the interrupt request generation.
(5) Set the interrupt level. TM6ICR (x'3FEF') bp7-6 : TM6LV1-0 = 01	(5) Set the interrupt level by the TM6LV1-0 flag of the timer 6 interrupt control register (TM6ICR). If the interrupt request flag may be already set, clear them. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM6ICR (x'3FEF') bp1 : TM6IE = 1	(6) Set the TM6IE flag of the TM6ICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

As TM6OC is set, TM6BC is initialized to x'00' to count up.
When TM6BC matches TM6OC, the timer 6 interrupt request flag is set at the next count clock and TM6BC is cleared to x'00' to restart counting.

If the TM6CLRS flag of the TM6MD register is set to "0", TM6BC can be initialized at every rewriting of TM6OC register, but in that state the timer 6 interrupt is disabled. If the timer 6 interrupt should be used, set the TM6CLRS flag to "1" after rewriting the TM6OC register.

On the timer 6 clock source selection, if the time base timer output or the time base timer synchronous output is selected, the clock setup of time base timer is necessary.

8-4 Time Base Timer

8-4-1 Operation

■Time Base Timer (Time Base Timer)
Interrupt is constantly generated by a selected clock source and a interrupt generation cycle.
Table 8-4-1 shows the interrupt generation cycle in combination with the clock source ;

Table 8-4-1 Selection of Time Base Timer Interrupt Generation Cycle

Selected clock source	Interrupt generation cycle	
fosc	fosc X $1/2^7$	6.4 µs
	fosc X $1/2^8$	12.8 µs
	fosc X $1/2^9$	25.6 µs
	fosc X $1/2^{10}$	51.2 µs
	fosc X $1/2^{13}$	409.6 µs
	fosc X $1/2^{15}$	1.64 ms
fx	fx X $1/2^7$	3.9 ms
	fx X $1/2^8$	7.8 ms
	fx X $1/2^9$	15.6 ms
	fx X $1/2^{10}$	31.2 ms
	fx X $1/2^{13}$	250 ms
	fx X $1/2^{15}$	1 s
fosc = 20(MHz) fx = 32.768(kHz)		

■Count Timing of Timer Operation (Time Base Timer)

The counter counts up with the selected clock source as a count clock.

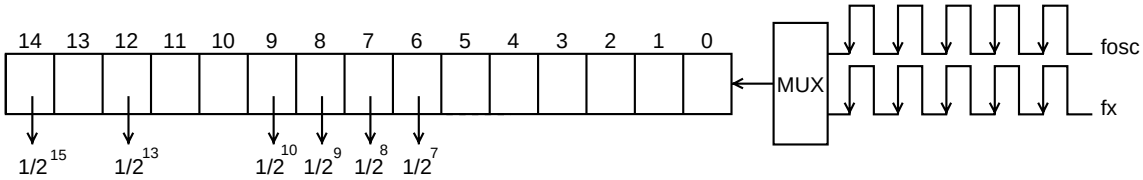


Figure 8-4-1 Count Timing of Timer Operation (Time Base Timer)

When the selected interrupt cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set.

An interrupt may be generated at switching of the clock source. Enable the interrupt after switching the clock source.

Time base timer cannot stop the operation.
The initialization can be done by writing an arbitrary value to the time base timer clear control register (TBCLR).

8-4-2 Setup Example

■Timer Operation Setup (Time Base Timer)

An interrupt can be generated constantly with time base timer in the selected interrupt cycle. The interrupt generation cycle is fosc × $1/2^{13}$(0.977 ms : fosc = 8.38 MHz) to generate interrupts.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the clock source. TM6MD (x'3F6A') bp0 : TM6CK0 = 0	(1) Select fosc as a clock source by the TM6CK0 flag of the timer 6 mode register (TM6MD).
(2) Select the interrupt generation cycle. TM6MD (x'3F6A') bp6-4 : TM6IR2-0 = 100	(2) Select the selected clock × $1/2^{13}$ as an interrupt generation cycle by the TM6IR2-0 flag of the TM6MD register.
(3) Initialize the time base timer. TBCLR (x'3F6B') = x'00'	(3) Write value to the time base timer clear control register (TBCLR) to initialize time base timer.
(4) Set the interrupt level. TBICR (x'3FF0') bp7-6 : TBLV1-0 = 01	(4) Set the interrupt level by the TBLV1-0 flag of the time base interrupt control register (TBICR). If any interrupt request flag may be already set, clear them. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(5) Enable the interrupt. TBICR (x'3FF0') bp1 : TBIE = 1	(5) Set the TBIE flag of the TBICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

When the selected interrupt generation cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

Chapter 9 Watchdog Timer

9

9-1 Overview

This LSI has a watchdog timer. This timer is used to detect software processing errors. It is controlled by the watchdog timer control register (WDCTR). And, once an overflow of watchdog timer is generated, a watchdog interrupt (WDIRQ) is generated. If the watchdog interrupt is generated twice, consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

9-1-1 Block Diagram

■Watchdog Timer Block Diagram

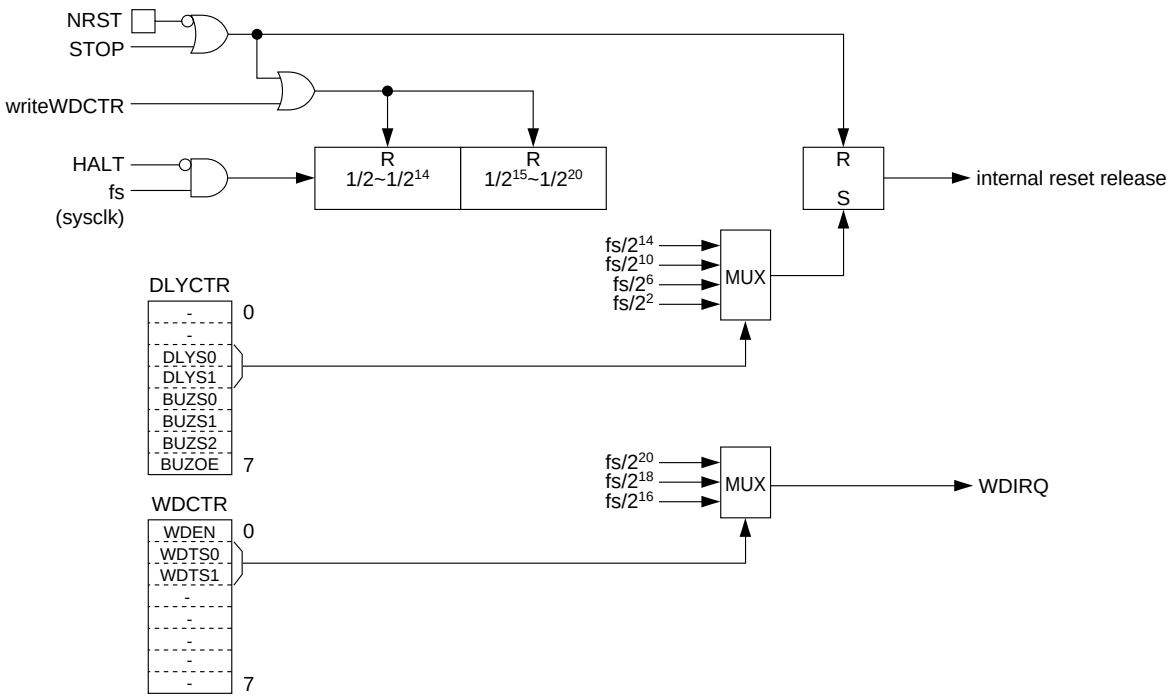


Figure 9-1-1 Block Diagram (Watchdog Timer)

The watchdog timer is also used as a timer to count the oscillation stabilization wait time. This is used as a watchdog timer except at recovering from STOP mode and at reset releasing.
The watchdog timer is initialized at reset or at STOP mode, and counts system clock (fs) as a clock source from the initial value (x'0000'). The oscillation stabilization wait time is set by the oscillation stabilization control register (DLYCTR). After the oscillation stabilization wait time is over, counting is continued as a watchdog timer. [☞ Chapter 2 2-6. Reset]

9-2 Control Registers

The watchdog timer is controlled by the watchdog timer control register (WDCTR).

■Watchdog Timer Control Register (WDCTR)

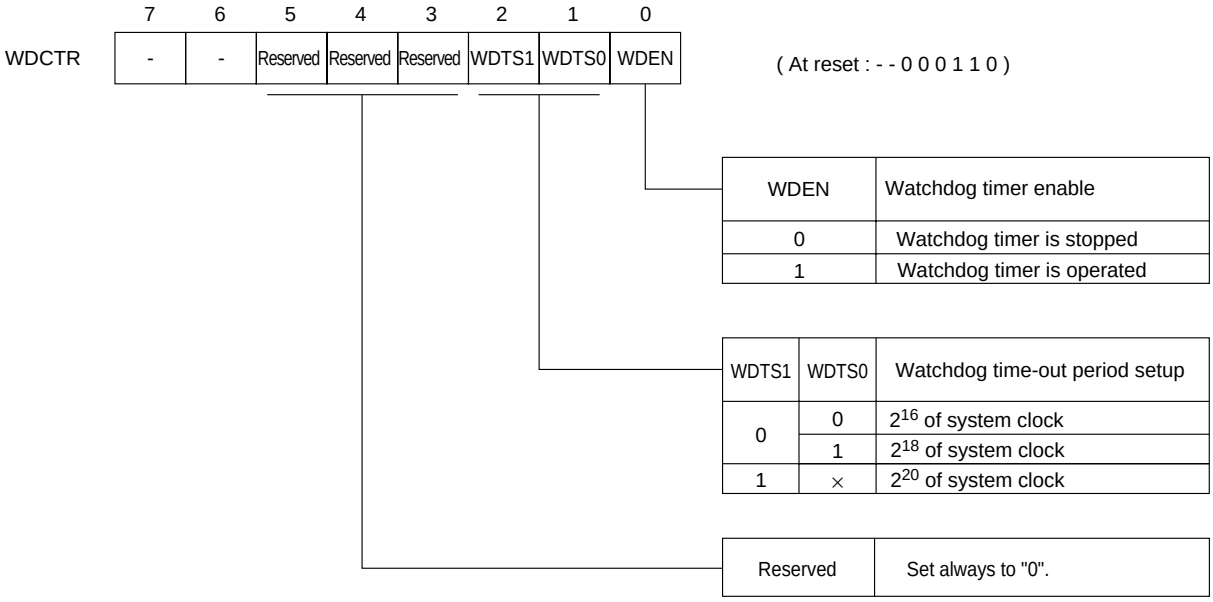

7 6 5 4 3 2 1 0
WDCTR
- - Reserved Reserved Reserved WDTS1 WDTS0 WDEN
(At reset : - - 0 0 0 1 1 0)
WDEN Watchdog timer enable
0 Watchdog timer is stopped
1 Watchdog timer is operated
WDTS1 WDTS0 Watchdog time-out period setup
0 0 2^16 of system clock
1 2^18 of system clock
1 × 2^20 of system clock
Reserved Set always to "0".

Figure 9-2-1 Watchdog Timer Control Register (WDCTR : x'03F02', R/W)

9-3 Operation

9-3-1 Operation

The watchdog timer counts system clock (fs) as a clock source. If the watchdog timer is overflowed, the watchdog interrupt (WDIRQ) is generated as an non maskable interrupt (NMI). At reset, the watchdog timer is stopped, but once the operation is enabled, it cannot be stopped except at reset. The watchdog timer control register (WDCTR) sets when the watchdog timer is released or how long the time-out period should be.

When watchdog clear is generated during time-out period, it is regarded as an error and the watchdog interrupt (WDIRQ) is generated.

If the watchdog interrupt (WDIRQ) is generated twice consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

The watchdog timer cannot stop, once it starts operation.

■Usage of Watchdog Timer

When the watchdog timer is used, constant clear in program is needed to prevent an overflow of the watchdog timer. As a result of the software failure, the software cannot execute in the intended sequence, thus the watchdog timer overflows to detect errors.

Programming of the watchdog timer is generally done in the last step of its programming.

■How to Detect Incorrect Code Execution

The watchdog timer is executed to be cleared in the certain cycle on the correct code execution. In this LSI, the watchdog timer detects errors when,

(1) the watchdog timer overflows.

When the watchdog timer detects any error, the watchdog interrupt (WDIRQ) is generated as a non maskable interrupt (NMI).

■How to Clear Watchdog Timer

The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR). The watchdog timer can be cleared regardless of the writing data to the register. The bit-set (BSET) that does not change the value is recommended.

■Watchdog Time-out Period

The watchdog time-out period is decided by the bp2, 1 (WDTS1-0) of the watchdog timer control register (WDCTR) and the system clock (fs). If the watchdog timer is not cleared by this set value, that is regarded as an error and the watchdog interrupt (WDIRQ) of the non maskable interrupt (NMI) is generated.

Table 9-3-1 Watchdog Time-out Period

WDTS1	WDTS0	Watchdog time-out period
0	0	2^{16} X systemclock
0	1	2^{18} X systemclock
1	X	2^{20} X systemclock

System clock is decided by the CPU mode control register (CPUM).

[☞ Chapter 2 2-5. Clock Switching]

The watchdog time-out period is generally decided from the execution time for main routine of program. That should be set the longer cycle than the value of the execution time for main routine divided by natural number (1, 2, , ,). And set the command of the watchdog timer clear to the main routine as that value makes the same cycle.

■Watchdog Timer and CPU Mode

The relation between this watchdog timer and CPU mode features are as follows ;

(1) In NORMAL, IDLE, SLOW mode, the system clock is counted.
(2) The counting is continued regardless of switching at NORMAL, IDLE, SLOW mode.
(3) In HALT mode, the watchdog timer is stopped.
(4) In STOP mode, the watchdog timer is cleared automatically.
(5) In STOP mode, the watchdog interrupt cannot be generated.
(6) After releasing reset or recovering from STOP, the counting is executed for the period of the oscillation stabilization wait time.

Normally on the system that uses STOP mode, instruction whether or not to enter to STOP mode causes branching on program in execution. This changes count value of the watchdog timer, and be careful about a generation of watchdog interrupt in such cases.

9-3-2 Setup Example

The watchdog timer detects errors. On the following example, the time-out period is set to $2^{18} \times$ system clock.
An example setup procedure, with a description of each step is shown below.

■Initial Setup Program (Watchdog Timer Initial Setup Example)

Setup Procedure	Description
(1) Set the time-out period. WDCTR (x'03F02') bp2-1 : WDTS1-0 = 01	(1) Set the WDTS1-0 flag of the watchdog timer control register (WDCTR) to "01" to select the time-out period to $2^{18} \times$ system clock.
(2) Start the watchdog timer operation. WDCTR (x'03F02') bp0 : WDEN = 1	(2) Set the WDEN flag of the WDCTR register to start the watchdog timer operation.

The command that sets WDEN flag to "1" should be issued at the end of the initial setting.

■Main Routine Program (Watchdog Timer Constant Clear Setup Example)

Setup Procedure	Description
(1) Set the watchdog timer for the constant clear. Writing to WDCTR (x'03F02') (cf.) BSET (WDCTR) WDEN (bp0 : WDEN = 1)	(1) Clear the watchdog timer by the cycle of $2^{18} \times$ system clock. The watchdog timer clear should be inserted in the main routine, with the same cycle, and to be the set cycle. The recommended instruction is the bit-set (BSET), does not change value, for clear.

■Interrupt Service Routine Setup

Setup Procedure	Description
(1) Set the watchdog interrupt service routine. NMICR (x'03FE1') TBNZ (NMICR) WDIR, WDPRO	(1) If the watchdog timer overflows, the non maskable interrupt is generated. Confirm that the WDIR flag of the non maskable interrupt control register (NMICR) is "1" on the interrupt service routine to manage the suitable execution.

The operation, just before the WDOG interrupt may be executed wrongly. Therefore, if the WDOG interrupt is generated, initialize the system.

Chapter 10 Buzzer

10

10-1 Overview

This LSI has a buzzer. It can output the square wave, that multiply by $1/2^9$ to $1/2^{14}$ of the high frequency oscillation clock, or by $1/2^3$ to $1/2^4$ of the low frequency oscillation clock.

10-1-1 Block Diagram

■Buzzer Block Diagram

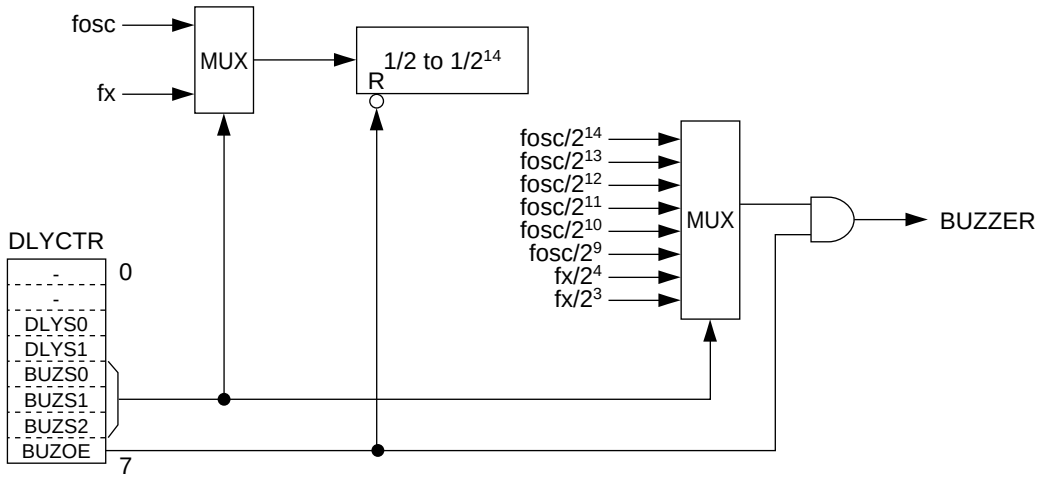


Figure 10-1-1 Block Diagram (Buzzer)

10-2 Control Register

■Oscillation Stabilization Wait Time Control Register

	7	6	5	4	3	2	1	0
DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-

(At reset : 0 0 0 0 0 1 - -)

DLYS1	DLYS0	Oscillation stabilization wait period selection
0	0	$fs/2^{14}$
	1	$fs/2^{10}$
1	0	$fs/2^{6}$ (option only in SLOW mode)
	1	$fs/2^{2}$ (option only in SLOW mode)

Note : After reset is released, the oscillation stabilization wait period is fixed at $fs/2^{10}$.

BUZS2	BUZS1	BUZS0	Buzzer output frequency selection
0	0	0	$fosc/2^{14}$
		1	$fosc/2^{13}$
	1	0	$fosc/2^{12}$
		1	$fosc/2^{11}$
1	0	0	$fosc/2^{10}$
		1	$fosc/2^{9}$
	1	0	$fx/2^{4}$
		1	$fx/2^{3}$

BUZOE	P06 output selection
0	P06 port output
1	P06 buzzer output

Figure 10-2-1 Oscillation Stabilization Wait Time Control Register (DLYCTR : x'03F03', R/W)

10-3 Operation

10-3-1 Operation

■Buzzer

Buzzer outputs the square wave, having frequency $1/2^9$ to $1/2^{14}$ of the high oscillation clock (fosc), or $1/2^3$ to $1/2^4$ of the low oscillation clock (fx). The BUZS 2, 1, 0 flag of the oscillation stabilization wait control register (DLYCTR) set the frequency of buzzer output. The BUZOE flag of the oscillation stabilization wait control register (DLYCTR) sets buzzer output ON / OFF.

■Buzzer Output Frequency

The frequency of buzzer output is decided by the frequency of the high oscillation clock (fosc) or the low oscillation clock (fx) and the bit 6, 5, 4 (BUZS2, BUZS1, BUZS0) of the oscillation stabilization wait control register (DLYCTR).

Table 10-3-1 Buzzer Output Frequency

fosc	fx	BUZS2	BUZS1	BUZS0	Buzzer output frequency
20 MHz	-	0	0	0	1.22 kHz
20 MHz	-	0	0	1	2.44 kHz
20 MHz	-	0	1	0	4.88 kHz
8.38 MHz	-	0	1	0	2.05 kHz
8.38 MHz	-	0	1	1	4.09 kHz
2 MHz	-	1	0	0	1.95 kHz
2 MHz	-	1	0	1	3.91 kHz
-	32 kHz	1	1	0	2 kHz
-	32 kHz	1	1	1	4 kHz

10-3-2 Setup Example

Buzzer outputs the square wave of 2 kHz from P06 pin. It is used 8.38 MHz as the high oscillation clock (fosc).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the buzzer frequency. DLYCTR (x'3F03') bp6-4 : BUZS2-0 = 010	(1) Set the BUZS2-0 flag of the oscillation stabilization wait control register (DLYCTR) to "010" to select fosc/2^{12} to the buzzer frequency. When the high oscillation clock fosc is 8.38 MHz, the buzzer output frequency is 2.05 kHz.
(2) Set P06 pin. P0OUT (x'3F10') bp6 : P0OUT6 = 0 P0DIR (x'3F30') bp6 : P0DIR6 = 1	(2) Set the output data P0OUT6 of P06 pin to "0", and set the direction control P0DIR6 of P06 pin to "1" to select output mode. Port 06 pin outputs low level.
(3) Buzzer output ON. DLYCTR (x'3F03') bp7 : BUZOE = 1	(3) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "1" to output the square wave of the buzzer output frequency set by P06 pin.
(4) Buzzer output OFF. DLYCTR (x'3F03') bp7 : BUZOE = 0	(4) Set the BUZOE flag of the oscillation stabilization wait control register to (DLYCTR) "0" to clear, and P06 pin outputs low level.

Chapter 11 Serial Interface 0

11

11-1 Overview

This LSI contains a serial interface 0 that can be used for both communication types of clock synchronous and UART (duplex).

11-1-1 Functions

Table 11-1-1 shows functions of serial interface 0.

Table 11-1-1 Serial Interface 0 Functions

Communication style	clock synchronous	UART (duplex)
Interrupt	SC0TIRQ	SC0TIRQ (on transmission completion) SC0RIRQ (on reception completion)
Used pins	SBO0,SBI0,SBT0	TXD,RXD
3 channels type	√	-
2 channels type	√ (SBO0, SBT0)	√
1 channel type	-	√ (TXD)
Specification of transfer bit count / Frame selection	1 to 8 bits	7 bits + 1STOP 7 bits + 2STOPs 8 bits + 1STOP 8 bits + 2STOPs
Selection of parity bit	-	√
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	√	only "enable start condition" is available
Specify of the first transfer bit	√	√
Specify of input edge / output edge	√	-
Continuous operation	√	√
Internal clock 1/8 dividing	√	only 1/8 dividing is available
Clock source	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 3 output External clock	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 3 output
Maximum transfer rate	2.5 MHz	300 kbps (standard 300 bps to 38.4 kbps) (timer 3 output)
fosc : Machine clock (High speed oscillation) fs : System clock [☞ Chapter 2 2-5. Clock Switching]		

*Descriptions of SBO0, SBI0, SBT0, TXD, RXD on this table also applied to both Port0 (TXDA/ SBO0A/RXDA/SBI0A/SBT0A) and PortB (TXDB/SBO0B/RXDB/SBI0B/SBT0B).

11-1-2 Block Diagram

■Serial Interface 0 Block Diagram

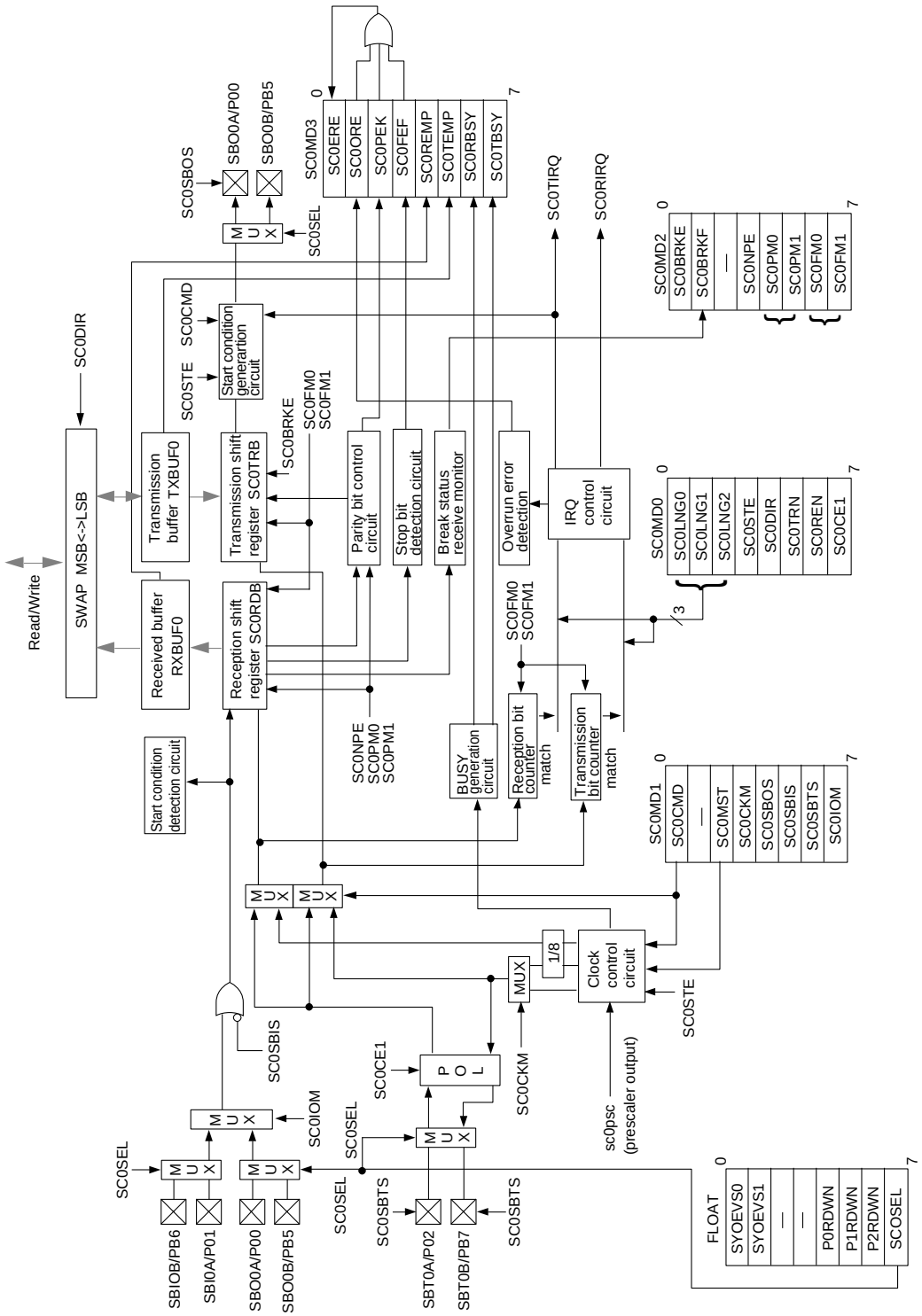


Figure 11-1-1 Serial Interface 0 Block Diagram

11-2 Control Registers

11-2-1 Registers

Table 11-2-1 shows registers to control serial interface 0.

Table 11-2-1 Serial Interface 0 Control Registers

	Register	Address	R/W	Function	Page
Serial 0	SC0MD0	x'03F90'	R/W	Serial interface 0 mode register 0	XI - 6
	SC0MD1	x'03F91'	R/W	Serial interface 0 mode register 1	XI - 7
	SC0MD2	x'03F92'	R/W	Serial interface 0 mode register 2	XI - 9
	SC0MD3	x'03F93'	R	Serial interface 0 state register	XI - 10
	RXBUF0	x'03F94'	R	Serial interface 0 received data buffer	XI - 5
	TXBUF0	x'03F95'	R/W	Serial interface 0 transmission data buffer	XI - 5
	SC0ODC	x'03F96'	R/W	Serial interface 0 port control register	XI - 11
	SC0CKS	x'03F97'	R/W	Serial interface 0 transfer clock selection register	V - 9, XI - 12
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLUD	x'03F40'	R/W	Port 0 pull-up / pull-down control register	IV - 7
	PBDIR	x'03F3B'	R/W	Port B direction control register	IV - 62
	PBPLU	x'03F4B'	R/W	Port B pull-up control register	IV - 62
	FLOAT	x'03F2E'	R/W	Pull-up / pull-down resistor selection, Pin control register	IV - 8, 16, 31, 59, XI - 8
	SC0RICR	x'03FF5'	R/W	Serial interface 0 UART reception interrupt control register 1	III - 36
	SC0TICR	x'03FF6'	R/W	Serial interface 0 interrupt control register 2	III - 37

R/W : Readable / Writable
R : Readable only

11-2-2 Data Buffer Registers

Serial Interface 0 has each 8-bit data buffer register for transmission, and for reception.

■Serial Interface 0 Received Data Buffer (RXBUF0)

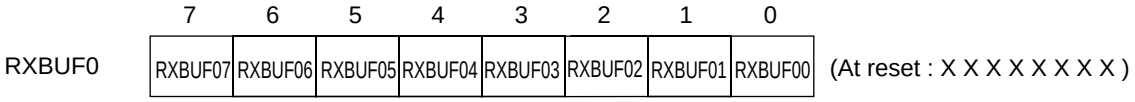


Figure 11-2-1 Serial Interface 0 Received Data Buffer (RXBUF0 : x'03F94', R)

■Serial Interface 0 Transmissin Data Buffer (TXBUF0)

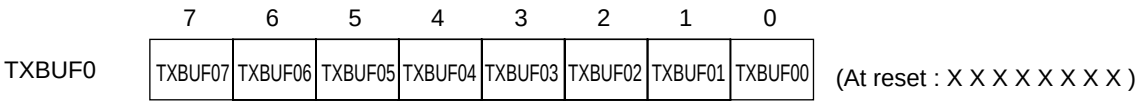


Figure 11-2-2 Serial Interface 0 Transmission Data Buffer (TXBUF0 : x'03F95', R/W)

11-2-3 Mode Registers

■Serial Interface 0 Mode Register 0 (SC0MD0)

	7	6	5	4	3	2	1	0
SC0MD0	SC0CE1	SC0REN	SC0TRN	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0

(At reset : 0 0 0 0 0 1 1 1)

SC0LNG2	SC0LNG1	SC0LNG0	Synchronous serial transfer bit count
0	0	0	1 bits
		1	2 bits
	1	0	3 bits
		1	4 bits
1	0	0	5 bits
		1	6 bits
	1	0	7 bits
		1	8 bits

SC0STE	Start condition selection
0	Disable start condition
1	Enable start condition

SC0DIR	First bit to be transfered
0	MSB first
1	LSB first

SC0TRN	Transmission data polarity selection
0	Positive polrity
1	Negative polrity

SC0REN	Received data polarity selection
0	Positive polrity
1	Negative polrity

SC1CE1	Transmission data output edge	Received data input edge
0	falling	rising
1	rising	falling

Figure 11-2-3 Serial Interface 0 Mode Register 0 (SC0MD0 : x'03F90', R/W)

■Serial Interface 0 Mode Register 1 (SC0MD1)

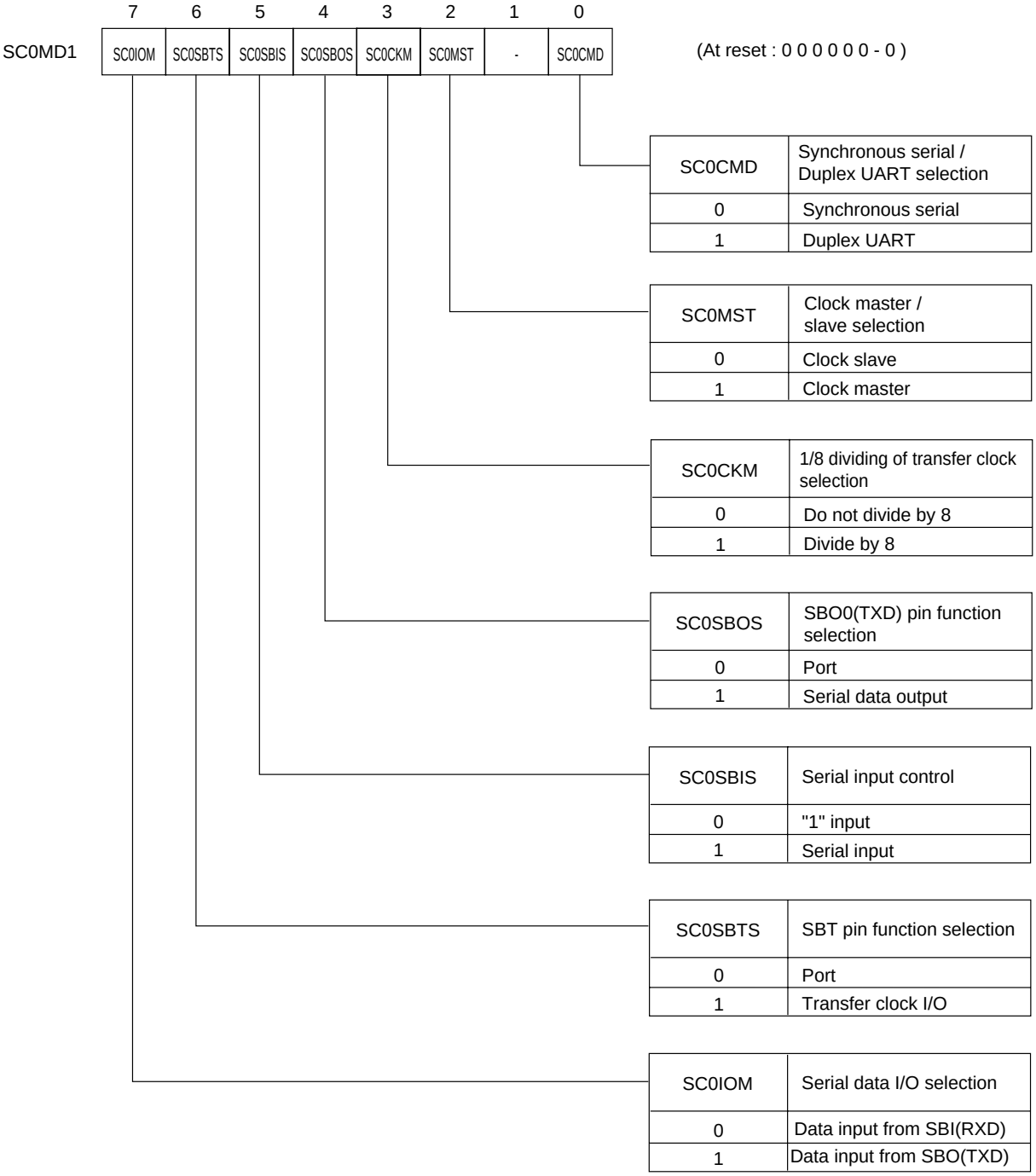

7 6 5 4 3 2 1 0
SC0MD1
SC0IOM SC0SBTS SC0SBIS SC0SBOS SC0CKM SC0MST - SC0CMD
(At reset : 0 0 0 0 0 0 - 0)
SC0CMD | Synchronous serial / Duplex UART selection
0 | Synchronous serial
1 | Duplex UART
SC0MST | Clock master / slave selection
0 | Clock slave
1 | Clock master
SC0CKM | 1/8 dividing of transfer clock selection
0 | Do not divide by 8
1 | Divide by 8
SC0SBOS | SBO0(TXD) pin function selection
0 | Port
1 | Serial data output
SC0SBIS | Serial input control
0 | "1" input
1 | Serial input
SC0SBTS | SBT pin function selection
0 | Port
1 | Transfer clock I/O
SC0IOM | Serial data I/O selection
0 | Data input from SBI(RXD)
1 | Data input from SBO(TXD)

Figure 11-2-4 Serial Interface 0 Mode Register 1 (SC0MD1 : x'03F91', R/W)

■Pull-up / pull-down resistor selection, Pin control Register (FLOAT)

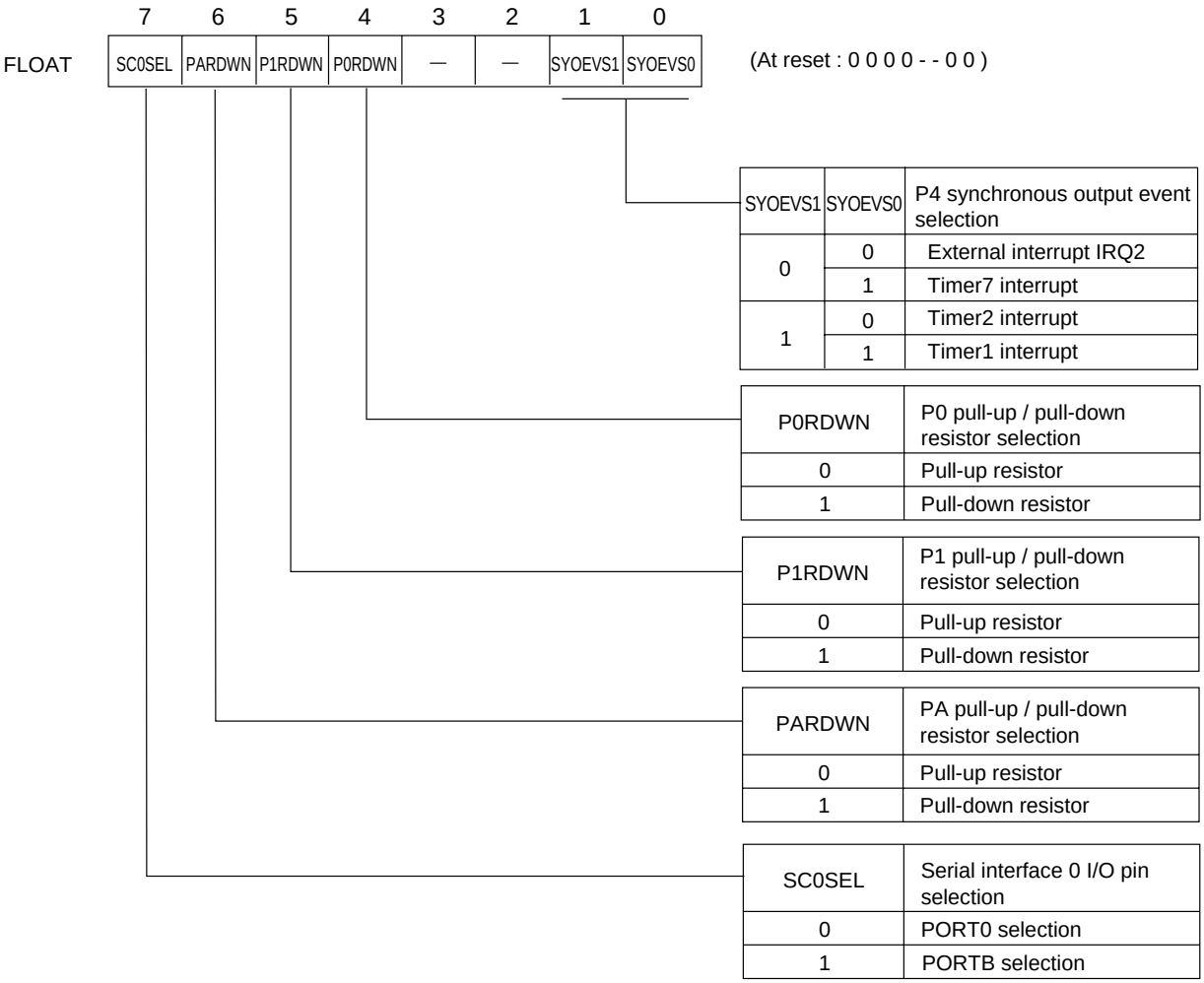
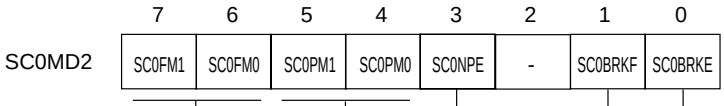

7 6 5 4 3 2 1 0
FLOAT
SC0SEL PARDWN P1RDWN P0RDWN — — SYOEVS1 SYOEVS0
(At reset : 0 0 0 0 - - 0 0)
SYOEVS1 SYOEVS0 P4 synchronous output event selection
0 0 External interrupt IRQ2
1 Timer7 interrupt
1 0 Timer2 interrupt
1 Timer1 interrupt
P0RDWN P0 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
P1RDWN P1 pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
PARDWN PA pull-up / pull-down resistor selection
0 Pull-up resistor
1 Pull-down resistor
SC0SEL Serial interface 0 I/O pin selection
0 PORT0 selection
1 PORTB selection

Figure 11-2-5 Pull-up / pull-down resistor selection, Pin control Register (FLOAT : x'03F2E', R/W)

■Serial Interface 0 Mode Register 2 (SC0MD2)

SC0BRKF flag is only for reading.



SC0BRKE	Break status transmit control
0	Data
1	Break

SC0BRKF (*)	Break status receive monitor
0	Data
1	Break

(*) Only read access is available.

SC0NPE	Parity enable
0	Enable parity bit
1	Disable parity bit

SC0PM1	SC0PM0	Added bit specification	
		Transmission	Reception
0	0	Add "0"	Check for 0
	1	Add "1"	Check for 1
1	0	Add odd parity	Check for odd parity
	1	Add even parity	Check for even parity

SC0FM1	SC0FM0	Frame mode specification
0	0	7 data bits + 1 stop bit
	1	7 data bits + 2 stop bits
1	0	8 data bits + 1 stop bit
	1	8 data bits + 2 stop bits

Figure 11-2-6 Serial Interface 0 Mode Register 2 (SC0MD2 : x'03F92', R/W)

■Serial Interface 0 Mode Register 3 (SC0MD3)

All flags are only for reading.

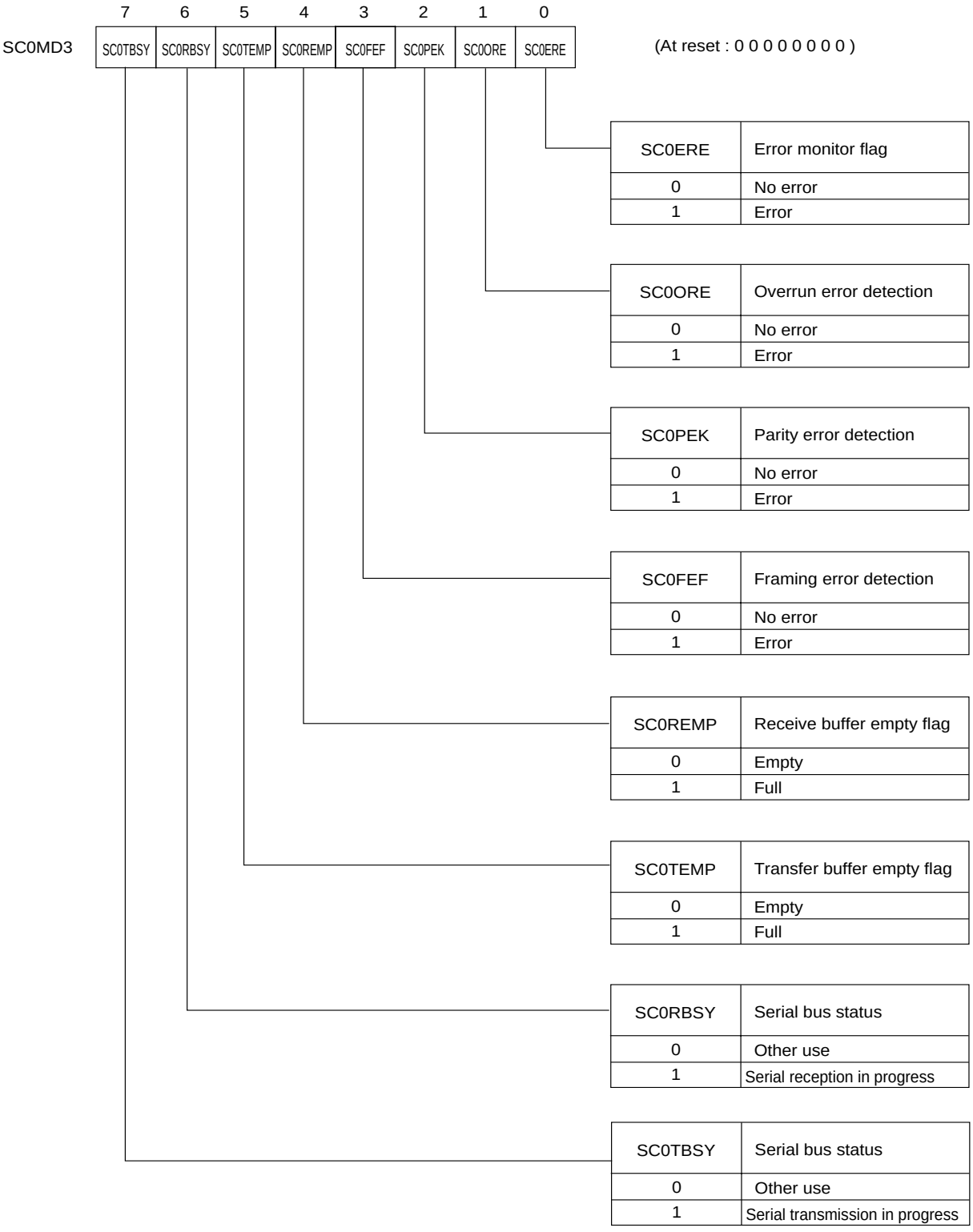


Figure 11-2-7 Serial Interface 0 Mode Register 3 (SC0MD3: x'03F93', R)

■Serial Interface 0 Port Control Register (SC0ODC)

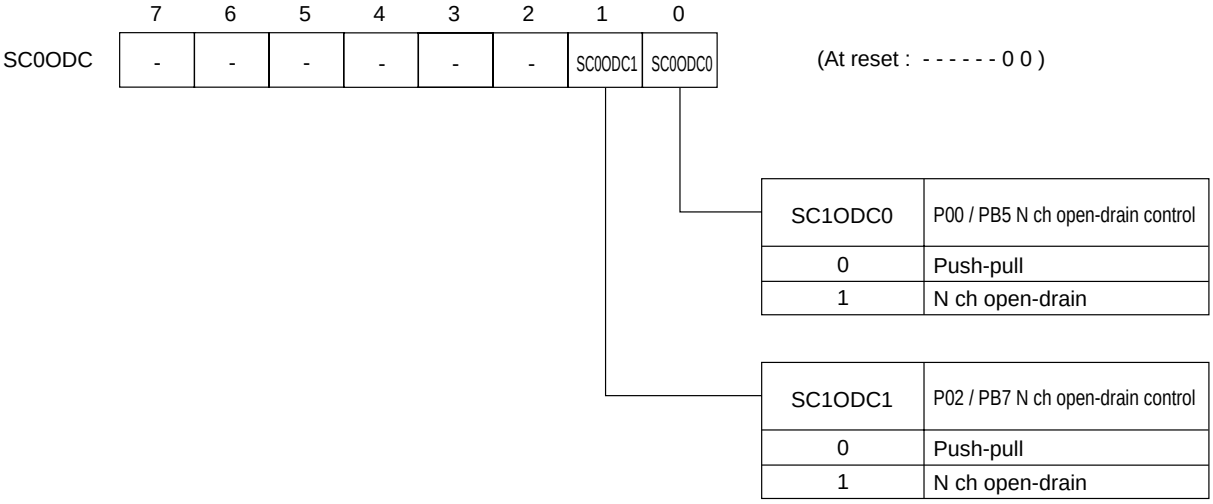


Figure 11-2-8 Serial Interface 0 Port Control Register (SC0ODC : x'03F96', R/W)

■Serial Interface 0 Transfer Clock Selection Register (SC0CKS)

	7	6	5	4	3	2	1	0
SC0CKS	—	—	—	—	SC0TMSEL	SC0PSC2	SC0PSC1	SC0PSC0

(At reset : - - - - X X X X)

SC0TMSEL	SC0PSC2	SC0PSC1	SC0PSC0	Clock selection
-	0	0	0	fosc/2
			1	fosc/4
		1	0	fosc/16
			1	fosc/64
	1	0	0	fs/2
			1	fs/4
0		1	0	Disable
			1	Timer 3 output
1			0	Disable
			1	Disable

Figure 11-2-9 Serial Interface 0 Tranfer Clock Selection Register (SC0CKS : x'03F97', R/W)

11-3 Operation

Serial Interface 0 can be used for both clock synchronous and duplex UART.

11-3-1 Clock Synchronous Serial Interface

■Activation Factor for Communication

Table 11-3-1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the transmission data buffer TXBUF0, or by receiving a start condition. Except during communication, the input signal from SBT pin is masked to prevent errors by noise or so. This mask can be released automatically by setting a data to TXBUF0(access to the TXBUF0 register), or by inputting a start condition to the data input pin. Therefore, at slave communication, set data to TXBUF0, or input an external clock after a start condition is input.

Table 11-3-1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
at master	Set transmission data	Set dummy data
		Input start condition
at slave	Input clock after transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■Transfer bit Setup

The transfer bit count is selected from 1 bit to 8 bits. Set them by the SC0LNG 2 to 0 flag of the SC0MD0 register (at reset : 111). The SC0LNG 2 to 0 flag holds the former set value until it is set again.

Except during communication, SBT pin is masked to prevent errors by noise. At slave communication, set data to TXBUF0 or input a clock to SBT pin after a start condition is input.

■Start Condition Setup

The SC0STE flag of the SC0MD0 register sets if a start condition is enabled or not. If a start condition is selected, and input at communication, a bit counter is cleared to restart the communication. The start condition is regarded that when a clock line (SBT pin) is "H", data line (SBI pin (with 3 lines) or SBO pin (with 2 lines)) is changed from "H" to "L". Both the SC0SBOS flag and the SC0SBIS flag of the SC0MD1 register should be set to "0", before the start condition setup is changed.

■First Transfer bit Setup

The SC0DIR flag of the SC0MD0 register can set the transfer first bit. MSB first or LSB first can be selected.

■Transmission Data Buffer

The transmission data buffer, TXBUF0 is a buffer of reserve that stores data to load the internal shift register. Data to be transfered should be set to the transmission data buffer, TXBUF0, to be loaded to the internal shifr register automatically. The first data loading to the internal shift register is done at the same timing of the data setting to TXBUF0.

■Received Data Buffer

The received data buffer RXBUF0 is a buffer of reserve that pushed the received data in the internal shift register. After the communication complete interrupt SC0TIRQ is generated, all data stored in the internal shift register are stored to the received data buffer RXBUF0 automatically. RXBUF0 can store data up to 1 byte. RXBUF0 is rewritten in everytime when communication is completed, so read out data of RXBUF0 till the next receive is completed. The received data buffer empty flag SC0REMP is set to "1" at the same time SC0TIRQ is generated. SC0REMP is cleared to "0" after RXBUF0 is read out.

If a start condition is input to restart during communication, the transmission data is not valid. Set the transmission data to TXBUF0 again to operate the transmission again.

Start condition should be switched after both the SC0SBOS and the SC0SBIS flags of the SC0MD1 register are set to "0". If they are not set to "0", the switching is not valid.

RXBUF0 is rewritten everytime when communication is completed. At continuous communication, data of RXBUF0 should be read out until the next reception is completed.

■Tranfer bit Count and First Transfer bit

When the transfer bit is 1 bit to 7 bits, the data storing method to the transmission data buffer TXBUF0 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF0 for storing. When there are 6 bits to be transfered, as shown on figure 11-3-1, if data "A" to "F" are stored to bp2 to bp7 of TXBUF0, the transmission is operated from "F" to "A". At LSB first, use the lower bits of TXBUF0 for storing. When there are 6 bits to be transfered, as shown on figure 11-3-2, if data "A" to "F" are stored to bp0 to bp5 of TXBUF0, the transmission is operated from "A" to "F".

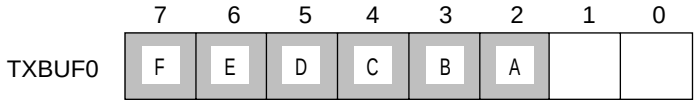


Figure 11-3-1 Transfer bit Count and First Transfer bit (starting with MSB)

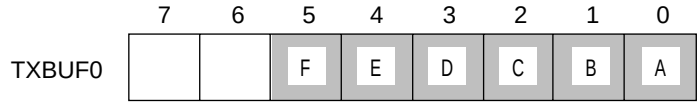


Figure 11-3-2 Transfer bit Count and First Transfer bit (starting with LSB)

■Receive bit Count and First Transfer bit

When the transfer bit count is 1 bit to 7 bits, the data storing method to the received data buffer RXBUF0 is different depending on the first transfer bit. At MSB first, data are stored to the lower bits of RXBUF0. When there are 6 bits to be transfered, as shown on figure 11-3-3, if data "A" to "F" are stored to bp0 to bp5 of RXBUF0, the transmission is operated from "F" to "A". At LSB first, data are stored to the upper bits of RXBUF0. When there are 6 bits to be transfered, as shown on figure 11-3-4, if data "A" to "F" are stored to bp2 to bp7 of RXBUF0, the transmission is operated from "A" to "F".

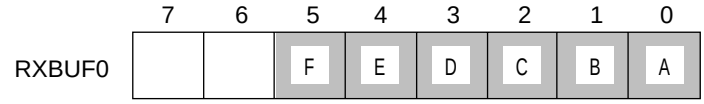


Figure 11-3-3 Receive bit Count and Transfer First bit (starting with MSB bit)

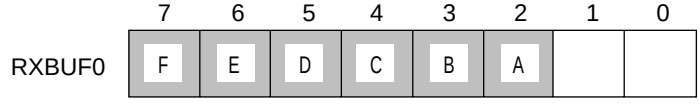


Figure 11-3-4 Receive bit Count and Transfer First bit (starting with LSB bit)

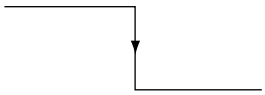
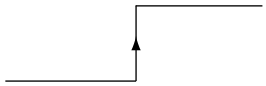
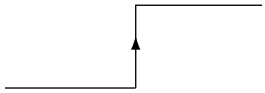
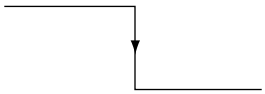
■Continuous Communication

This serial has a function for continuous communication. If data is set to the transmission data buffer TXBUF0 during communication, the transmission buffer empty flag SC0TEMP is automatically set to communicate continuously. Data setup to TXBUF0 should be done till the communication complete interrupt SC0TIRQ is generated after the former data is set. At master communication, there is a suspension of communication for 3 transfer clocks till the next transmission clock is output after the SC0TIRQ generation.

■Input Edge / Output Edge Setup

The SC0CE 1 flag of the SC0MD0 register set an output edge of the transmission data, an input edge of the received data. As the SC0CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC0CE1="0", the received data is received at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table 11-3-2 Transmission Data Output Edge and Received Data Input Edge

SC0CE1	Transmission data output edge	Received data input edge
0		
1		

■Change of Polarity of Transmission / Reception Data

It is possible to change the polarity of the transmission / reception data. When the SC0REN flag of SC0MD0 register is set to "1", the polarity inverted input signals from the data input pins are loaded to reception shift register. When the SC0TRN flag of SC0MD0 register is set to "1", the inverted signals of the data set in the transmission buffer TXBUF0 is output to the data output pins.

■Clock Setup

The SC0CKS register selects a clock source from the special prescaler and timer output. The special prescaler starts its operation after the PSCMD (x'03F6F') register selects "prescaler operation". The SC0MST flag of the SC0MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock that has the same clock cycle or below to the external clock, by the SC0CKS register. That is happened, because the interrupt flag SC0TIRQ is generated by the internal clock. Here is the internal clock source that can be set by the SC0CKS register. Also, the SC0CKM flag of the SC0MD1 register can divide the internal clock by 8.

Table 11-3-3 Synchronous Serial Interface Internal Clock Source

	Serial 0
Internal clock	fosc/2
	fosc/4
	fosc/16
	fosc/64
	fs/2
	fs/4
	Timer 3 output

■Data Input Pin Setup

3 channels type (clock pin (SBT pin), data output pin (SBO pin), data input pin (SBI pin)) or 2 channels type (clock pin (SBT pin), data I/O pin (SBO pin)) can be selected as a communication mode. SBI pin can be used for only serial data input. SBO pin can select serial data input or output. The SC0IOM flag of the SC0MD1 register can select if the serial data is input to SBI pin or SBO pin. When "data input from SBO pin" is selected to set the 2 lines type, the P0DIR0 flag of the P0DIR register controls direction of SBO pin to switch transmission / reception. At this time, SBI pin can be used as a general port, too.

In initial condition (at reset), Port0 pins (SBO0A/P00, SBI0A/P01, SBT0A/P02) are assigned to be serial interface data I/O pins, which can be substituted with PortB pins (SBO0B/PB5, SBI0B/PB6, SBT0B/PB7). Serial interface I/O pins are selected with SC0SEL flag of the FLOAT register. To select Port0 set 0 to the SC0SEL flag, and to select PortB set 1 to the SC0SEL flag.

The transfer speed should be up to 2.5 MHz. If the transfer clock is over 2.5 MHz, the transmission data may not be sent correctly.

At reception, if SC0IOM of the SC0MD1 register is set to "1" and "serial data input from SBO" is selected, SBI pin can be used as a general port.

■Reception Buffer Empty Flag

When SC0TIRQ is generated, data is automatically stored to RXBUF0 from the internal shift register. If data is stored to the shift register RXBUF0, the reception buffer empty flag SC0REMP of the SC0MD3 register is set to "1". This indicates that the received data is going to read out. SC0REMP is cleared to "0" by reading out the data of RXBUF0.

■Transmission Buffer Empty Flag

If any data is set to TXBUF0 again, during communication (after setting data to TXBUF0 and before the communication complete interrupt SC0TIRQ is generated), the transmission buffer empty flag SC0TEMP of the SC0MD3 register is set to "1". This indicates that the next transmission data is going to be loaded. Data is loaded to the inside shift register from TXBUF0 by generation of SC0TIRQ, and the next transfer is started as SC0TEMP is cleared to "0".

■Overrun Error and Error Monitor Flag

If, after reception complete, the next data has been already received before reading out of the data of the received data buffer RXBUF0, overrun error is generated and the SC0ORE flag of the SC0MD3 register is set to "1". And at the same time, the error monitor flag SC0RE is set to indicate that error is occurred on reception. The SC0ORE flag holds the status unless the data of RXBUF0 is read out. SC0ERE is cleared as SC0ORE flag is cleared. These error flags have no effect on communication operation.

■Reception BUSY Flag

When any data is set to TXBUF0 or when the SC0SBIS flag of the SC0MD1 register is "1" as start condition is input, the SC0RBSY flag of the SC0MD3 register is set to "1". And, on the generation of the communication complete interrupt SC0TIRQ, the flag is cleared to "0". And, during continuous communication, the SC0RBSY flag is always set. If the transmission buffer empty flag SC0TEMP is cleared to "0" as the communication complete interrupt SC0TIRQ is generated, SC0RBSY is cleared to "0". If the SC0SBIS flag is set to "0" during communication, the SC0RBSY flag is cleared to "0".

■Transmission BUSY Flag

When any data is set to TXBUF0 or when the SC0SBOS flag of the SC0MD1 register is "1" as start condition is input, the SC0TBSY flag of the SC0MD3 register is set to "1". And, on the generation of the communication complete interrupt SC0TIRQ, the flag is cleared to "0". And, during continuous communication, the SC0TBSY falg is always set. If the transmission buffer empty flag SC0TEMP is cleared to "0" as the communication complete interrupt SC0TIRQ is generated, SC0TBSY is cleared to "0". If the SC0SBOS flag is set to "0" during communication, the SC0TBSY flag is cleared to "0".

■Emergency Reset

This serial interface contains emergency reset for abnormal operation. For emergency reset, the SC0SBOS flag and the SC0SBIOS flag of the SC0MD1 register should be set to "0" (SBO pin : port, input data : "1" input). At emergency reset, the status registers (the SC0BRKF flag of the SC0MD2 register, all flags of the SC0MD3 register) are initialized as they are set at reset, but the control register holds the set value.

■Last bit of Transfer Data

Table 11-3-4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. After data output holding period of the last bit, "H" is output.

Table 11-3-4 Last bit Data Length of Transfer Data

	The last bit data holding period at transmission	The last data input period at reception
At master	1 bit data length	1 bit data length (Minimum)
At slave	1 bit data length × 1 to 1.5	

■Other Control Flag Setup

Table 11-3-5 shows flags that are not used at clock synchronous communication. So, they are not needed to set or monitor.

Table 11-3-5 Other Control Flag

Register	Flag	Detail
SC0MD2	SC0BRKF	Brake status reception monitor
	SC0NPE	Parity is enabled
	SC0PM1 to 0	Added bit specification
	SC0FM1 to 0	Frame mode specification
SC0MD3	SC0PEK	Parity error detection
	SC0FEF	Frame error detection

■Trasnmission Timing

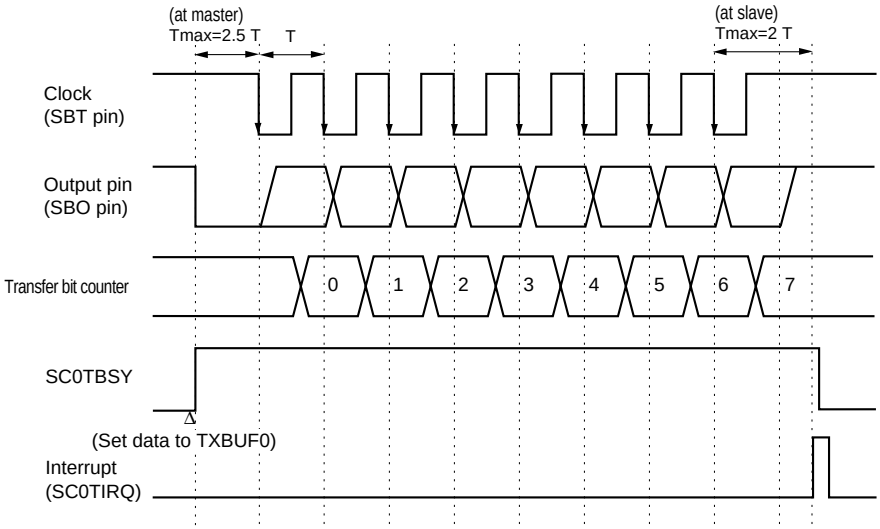


Figure 11-3-5 Transmission Timing (at falling edge, start condition is enabled)

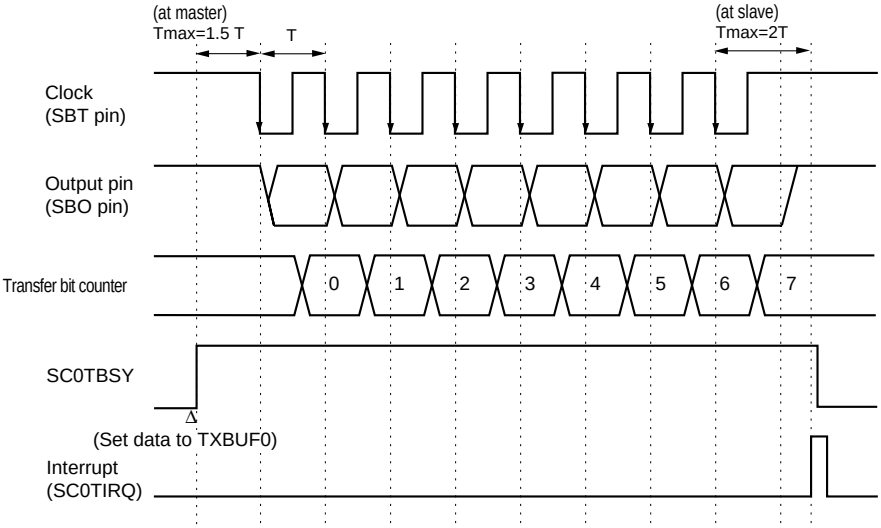


Figure 11-3-6 Transmission Timing (at falling edge, start condition is disabled)

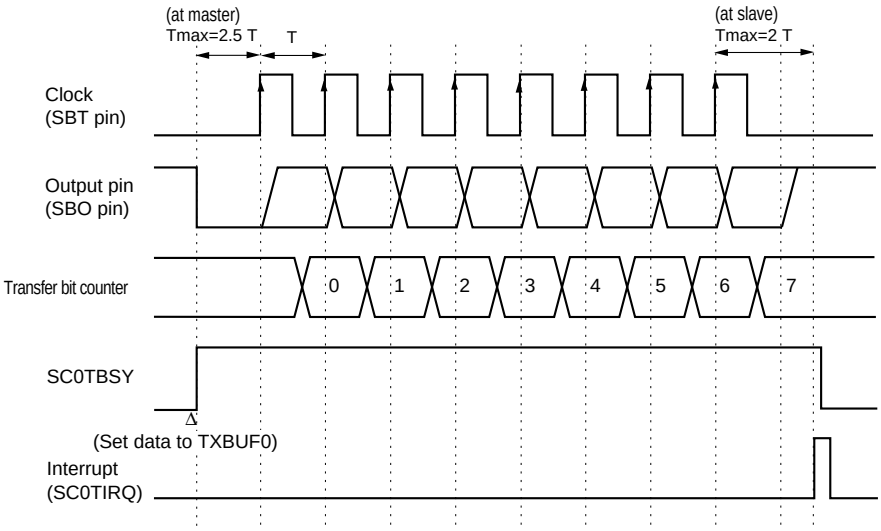


Figure 11-3-7 Transmission Timing (at rising edge, start condition is enabled)

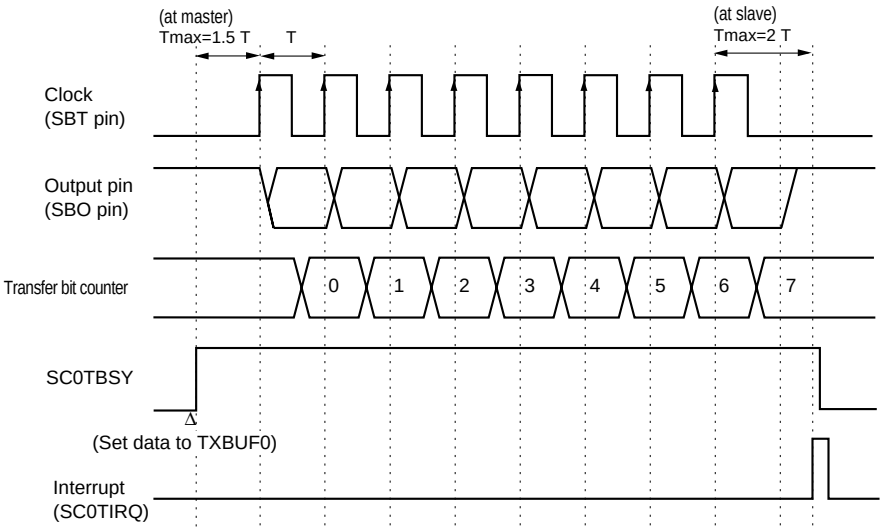


Figure 11-3-8 Transmission Timing (at rising edge, start condition is disabled)

■Reception Timing

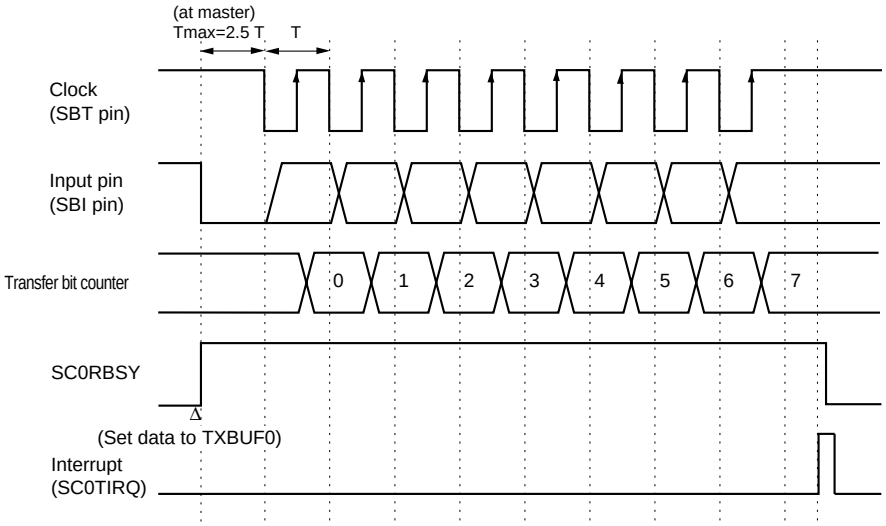


Figure 11-3-9 Reception Timing (at rising edge, start condition is enabled)

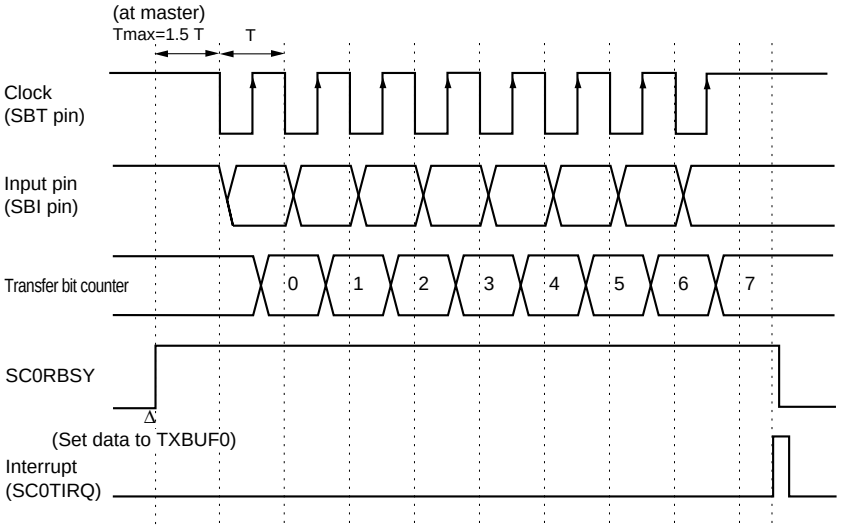


Figure 11-3-10 Reception Timing (at rising edge, start condition is disabled)

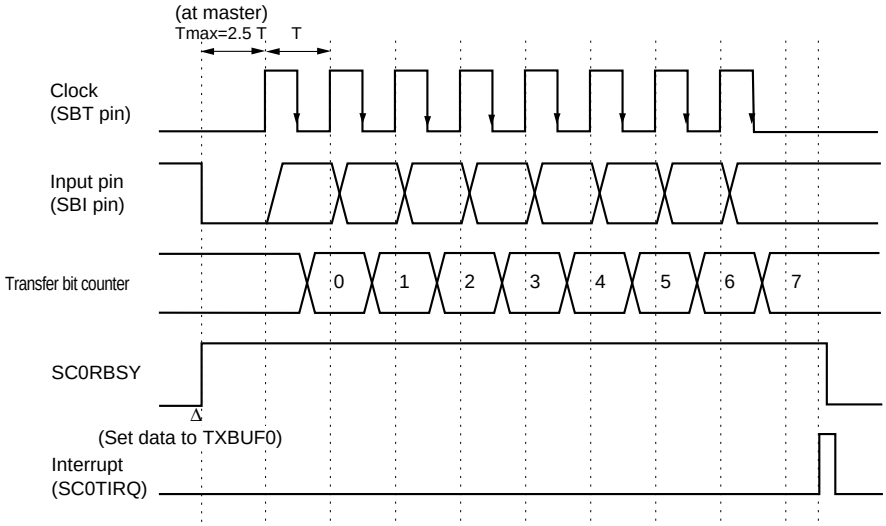


Figure 11-3-11 Reception Timing (at falling edge, start condition is enabled)

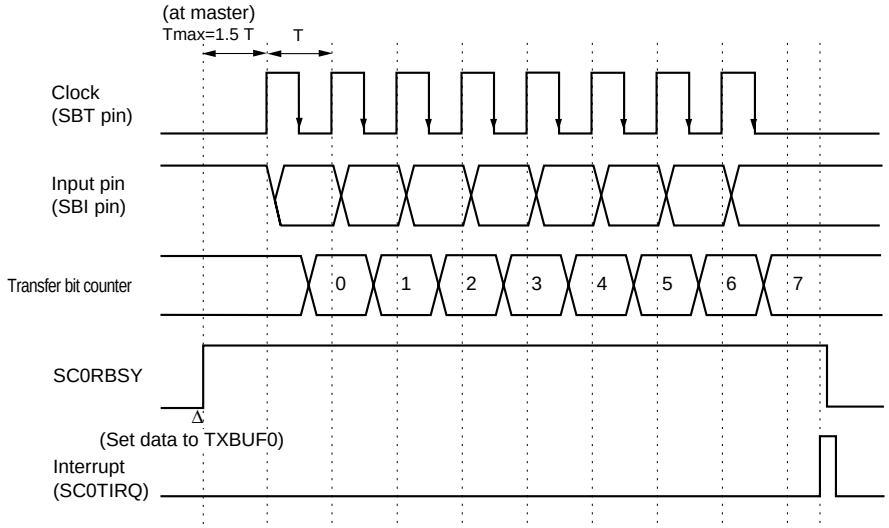


Figure 11-3-12 Reception Timing (at falling edge, start condition is disabled)

■Transmission / Reception Timing

When transmission and reception are operated at the same time, set the SC0CE1 flag of the SC0MD0 register to "0" or "1". Data is received at the opposit output edge of the transmission data, so that the input edge of the received data should be the opposide output edge of the transmission data from the other side.

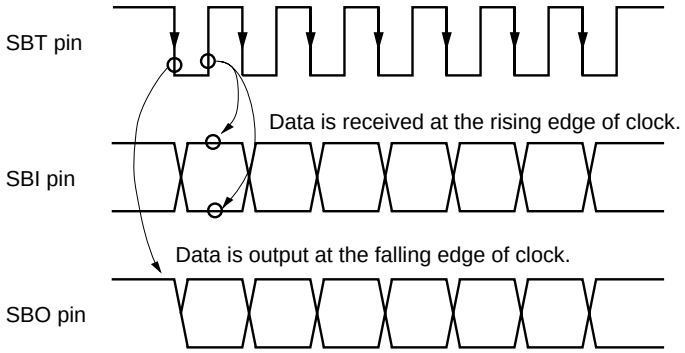


Figure 11-3-13 Transmission / Reception Timing
(Reception : at rising edge, Transmission : at falling edge)

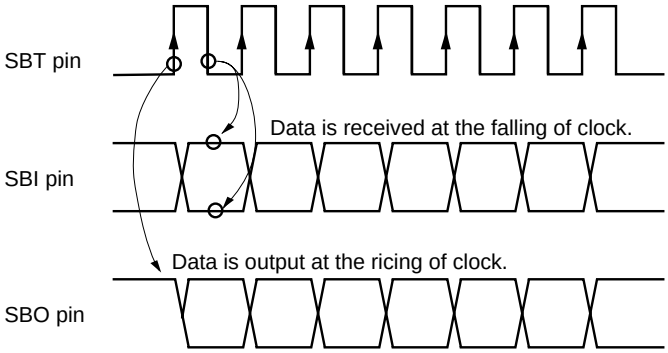


Figure 11-3-14 Transmission / Reception Timing
(Reception : at falling edge, Transmission : at rising edge)

■Pins Setup (with 3 channels, at transmission)

Table 11-3-6 shows the setup for synchronous serial interface pin with 3 channels (SBO0A pin, SBI0A pin, SBT0A pin) at transmission.

Table 11-3-6 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0A pin	SBI0A pin	SBT0A pin	
			Internal clock	External clock
Port pin	P00	P01	P02	
SBI / SBO pin	SBI / SBO independent		-	
	SC0MD1(SC1IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up / Pull-down	Added / Not added	-	Added / Not added	Added / Not added
	P0PLUD(P0PLUD0)		P0PLUD(P0PLUD2)	

■Pins Setup (with 3 channels, at reception)

Table 11-3-7 shows the setup for synchronous serial interface pin with 3 channels (SBO0A pin, SBI0A pin, SBT0A pin).

Table 11-3-7 Setup for Synchronous Serial Interface Pin (with 3 channels, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0A pin	SBI0A pin	SBT0A pin	
			Internal clock	External clock
Port pin	P00	P01	P02	
SBI / SBO pin	SBI / SBO independent		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC(SC0ODC1)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR(P0DIR1)	P0DIR(P0DIR2)	
Pull-up / Pull-down	-	-	Added / Not added	Added / Not added
			P0PLUD(P0PLUD2)	

■Pins Setup (with 3 channels, at transmission / reception)

Table 11-3-8 shows the setup for synchronous serial interface pin with 3 channels (SBO0A pin, SBI0A pin, SBT0A pin) at transmission / reception.

Table 11-3-8 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission / reception)

<table>
<tr><td rowspan="3">Setup item</td><td>Data output pin</td><td>Data input pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO0A pin</td><td rowspan="2">SBI0A pin</td><td colspan="2">SBT0A pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td>Port pin</td><td>P00</td><td>P01</td><td colspan="2">P02</td></tr>
<tr><td rowspan="2">SBI / SBO pin</td><td colspan="2">SBI / SBO independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC0MD1(SC0IOM)</td></tr>
<tr><td rowspan="2">Function</td><td>Serial data output</td><td>Serial data input</td><td>Serial clock I/O</td><td>Serial clock I/O</td></tr>
<tr><td>SC0MD1(SC0SBOS)</td><td>SC0MD1(SC0SBIS)</td><td colspan="2">SC0MD1(SC0SBTS)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull /
Nch open-drain</td><td rowspan="2">-</td><td>Push-pull /
Nch open-drain</td><td>Push-pull /
Nch open-drain</td></tr>
<tr><td>SC0ODC(SC0ODC0)</td><td colspan="2">SC0ODC(SC0ODC1)</td></tr>
<tr><td rowspan="2">I/O</td><td>Output mode</td><td>Input mode</td><td>Output mode</td><td>Input mode</td></tr>
<tr><td>P0DIR(P0DIR0)</td><td>P0DIR(P0DIR1)</td><td colspan="2">P0DIR(P0DIR2)</td></tr>
<tr><td rowspan="2">Pull-up</td><td>Added / Not added</td><td rowspan="2">-</td><td>Added / Not added</td><td>Added / Not added</td></tr>
<tr><td>P0PLUD(P0PLUD0)</td><td colspan="2">P0PLUD(P0PLUD2)</td></tr>
</table>

■Pins Setup (with 2 channels, at transmission)

Table 11-3-9 shows the setup for synchronous serial interface pin with 2 channels (SBO0A pin, SBT0A pin) at transmission. SBI0A pin can be used as a port.

Table 11-3-9 Setup for Synchronous Serial Interface Pin (with 2 channels, at transmission)

Setup item	Data output pin		Clock I/O pin	
	SBO0A pin	SBI0A pin	SBT0A pin	
			Internal clock	External clock
Port pin	P00		P02	
SBI / SBO pin	SBI/SBO connected		-	
	SC0MD1(SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	P0PLUD(P0PLUD0)		P0PLUD(P0PLUD2)	

■Pins Setup (with 2 channels, at reception)

Table 11-3-10 shows the setup for synchronous serial interface pin with 2 channels (SBO0A pin, SBT0A pin) at reception. SBI0A pin can be used as a port.

Table 11-3-10 Setup for Synchronous Serial Interface Pin (with 2 channels, at reception)

Setup item	Data input pin		Clock I/O pin	
	SBO0A pin	SB0AI pin	SBT0A pin	
			Internal clock	External clock
Port pin	P00		P02	
SBI / SBO pin	SBI / SBO connected		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC(SC0ODC1)	
I/O	Input mode	-	Output mode	Input mode
	P0DIR(P0DIR0)		P0DIR(P0DIR2)	
Pull-up	-	-	Added / Not added	Added / Not added
			P0PLUD(P0PLUD2)	

■Pins Setup (with 3 channels, at transmission)

Table 11-3-11 shows the setup for synchronous serial interface pin with 3 channels (SBO0B pin, SBI0B pin, and SBT0B pin) at transmission.

Table 11-3-11 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0B pin	SBI0B pin	SBT0B pin	
			Internal clock	External clock
Port pin	PB5	PB6	PB7	
SBI / SBO pin	SBI/SBO independant		-	
	SC0MD1(SC1IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	-	Output mode	Input mode
	PBDIR(PBDIR5)		PBDIR(PBDIR7)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	PBPLU(PBPLU5)		PBPLU(PBPLU7)	

■Pins Setup (with 3 channels, at reception)

Table 11-3-12 shows the setup for synchronous serial interface pin with 3 channels (SBO0B pin, SBI0B pin, and SBT0B pin) at reception.

Table 11-3-12 Setup for Synchronous Serial Interface Pin (with 3 channels, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0B pin	SBI0B pin	SBT0B pin	
			Internal clock	External clock
Port pin	PB5	PB6	PB7	
SBI / SBOs pin	SBI/SBO independent		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data output	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC(SC0ODC1)	
I/O	-	Input mode	Output mode	Input mode
		PBDIR(PBDIR6)	PBDIR(PBDIR7)	
Pull-up	-	-	Added / Not added	Added / Not added
			PBPLU(PBPLU7)	

■Pins Setup (with 3 channels, at transmission / reception)

Table 11-3-13 shows the setup for synchronous serial interface pin with 3 channels (SBO0B pin, SBI0B pin, and SBT0B pin) at transmission / reception.

Table 11-3-13 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0B pin	SBI0B pin	SBT0B pin	
			Internal clock	External clock
Port pin	PB5	PB6	PB7	
SBI / SBO pin	SBI/SBO independent		-	
	SC0MD1(SC0IOM)			
Function	Serial data output	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	Input mode	Output mode	Input mode
	PBDIR(PBDIR5)	PBDIR(PBDIR6)	PBDIR(PBDIR7)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	PBPLU(PBPLU5)		PBPLU(PBPLU7)	

■Pins Setup (with 2 channels, at transmission)

Table 11-3-14 shows the setup for synchronous serial interface pin with 2 channels (SBO0B pin and SBT0B pin) at transmission. SBI0B pin can be used as a port.

Table 11-3-14 Setup for Synchronous Serial Interface Pin (with 2 channels, at transmission)

Setup item	Data output pin		Clock I/O pin	
	SBO0B pin	SBI0B pin	SBT0B pin	
			Internal clock	External clock
Port pin	PB5		PB7	
SBI / SBO pin	SBI/SBO connection		-	
	SC0MD1(SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0)		SC0ODC(SC0ODC1)	
I/O	Output mode	-	Output mode	Input mode
	PBDIR(PBDIR5)		PBDIR(PBDIR7)	
Pull-up	Added / Not added	-	Added / Not added	Added / Not added
	PBPLU(PBPLU5)		PBPLU(PBPLU7)	

■Pins Setup (with 2 channels, at reception)

Table 11-3-15 shows the setup for synchronous serial interface pin with 2 channels (SBO0B pin, and SBT0B pin) at reception. SBI0B pin can be used as a port.

Table 11-3-15 Setup for Synchronous Serial Interface Pin (with 2 channels, at reception)

Setup item	Data output pin		Clock I/O pin	
	SBO0B pin	SBI0B pin	SBT0B pin	
			Internal clock	External clock
Port pin	PB5		PB7	
SBI / SBO pin	SBI/SBO connection		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC(SC0ODC1)	
I/O	Input mode	-	Output mode	Input mode
	PBDIR(PBDIR5)		PBDIR(PBDIR7)	
Pull-up	-	-	Added / Not added	Added / Not added
			PBPLU(PBPLU7)	

11-3-2 Setup Example

■Transmission / Reception Setup Example

The setup example for clock synchronous serial communication with serial 0 is shown. Table 11-3-11 shows the conditions at transmission / reception.

Table 11-3-16 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	set to		Setup item	set to
SBI / SBO pin	Independent (with 3 channels)		Clock source	fs/2
Transfer bit count	8 bits		Clock source 1/8 dividing	divided by 8
Start condition	none		SBT / SBO pin style	Nch open-drain
First transfer bit	MSB		SBT pin pull-up resistor	Added
Input edge	falling edge		SBO pin pull-up resistor	Added
Output edge	rising edge		Serial 0 communication complete interrupt	Enable
Clock	Internal clock			

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select "prescaler operation".
(2) Select the clock source. SC0CKS (x'3F97') bp2-0 : SC0PSC2-0= 100 bp3 : SC0TMSEL= 0	(2) Select the clcok source by the SC0CKS register. Set bp3-0 to "0100" to select "fs/2".
(3) Control the pin type. SC0ODC (x'3F96') bp1-0 : SC0ODC1-0= 11 P0PLUD (x'3F40') bp2, 0 : P0PLUD2, 0= 1, 1	(3) Set the SC0ODC1-0 flag of the SC0ODC register to "11" to select "N-ch open drain" to the SBO/SBT pin. Set the P0PLUD2, 0 flag of the P0PLUD register to "1, 1" to add pull-up/ pull-down resistor.
(4) Control the pin direction. P0DIR (x'3F30') bp2-0 : P0DIR2-0 = 101	(4) Set the P0DIR2-0 flag of the port 0 pindirection control register (P0DIR) to "101" to set P00, P02 "output mode", and to set P01 "input mode".
(5) Set the SC0MD0 register. Select the transfer bit count. SC0MD0 (x'3F90') bp2-0 : SC0LNG2-0= 111	(5) Set the SC0LNG2-0 flag of the serial 0 mode register (SC0MD0) to "111" to set the transfer bit count "8 bits".

Setup Procedure	Description
(6) Select the start condition. SC0MD0 (x'3F90') bp3 : SC0STE = 0	(6) Set the SC0STE flag of the SC0MD0 register to "0" to disable start condition.
(7) Select the first bit to be transfered. SC0MD0 (x'3F90') bp4 : SC0DIR = 0	(7) Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit.
(8) Select the transfer edge. SC0MD0 (x'3F90') bp7 : SC0CE1 = 1	(8) Set the SC0CE1 flag of the SC0MD0 register to "1" to set the transmission data output edge "rising" and the received data input edge "falling".
(9) Set the SC0MD2 register Control the output data. SC0MD2 (x'3F92') bp0 : SC0BRKE = 0	(9) Set the SC0BRKE flag of the SC0MD2 register to "0" to select "serial data transmission".
(10) Set other mode registers. SC0MD2 (x'3F92') bp7-3	(10) No need at synchronous serial communication.
(11) Set the SC0MD1 register. Select the communication type. SC0MD1 (x'3F91') bp0 : SC0CMD = 0	(11) Set the SC0CMD flag of the SC0MD1 register to "0" to select "synchronous serial".
(12) Select the transfer clock. SC0MD1 (x'3F91') bp2 : SC0MST = 1 bp3 : SC0CKM = 1	(12) Set the SC0MST flag of the SC0MD1 register to "1" to select clock master (inside clock). Set the SC0CKM flag to "1" to select "divide by 8" for source clock.
(13) Control the pin function. SC0MD1 (x'3F91') bp4 : SC0SBOS = 1 bp5 : SC0SBIS = 1 bp6 : SC0SBTS = 1 bp7 : SC0IOM = 0	(13) Set the SC0SBOS, SC0SBIS, SC0SBTS flag of the SC0MD1 register to "1" to set SBO pin "serial data output", SBI pin "serial data input", and SBT pin "serial clock I/O". Set the SC0IOM flag "0" to set serial data input from SBI pin.
(14) Set the interrupt level. SC0TICR (x'3FF6') bp7-6 : SC0TLV1-0= 10	(14) Set the interrupt level by the SC0TLV1-0 flag of the serial 0 transmission interrupt control register (SC0TICR). (Set level 2.)

Setup Procedure	Description
(15) Enable the interrupt. SC0TICR (x'3FF6') bp1 : SC0TIE = 1	(15) Set the SC0TIE flag of the SC0TICR register to "1" to enable interrupts. If any interrupt request flag (SC0TIR of the SC0TICR register) is already set, clear SC0TIR before an interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(16) Start serial transmission. Transmission data→TXBUF0 (x'3F95') Received data→input to SBI pin.	(16) Set the transmission data to the serial transmission data buffer TXBUF0. Then, an internal clock is generated to start transmission / reception. After the transmission is finished, serial0 transmission interrupt SC0TIRQ is generated.

Note : Each procedure (5) to (8), (9) to (11), and (11) to (13) can be set at the same time.

When only reception with 3 channels are operated, set SC0SBOS of the SC0MD1 register to "0" and select a port. The SBO pin can be used as a general port.

When SBO / SBI pin are connected for communication with 2 lines, the SBO pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIS of the SC0MD1 register to "1", always, to select "serial data input". The SBI pin can be used as a general port.

This serial interface contains a emergency reset function. If the communication should be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (except Table 11-2-1 : TXBUF0, RXBUF0) are set.

Transfer rate of transfer clock set by SC0CKS register should be under 2.5 MHz.

11-3-3 UART Serial Interface

Serial 0 can be used for duplex UART communication. Table 11-3-12 shows UART serial interface functions.

Table 11-3-17 UART Serial Interface Functions

Communication style	UART(duplex)
Interrupt	SC0TIRQ(transmission), SC0RIRQ(reception)
Used pins	TXD(output, input) RXD(input)
Specification the first transfer bit	MSB / LSB
Selection of parity bit	√
Parity bit control	0 parity 1 parity odd parity even parity
Frame selection	7 bits + 1 STOP 7 bits + 2 STOPs 8 bits + 1 STOP 8 bits + 2 STOPs
Continuous operation	√
Maximum transfer rate	300 kbps (standard 300 bps to 38.4 kbps) (with baud rate timer)

*Descriptions of TXD, RXD on this table also applied to both Port0 (TXDA/RXDA) and PortB (TXDB/RXDB).

■Activation Factor for Communication

At transmission, if any data is set to the transmission data buffer TXBUF0, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. At reception, if the data length of "L" for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■Transmission

Data transfer is automatically started by setting data to the transmission data buffer TXBUF0. When the transmission is completed, the serial 0 transmission interrupt SC0TIRQ is generated.

■Reception

Once a start condition is received, reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial 0 reception interrupt SC0RIRQ is generated.

■Duplex communication

On duplex communication, the transmission and reception can be operated separately at the same time. The frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■Transfer bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SC0FM1 to 0 flag of the SC0MD2 register. If the SC0CMD flag of the SC0MD1 register is set to "1", and UART communication is selected, the setup by the synchronous serial transfer bit count selection flag SC0LNG2 to 0 is no more valid.

■Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD pin), data input pin (RXD pin)), or with 1 channel (data I/O pin TXD pin). The RXD pin can be used only for serial data input. The TXD pin can be used for serial data input or output. The SC0IOM flag of the SC0MD1 register can specify which pin, RXD or TXD inputs the serial data. If "data input from TXD pin" is selected to be with 1 line communication, transmission / reception is switched by controlling TXD pin's direction by the P0DIR0 flag of the P0DIR register. At that time, the RXD pin can be used as a general port.

Port0 pins (TXDA/P00, RXDA/P01) are normally assigned as serial interface data I/O pins, which can be substituted with PortB pins (TXDB/PB5, RXDB/PB6).
Serial interface I/O pins are selected with SC0SEL flag of the FLOAT register. To select Port0 set "0" to the SC0SEL flag, and to select PortB set "1" to the SC0SEL flag.

■Reception Buffer Empty Flag

When SC0RIRQ is generated, data is stored to RXBUF0 from the internal shift register, automatically. If data is stored to the shift register RXBUF0, the reception buffer empty flag SC0REMP of the SC0MD3 register is set to "1". That indicates that the received data is going to be read out. SC0REMP is cleared to "0" by reading out the data of RXBUF0.

■Reception BUSY flag

When the start condition is reagrded, the SC0RBSY flag of the SC0MD3 register is set to "1". That is cleared to "0" by the generation of the reception complete interrupt SC0RIRQ. If the SC0SBIS flag is set to "0" during receptin, the SC0RBSY flag is reset to "0".

■Transmission BUSY flag

When any data is set to TXBUF0, the SC0TBSY flag of the SC0MD3 register is set to "1". That is cleared to "0" by the generation of the transmission complete interrupt SC0TIRQ. During continuous communication the SC0TBSY flag is always set. If the transmission buffer empty flag S0TEMP is set to "0" as the transmission complete interrupt SC0TIRQ is generated, the SC0TBSY is cleared to "0". If the SC0SBOS flag is set to "0", the SC0TBSY flag is reset to "0".

■Frame Mode and Parity Check Setup

Figure 11-3-15 shows the data format at UART communication.

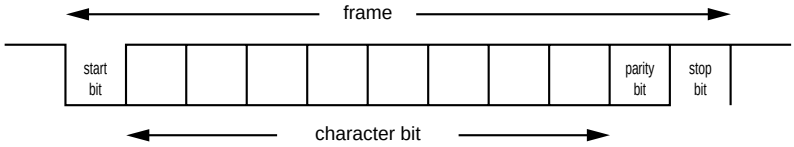


Figure 11-3-15 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit.
Table 11-3-13 shows its kinds to be set.

Table 11-3-18 UART Serial Interface Transmission / Reception Data

Start bit	1 bit
Character bit	7, 8 bits
Parity bit	fixed to 0, fixed to 1, even, odd, none
Stop bit	1, 2 bits

The SC0FM1 to 0 flag of the SC0MD2 register sets the frame mode. Table 11-3-19 shows the UART serial interface frame mode settings. If the SC0CMD flag of the SC0MD1 register is set to "1", and UART communication is selected, the transfer bit count on the SC0LNG2 to 0 flag of the SC0MD0 register is no more valid.

Table 11-3-19 UART Serial Interface Frame Mode

SC0MD2 register		Frame mode
SC0FM1	SC0FM0	
0	0	Character bit 7 bits + Stop bit 1 bit *
0	1	Character bit 7 bits + Stop bit 2 bits *
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data.
Table 11-3-20 shows kinds of parity bit. The SC0NPE, SC0PM1 to 0 flag of the SC0MD2 register set parity bit.

Table 11-3-20 Parity bit of UART Serial Interface

SC0MD2 register			Parity bit	Setup
SC0NPE	SC0PM1	SC0PM0		
0	0	0	fixed to 0	Set parity bit to "0".
0	0	1	fixed to 1	Set parity bit to "1".
0	1	0	odd parity	Control that the total of "1" of parity bit and character bit should be odd.
0	1	1	even parity	Control that the total of "1" of parity bit and character bit should be even.
1	-	-	none	Do not add parity bit.

■Brake Status Transmission Control Setup
The SC0BRKE flag of the SC0MD2 register generates the brake status. If SC0BRKE is set to "1" to select the brake transmission, all bits from start bits to stop bits transfer "0".

■Reception Error

At reception , there are 3 types of error ; overrun error, parity error and framing error. Reception error can be determined by the SC0ORE, SC0PEK, SC0FEF flag of the SC0MD3 register. Even one of those errors is detected, the SC0ERE flag of the SC0MD3 register is set to "1". The SC0PEK, the SC0FEF flags in recepption error flag are renewed at generation of the reception complete interrupt SC0RIRQ. The SC0ORE flag holds the status unless data of RXBUF0 is read out. The decision of the received error flag should be operated until the next communication is finished. Those error flag has no effect on communication operation. Table 11-3-16 shows the list of reception error source.

Table 11-3-21 Reception Error Source of UART Serial Interface

Flag	Error	Error source	
SC0ORE	Overrun error	Next data is received before reading the receive buffer.	
SC0PEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	when parity bit is "0"
		odd parity	The total of "1" of parity bit and character bit is even.
		even parity	The total of "1" of parity bit and character bit is odd.
SC0FEF	Framing error	Stop bit is not detected.	

■Judgement of Brake Status Reception

Reception at brake status can be judged. If all received data from start bit and stop bit is "0", the SC0BRKF flag of the SC0MD2 register is set and regards the brake status. The SC0BRKF flag is set at generation of the reception complete interrupt SC0RIRQ.

■Continuous Communication

This serial interface has continuous communication function. If data is set to the transmission data buffer TXBUF0 during communication, the transmission buffer empty flag SC0TEMP is set to continue automatic communication. This does not generate any blank in communication. Set data to TXBUF0 between previous data setup and generation of the communication complete interrupt SC0TIRQ.

■Changing Polarity of Transmission / Reception Data

The polarity of the transmission / reception data can not be swtched during UART communication, Therefore, setting SC0TRN and SC0REN flags of the SC0MD0 register has no effect during UART communication.

■Clock Setup

Transfer clock is not necessary for UART communication itself, but necessary for setup of data transmission / reception timing in the serial interface.

Select the timer to be used as a baud rate timer by the SC0CKS register, and set the SC0MST flag of the SC0MD1 register to "1" to select the internal clock (clock master).

At UART communication, set the SC0MST flag of the SC0MD1 register to "1". If "0" is set, the communication is disabled.

■Tranfer Bit Count and First Transfer Bit

When the transfer bit is 7 bits, the data storing method to the transmission data buffer TXBUF0 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF0 for storing. When there are 7 bits to be transfered, as shown on figure 11-3-16, if data "A" to "G" are stored to bp1 to bp7 of TXBUF0, the transmission is operated from "G" to "A". At LSB first, use the lower bits of TXBUF0 for storing. When there are 7 bits to be transfered, as shown on figure 11-3-17, if data "A" to "G" are stored to bp0 to bp6 of TXBUF0, the transmission is operated from "A" to "G".

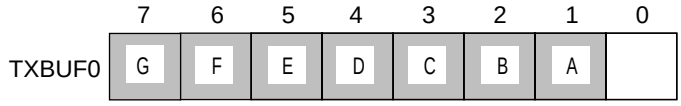


Figure 11-3-16 Transfer Bit Count and First Transfer Bit (starting with MSB)

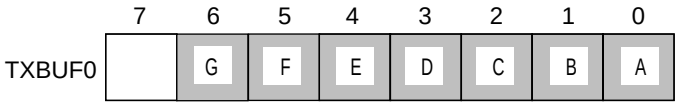


Figure 11-3-17 Transfer Bit Count and First Transfer Bit (starting with LSB)

■Receive Bit Count and First Transfer Bit

When the transfer bit count is 7 bits, the data storing method to the received data buffer RXBUF0 is different depending on the first transfer bit selection. At MSB first, data are stored to the upper bits of RXBUF0. When there are 7 bits to be transfered, as shown on figure 11-3-18, if data "G" to "A" are stored to bp7 to bp1 of RXBUF0. At LSB first, data are stored to the lower bits of RXBUF0. When there are 7 bits to be transfered, as shown on figure 11-3-19, if data "A" to "G" are stored to bp0 to bp6 of RXBUF0.

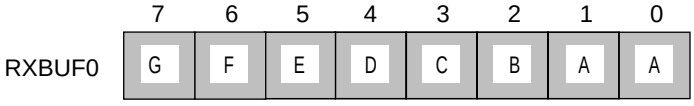


Figure 11-3-18 Receive Bit Count and Transfer First Bit (starting with MSB bit)

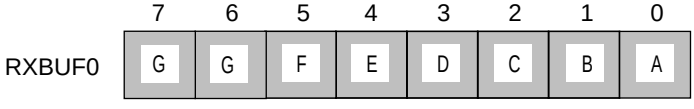


Figure 11-3-19 Receive Bit Count and Transfer First Bit (starting with LSB bit)

The following items are same as clock synchronous serial.
Reference as follows ;

■First Transfer bit Setup
Refer to : XI-14

■Transmission Data Buffer
Refer to : XI-14

■Received Data Buffer
Refer to : XI-14

■Transmission Buffer Empty Flag
Refer to : XI-18

■Emergency Reset
Refer to : XI-19

■Transmission Timing

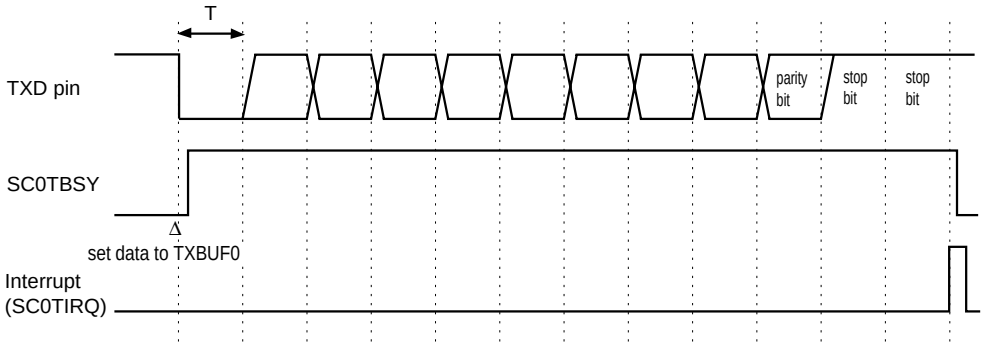


Figure 11-3-20 Transmission Timing (parity bit is enabled)

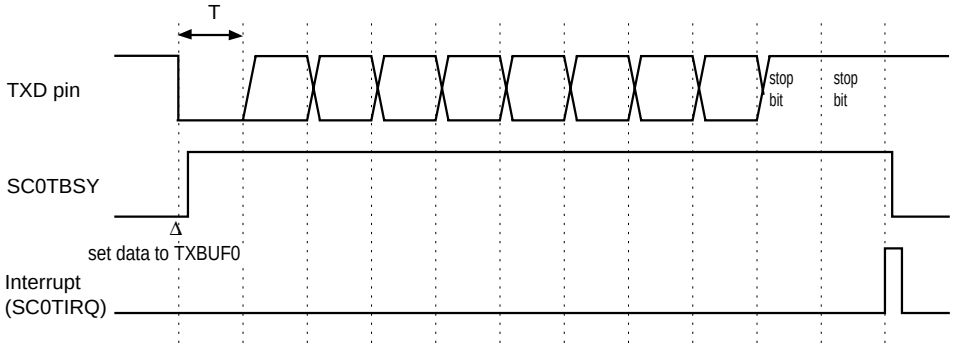


Figure 11-3-21 Transmission Timing (parity bit is disabled)

■Reception Timing

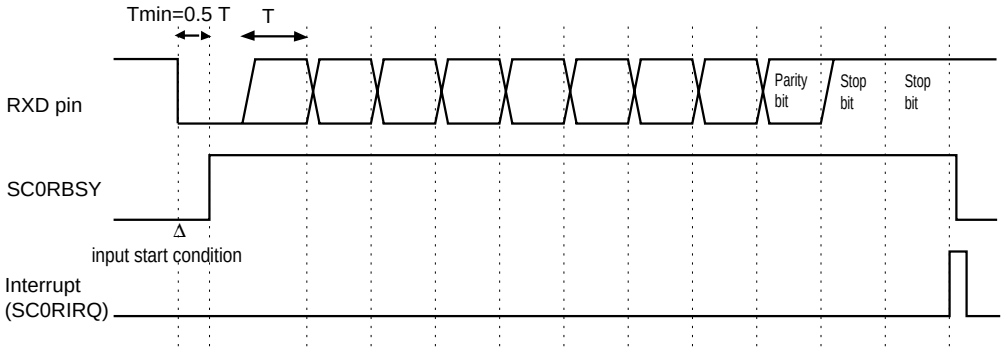


Figure 11-3-22 Reception Timing (parity bit is enabled)

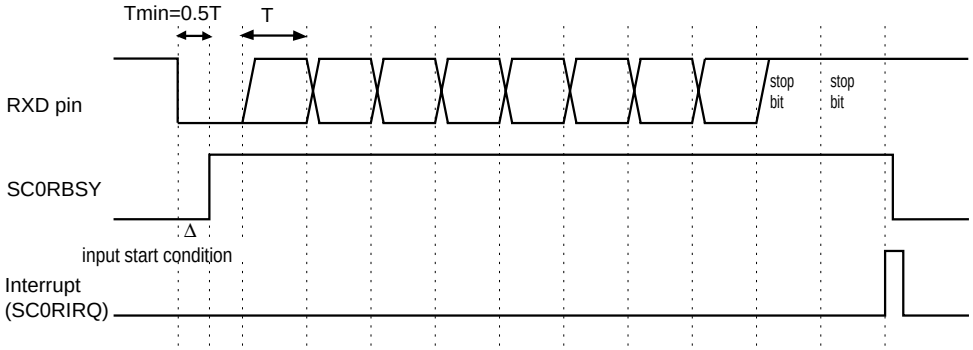


Figure 11-3-23 Reception Timing (parity bit is disabled)

■Transfer Speed Setup

Baud rate timer can set any transfer rate.

Table 11-3-22 shows the setup example of the transfer speed. Refer to chapter 6. 8-bit Timer for baud rate timer setup.

Table 11-3-22 UART Serial Interface Transfer Speed Setup Register

Setup	Register	Page
Serial 0 clock source (timer output)	SC0CKS	V - 9, XI - 12
Timer clock source	TMnMD	VI - 10 to 13
Timer compare register	TMnOC	VI - 8

Timer compare register is set as follows ;

overflow cycle = (set value of compare register + 1) x timer clock cycle

baud rate = 1 / (overflow cycle x 2 x 8) ("8" means that clock source is divided by 8)

therefore,

set value of compare register = timer clock frequency / (baud rate x 2 x 8) - 1

For example, if baud rate should be 300 bps at timer clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows ;

Set value of comapre register = $(8 \times 10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= x'CF'

Timer clock source and the set value of timer comapre register at the standard rate are shown in the following page.

Transfer rate should be selected under 300 kbps.

Table 11-3-23-1 Setup Value of UART Serial Interface Transfer Speed (decimal)

fosc (MHz)	Clock source (timer)	Transfer speed (bps)									
		300		960		1200		2400		4800	
		Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value
4.00	fosc	-	-	-	-	207	1202	103	2404	51	4808
	fosc/4	207	300	64	962	51	1202	25	2404	12	4808
	fosc/16	51	300	-	-	12	1202	-	-	-	-
	fosc/32	25	300	-	-	-	-	-	-	-	-
	fosc/64	12	300	-	-	-	-	-	-	-	-
	fs/2	207	300	64	962	51	1202	25	2404	12	4808
	fs/4	104	297	-	-	25	1202	12	2404	-	-
4.19	fosc	-	-	-	-	217	1201	108	2403	54	4761
	fosc/4	217	300	67	963	-	-	-	-	-	-
	fosc/16	-	-	16	963	-	-	6	2338	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	217	300	67	963	-	-	-	-	-	-
	fs/4	108	300	33	963	-	-	13	2338	-	-
8.00	fosc	-	-	-	-	-	-	207	2404	103	4808
	fosc/4	-	-	129	962	103	1202	51	2404	25	4808
	fosc/16	103	300	-	-	25	1202	12	2404	-	-
	fosc/32	51	300	-	-	12	1202	-	-	-	-
	fosc/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	129	962	103	1202	51	2404	25	4808
	fs/4	207	300	64	962	51	1202	25	2404	12	4808
8.38	fosc	-	-	-	-	-	-	217	2403	108	4805
	fosc/4	-	-	135	963	108	1201	-	-	-	-
	fosc/16	108	300	33	963	-	-	13	2338	-	-
	fosc/32	-	-	16	963	-	-	6	2338	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	135	963	108	1201	-	-	-	-
	fs/4	217	300	67	963	-	-	-	-	-	-
12.00	fosc	-	-	-	-	-	-	-	-	155	4808
	fosc/4	-	-	194	962	155	1202	77	2404	38	4808
	fosc/16	155	300	-	-	38	1202	-	-	-	-
	fosc/32	77	300	-	-	-	-	-	-	-	-
	fosc/64	38	300	-	-	-	-	-	-	-	-
	fs/2	-	-	194	962	155	1202	77	2404	38	4808
	fs/4	-	-	-	-	77	1202	38	2404	-	-
16.00	fosc	-	-	-	-	-	-	-	-	207	4808
	fosc/4	-	-	-	-	207	1202	103	2404	51	4808
	fosc/16	207	300	64	962	51	1202	25	2404	12	4808
	fosc/32	103	300	-	-	25	1202	12	2404	-	-
	fosc/64	51	300	-	-	12	1202	-	-	-	-
	fs/2	-	-	-	-	207	1202	103	2404	51	4808
	fs/4	-	-	129	962	103	1202	51	2404	25	4808
16.76	fosc	-	-	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	217	1201	108	2403	54	4761
	fosc/16	217	300	67	963	-	-	-	-	-	-
	fosc/32	108	300	33	963	-	-	-	-	-	-
	fosc/64	-	-	16	963	-	-	-	-	-	-
	fs/2	-	-	-	-	217	1201	108	2403	54	4761
	fs/4	-	-	135	963	108	1201	54	2381	-	-
20.00	fosc	-	-	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	129	2404	64	4808
	fosc/16	-	-	-	-	64	1202	-	-	-	-
	fosc/32	129	300	-	-	-	-	-	-	-	-
	fosc/64	64	300	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	129	2404	64	4808
	fs/4	-	-	162	959	129	1202	64	2404	-	-

Table 11-3-23-2 Setup Value of UART Serial Interface Transfer Speed (decimal)

		Transfer speed (bps)									
fosc (MHz)	Clock source (timer)	9600		19200		28800		31250		38400	
		Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value
4.00	fosc	25	9615	12	19231	-	-	7	31250	-	-
	fosc/4	-	-	-	-	-	-	1	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
4.19	fosc	26	9699	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
8.00	fosc	51	9615	25	19231	-	-	15	31250	12	38462
	fosc/4	12	9615	-	-	-	-	3	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
8.38	fosc	54	9523	26	19398	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
12.00	fosc	77	9615	38	19231	25	28846	23	31250	-	-
	fosc/4	-	-	-	-	-	-	5	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	5	31250	-	-
	fs/4	-	-	-	-	-	-	2	31250	-	-
16.00	fosc	103	9615	51	19231	-	-	31	31250	25	38462
	fosc/4	25	9615	12	19231	-	-	7	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	25	9615	-	-	-	-	7	31250	-	-
	fs/4	12	9615	-	-	-	-	3	31250	-	-
16.76	fosc	108	9610	54	19045	-	-	-	-	-	-
	fosc/4	26	9699	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	26	9699	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
20.00	fosc	129	9615	64	19231	-	-	39	31250	-	-
	fosc/4	-	-	-	-	-	-	9	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	9	31250	-	-
	fs/4	-	-	-	-	-	-	4	31250	-	-

■Pin Setup (with 1, 2 channels, at transmission)

Table 11-3-24 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXDA pin, RXDA pin, regardless of those pins are independednt / connected.

Table 11-3-24 UART Serial Interface Pin Setup (with 1, 2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXDA pin	RXDA pin
Port pin	P00	P01
TXD / RXD pins	TXD / RXD pins connected or independent	
	SC0MD1(SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC(SC0ODC0)	
I/O	Output mode	-
	P0DIR(P0DIR0)	
Pull-up	Added / Not added	-
	P0PLUD(P0PLUD0)	

■Pin Setup (with 2 channels, at reception)

Table 11-3-25 shows the pins setup at UART serial interface reception with 2 channels (TXDA pin, RXDA pin).

Table 11-3-25 UART Serial Interface Pin Setup (with 2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXDA pin	RXDA pin
Port pin	P00	P01
TXD / RXD pin	TXD / RXD pins connected or independent	
	SC0MD1(SC0IOM)	
Function	port	serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	-	input mode
	-	P0DIR(P0DIR1)
Pull-up	-	-

■Pin Setup (with 1 channel, at reception)

Table 11-3-26 shows the pin setup at UART serial interface reception with 1 channel (TXDA pin). The RXDA pin is not used, so can be used as a port.

Table 11-3-26 UART Serial Interface Pin Setup (with 1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXDA pin	RXDA pin
Port pin	P00	P01
TXD / RXD pin	TXD / RXD pins connected	
	SC0MD1(SC0IOM)	
Function	Port	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	Input mode	-
	P0DIR(P0DIR0)	-
Pull-up	-	-

■Pin Setup (with 2 channels, at transmission / reception)

Table 11-3-27 shows the pin setup at UART serial interface transmission / reception with 2 channels (TXDA pin, RXDA pin).

Table 11-3-27 UART Serial Interface Pin Setup (with 2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXDA pin	RXDA pin
Port pin	P00	P01
TXD / RXD pins	TDX / RXD pins independent	
	SC0MD1(SC0IOM)	
Function	Serial data output	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC(SC0ODC0)	
I/O	Output mode	Input mode
	P0DIR(P0DIR0)	P0DIR(P0DIR1)
Pull-up	Added / Not added	-
	P0PLUD(P0PLUD0)	

■Pin Setup (with 1, 2 channels, at transmission)

Table 11-3-28 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXDB pin, RXDB pin, regardless of those pins are independednt / connected.

Table 11-3-28 UART Serial Interface Pin Setup (with 1, 2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXDB pin	RXDB pin
Port pin	PB5	PB6
TXD / RXD pins	TXD/RXD pins connected or independent	
	SC0MD1(SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC(SC0ODC0)	
I/O	Output mode	-
	PBDIR(PBDIR5)	
Pull-up	Added / Not added	-
	PBPLU(PBPLU5)	

■Pin Setup (with 2 channels, at reception)

Table 11-3-29 shows the pins setup at UART serial interface reception with 2 channels (TXDB pin, RXDB pin).

Table 11-3-29 UART Serial Interface Pin Setup (with 2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXDB pin	RXDB pin
Port pin	PB5	PB6
TXD / RXD pin	TXD/RXD pins connected	
	SC0MD1(SC0IOM)	
Function	port	serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	-	input mode
	-	PBDIR(PBDIR5)
Pull-up	-	-

■Pin Setup (with 1 channel, at reception)

Table 11-3-30 shows the pin setup at UART serial interface reception with 1 channel (TXDB pin). The RXDB pin is not used, so can be used as a port.

Table 11-3-30 UART Serial Interface Pin Setup (with 1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXDB pin	RXDB pin
Port pin	PB5	PB6
TXD / RXD pin	TXD/RXD pins connected	
	SC0MD1(SC0IOM)	
Function	port	serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	input mode	-
	PBDIR(PBDIR5)	-
Pull-up	-	-

■Pin Setup (with 2 channels, at transmission / reception)

Table 11-3-31 shows the pin setup at UART serial interface transmission / reception with 2 channels (TXDB pin, RXDB pin).

Table 11-3-31 UART Serial Interface Pin Setup (with 2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXDB pin	RXDB pin
Port pin	PB5	PB6
TXD / RXD pin	TXD/RXD pins independent	
	SC0MD1(SC0IOM)	
Function	serial data output	serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC(SC0ODC0)	
I/O	output mode	input mode
	PBDIR(PBDIR5)	PBDIR(PBDIR6)
Pull-up	Added / Not added	-
	PBPLU(PBPLU5)	

11-3-4 Setup Example

■Transmission / Reception Setup

The setup example at UART transmission / reception with serial 0 is shown.

Table 11-3-32 shows the conditions at transmission / reception.

Table 11-3-32 UART Interface Transmision Reception Setup

Setup item	set to
TXD / RXD pin	independent (with 2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	timer 3
TXD0 / RXD0 pin type	Nch open-drain
Pull-up resistor of TXD pin	added
Parity bit add / check	"0"add / check
Serial 0 transmission complete interrupt	Enable.
Serial 0 reception complete interrupt	Enable.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select prescaler operation.
(2) Select the clock source. SC0CKS (x'3F97') bp2-0 : SC0PSC2-0= 111 bp3 : SC0TMSEL= 1	(2) Set the bp3-0 flag of the SC0CKS register to "1111" to select timer 3 output as a clock source.
(3) Control the pin type. SC0ODC (x'3F96') bp0 : SC0ODC0 = 1 P0PLUD (x'3F40') bp0 : P0PLUD0 = 1	(3) Set the SC0ODC0 flag of the SC0ODC register to "1" to select N-ch open drain for the TXD pin. Set the P0PLUD0 flag of the P0PLUD register to "1" to add pull-up resistor.
(4) Control the pin direction. P0DIR (x'3F30') bp1-0 : P0DIR1-0 = 01	(4) Set the P0DIR1-0 flag of the port 0 pin direction control register (P0DIR) to "01" to set P00 to output mode, and P01 to input mode.
(5) Set the SC0MD0 register. Select the start condition. SC0MD0 (x'3F90') bp3 : SC0STE = 1	(5) Set the SC0STE flag of the SC0MD0 register to "1" to enable start condition.

Setup Procedure	Description
(6) Select the first bit to be transfered. SC0MD0 (x'3F90') bp4 : SC0DIR = 0	(6) Set the SC0DIR flag of the SC0MD0 register to "0" to select MSB as first transfer bit.
(7) Set the SC0MD2 register. Control the output data. SC0MD2 (x'3F92') bp0 : SC0BRKE = 0	(7) Set the SC0BRKE flag of the SC0MD2 register to "0" to select serial data transmission.
(8) Select the added parity bit. SC0MD2 (x'3F92') bp3 : SC0NP = 0 bp5-4 : SC0PM1-0 = 00	(8) Set the SC0PM1-0 flag of the SC0MD2 register to "00" to select 0 parity, and set the SC0NPE flag to "0" to add parity bit.
(9) Specify the flame mode. SC0MD2 (x'3F92') bp7-6 : SC0FM1-0 = 11	(9) Set the SC0FM1-0 flag of the SC0MD2 register to "11" to select 8 bits + 2 stop bits at the flame mode.
(10) Set the SC0MD1 register. Select the communication type. SC0MD1 (x'3F91') bp0 : SC0CMD = 1	(10) Set the SC0CMD flag of the SC0MD1 register to "1" to select duplex UART.
(11) Select the clock frequency. SC0MD1 (x'3F91') bp3 : SC0CKM = 1 bp2 : SC0MST = 1	(11) Set the SC0CKM flag of the SC0MD1 register to "1" to select "divided by 8" at source clock. And, the SC0MST flag should be always set to "1" to select colck master.
(12) Control the pin function. SC0MD1 (x'3F91') bp4 : SC0SBOS = 1 bp5 : SC0SBIS = 1 bp7 : SC0IOM = 0	(12) Set the SC0SBOS, SC0SBIS flag of the SC0MD1 register to "1" to set the TXD pin to serial data output and the RXD pin to serial data input.
(13) Enable the interrupt. SC0RICR (x'3FF5') bp1 : SC0RIE = 1 SC0TICR (x'3FF6') bp1 : SC0TIE = 1	(13) Set the SC0RIE flag of the SC0RICR register to "1", and set the SC0TIE flag ot the SC0TICR register to "1" to enable the interrupt request. If any interrupt request flag is already set, clear them. [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]

Setup Procedure	Description
(14) Set the baud rate timer.	(14) Set the baud rate timer by the TM3MD register, the TM3OC register. Set the TM3EN flag to "1" to start timer 3. [☞ Chapter 6. 8-bit Timer]
(15) Start serial communication. The transmission data → TXBUF0 (x'3F95') The received data → input to RXD	(15) The transmission is started by setting the transmission data to the serial transmission data buffer (TXBUF0). When the transmission is finished, the serial 0 transmission interrupt (SC0TIRQ) is generated. After the serial data is input from the RXD pin and the start condition is recognized, the received data is stored. When the reception is finished, the received data is stored to the serial received data buffer RXBUF0 and the serial 0 reception data buffer interrupt SC0RICR is generated.

Note : (5) to (6), (7) to (9), (10) to (12) can be set at the same time.

When the TXD / RXD pin are connected for communication with 1 channel, the TXD pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIOS of the SC0MD1 register to "1" to select serial data input. The RXD pin can be used as a general port.

This serial interface contains emergency reset function. If communication need to be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as the setup procedure in order. Activation of communication should be operated after all control registers (except Table 11-2-1 : TXBUF0, RXBUF0) are set.

Only timer 3 can be used as a baud rate timer.
Refer to Chapter 6. 8-bit Timer for baud rate setup.

Chapter 12 Serial Interface 2

12

12-1 Overview

Serial interface 2 can be used for clock synchronous serial communication.

12-1-1 Functions

Table 12-1-1 shows the serial interface 2 functions.

Table 12-1-1 Serial Interface 2 Functions List

Communication style	Clock synchronous
Interrupt	SC2IRQ
Pins	SBO2,SBI2,SBT2
3 channels type	√
2 channels type	√(SBO2,SBT2)
Start condition	√
Transfer bit count	1 to 8 bit
First bit to be transfered	√
Input edge / Output edge	√
Continuous operation (with ATC1)	√
Clock source	fosc/2 fosc/4 fosc/16 fosc/32 fs/2 fs/4 timer 3 output external clock
Maximum transfer rate	2.5 MHz
fosc : machine clock (Oscillation for high speed) fs : system clock [☞ Chapter 2 2-5. Clock Switching]	

12-1-2 Block Diagram

■Serial Interface 2 Block Diagram

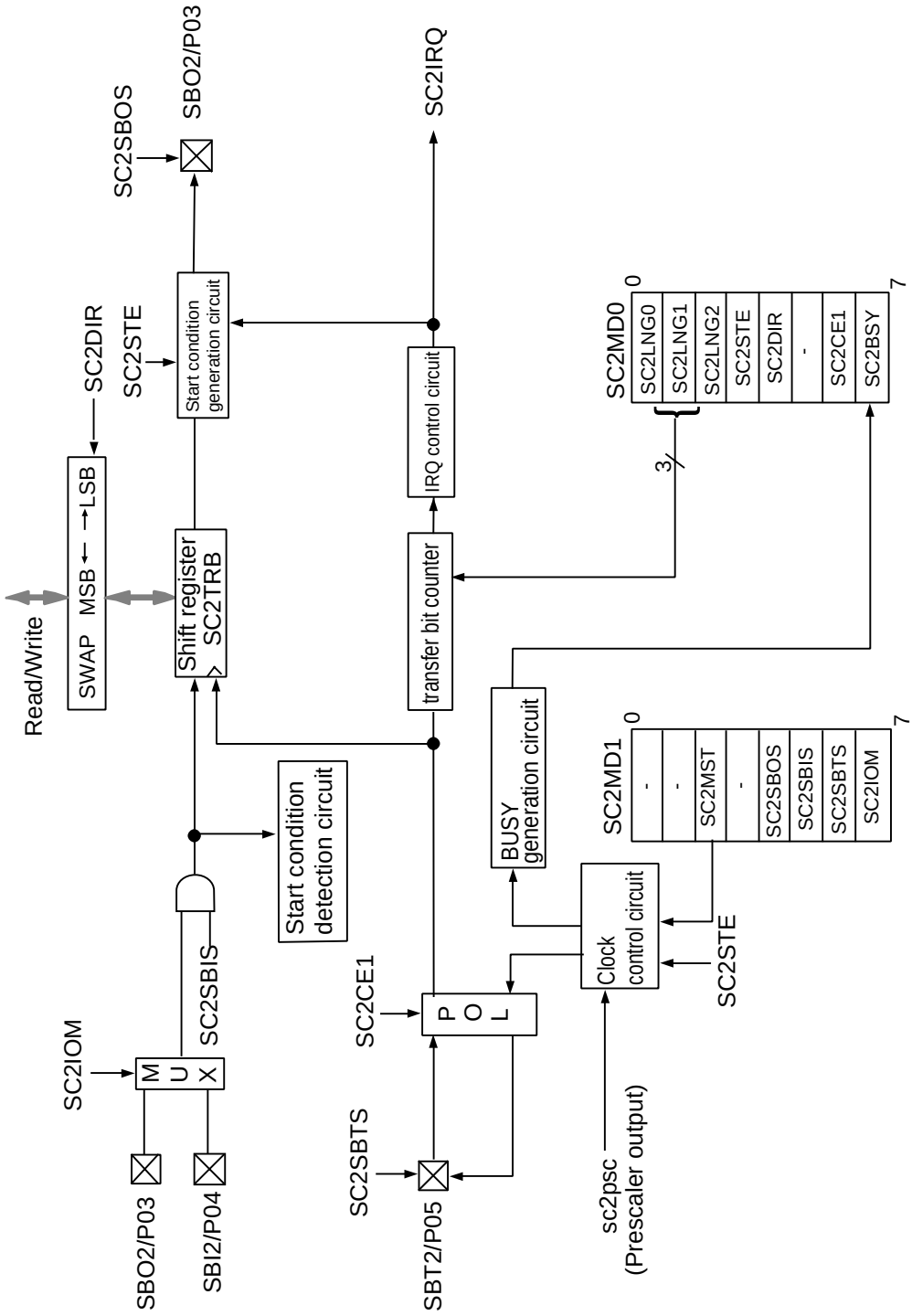


Figure 12-1-1 Serial Interface 2 Block Diagram

12-2 Control Registers

12-2-1 Registers List

Table 12-2-1 shows the registers to control serial interface 2.

Table 12-2-1 Serial Interface 2 Control Registers List

	Register	Address	R/W	Function	Page
Serial 2	SC2MD0	x'03FA0'	R/W	Serial interface 2 mode register 0	XII - 6
	SC2MD1	x'03FA1'	R/W	Serial interface 2 mode register 1	XII - 7
	SC2TRB	x'03FA2'	R/W	Serial interface 2 transmit/receive shift register	XII - 5
	SC2ODC	x'03FA6'	R/W	Serial interface 2 port control register	XII - 8
	SC2CKS	x'03FA7'	R/W	Serial interface 2 transfer clock selection register	V - 9, XII - 8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLUD	x'03F40'	R/W	Port 0 pull-up / pull-down control register	IV - 7
	FLOAT	x'03F2E'	R/W	Pull-up / pull-down resistor control, Pin control register	IV-8, 16, 31, 59, XI - 8
	SC2ICR	x'03FF8'	R/W	Serial interface 2 interrupt control register	III - 38

R /W : Readable / Writable

12-2-2 Data Register

Serial interface 2 has a 8-bit serial data register.

■Serial Interface 2 Transmission / Reception Shift Register (SC2TRB)

	7	6	5	4	3	2	1	0	
SC2TRB	SC2TRB7	SC2TRB6	SC2TRB5	SC2TRB4	SC2TRB3	SC2TRB2	SC2TRB1	SC2TRB0	(at reset: XXXXXXXX)

Figure 12-2-2 Serial Interface 2 Transmission / Reception Shift Register (SC2TRB : x'03FA2', R/W)

12-2-3 Mode Registers

■Serial Interface 2 Mode Register 0 (SC2MD0)

	7	6	5	4	3	2	1	0
SC2MD0	SC2BSY	SC2CE1	-	SC2DIR	SC2STE	SC2LNG2	SC2LNG1	SC2LNG0

(At reset : 0 0 - 0 0 1 1 1)

SC2LNG2	SC2LNG1	SC2LNG0	Synchronous serial transfer bit count
0	0	0	1 bit
		1	2 bits
	1	0	3 bits
		1	4 bits
1	0	0	5 bits
		1	6 bits
	1	0	7 bits
		1	8 bits

SC2STE	Start condition selection
0	Disable start condition
1	Enable start condition

SC2DIR	First bit to be transfered
0	MSB first
1	LSB first

SC2CE1	Transmission data output edge	Reception data input edge
0	Falling	Rising
1	Rising	Falling

SC2BSY	Serial bus status
0	Other use
1	Serial transmission in progress

Figure 12-2-3 Serial Interface 2 Mode Register 0
(SC2MD0 : x'03FA0', R/W)

■Serial Interface 2 Mode Register 1 (SC2MD1)

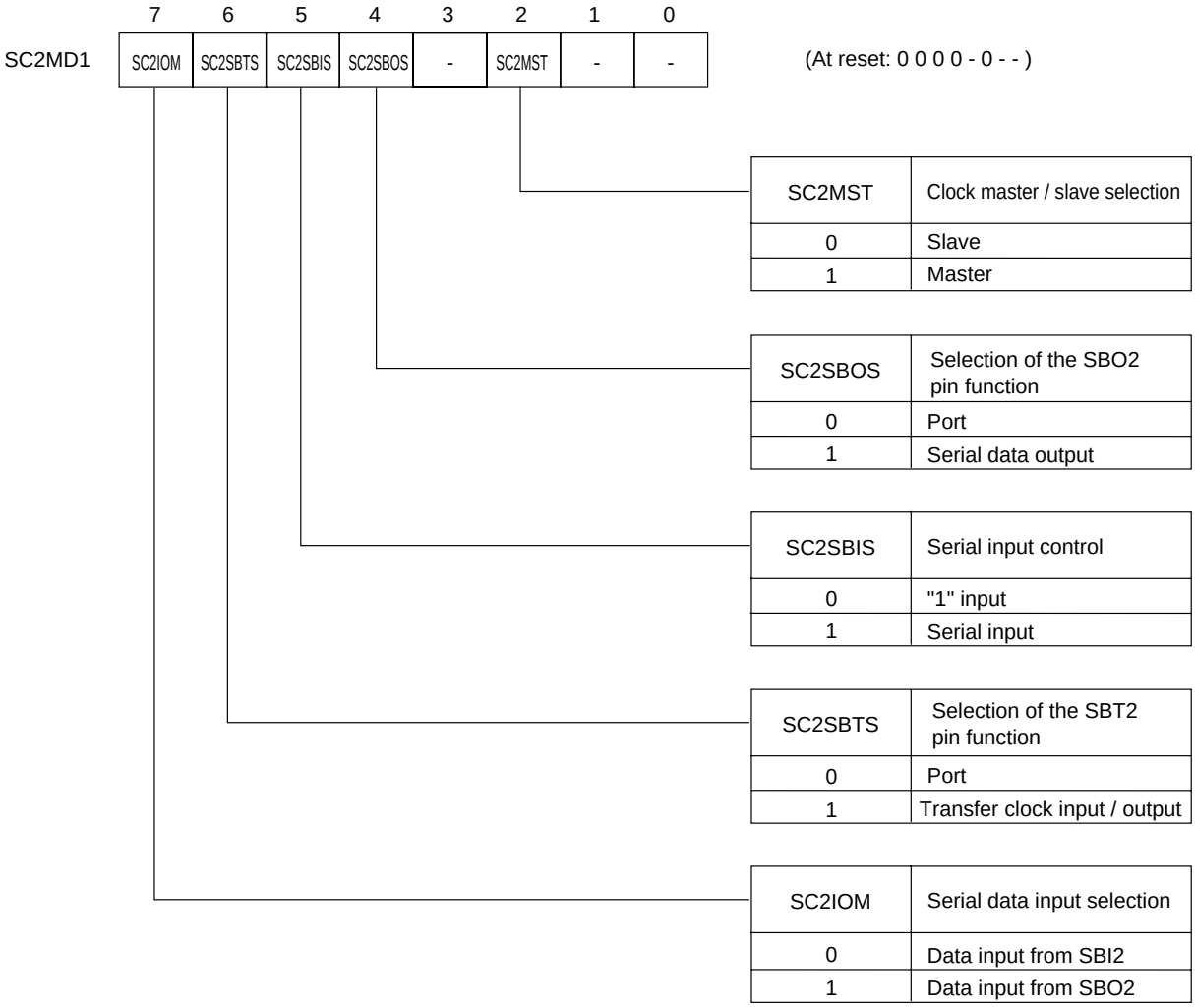

7 6 5 4 3 2 1 0
SC2MD1
SC2IOM SC2SBTS SC2SBIS SC2SBOS - SC2MST - -
(At reset: 0 0 0 0 - 0 - -)
SC2MST Clock master / slave selection
0 Slave
1 Master
SC2SBOS Selection of the SBO2 pin function
0 Port
1 Serial data output
SC2SBIS Serial input control
0 "1" input
1 Serial input
SC2SBTS Selection of the SBT2 pin function
0 Port
1 Transfer clock input / output
SC2IOM Serial data input selection
0 Data input from SBI2
1 Data input from SBO2

Figure 12-2-4 Serial Interface 2 Mode Register 1
(SC2MD1 : x'03FA1', R/W)

■Serial Interface 2 Port Control Register (SC2ODC)

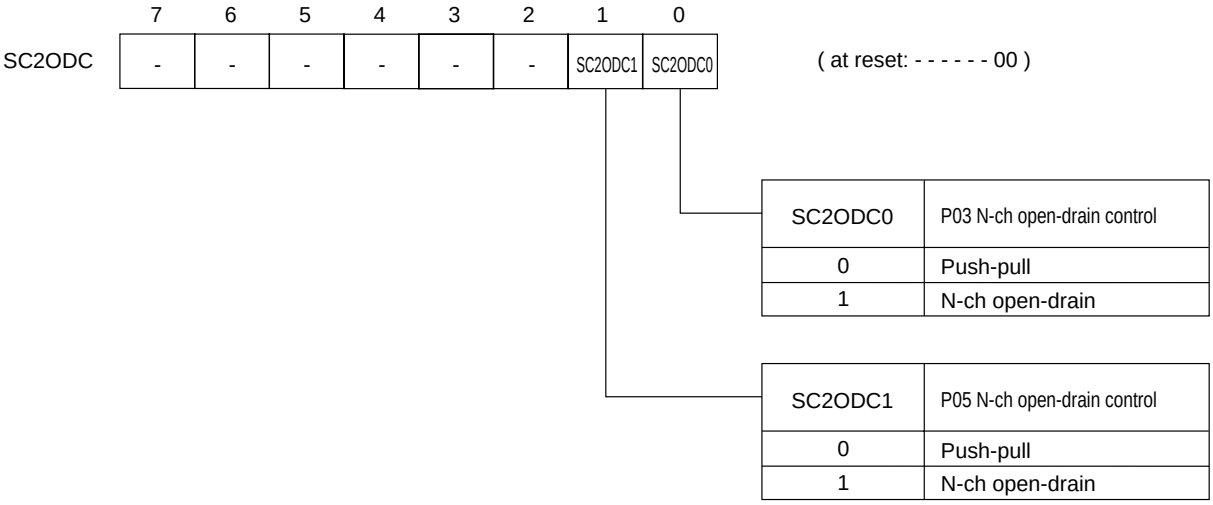

7 6 5 4 3 2 1 0
SC2ODC
- - - - - - SC2ODC1 SC2ODC0
(at reset: - - - - - - 00)
SC2ODC0 P03 N-ch open-drain control
0 Push-pull
1 N-ch open-drain
SC2ODC1 P05 N-ch open-drain control
0 Push-pull
1 N-ch open-drain

Figure 12-2-5 Serial Interface 2 Port Control Register
(SC2ODC : x'03FA6', R/W)

■Serial Interface 2 Transfer Clock Selection Register (SC2CKS)

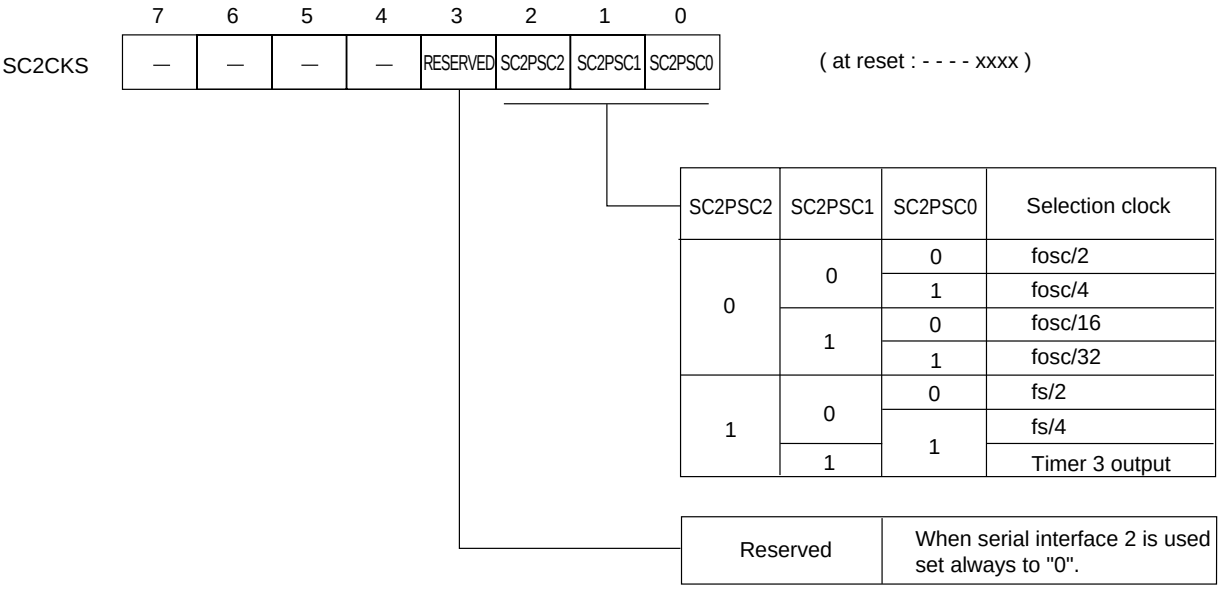

7 6 5 4 3 2 1 0
SC2CKS
— — — — RESERVED SC2PSC2 SC2PSC1 SC2PSC0
(at reset : - - - - xxxx)
SC2PSC2 SC2PSC1 SC2PSC0 Selection clock
0 0 0 fosc/2
1 fosc/4
1 0 fosc/16
1 fosc/32
1 0 0 fs/2
1 fs/4
1 Timer 3 output
Reserved
When serial interface 2 is used set always to "0".

Figure 12-2-6 Serial Interface 2 Transfer Clock Selection Register
(SC2CKS : x'03FA7', R/W)

12-3 Operation

Serial interface 2 is clock synchronous serial interface.

12-3-1 Clock Synchronous Serial Interface

■Activation Factor for Communication

Table 12-3-1 shows the activation source for communication. At master communication, a transfer clock is generated by setting data to the transmission / receiption shift register SC2TRB, or by receiving a start condition. Except during communication, input signals from SBT2 pin are masked inside serial interface to prevent errors by noise. This mask is automatically released by setting data to SC2TRB (writing to the SC2TRB register), or inputting start condition to the data input pin. Therefore, at slave communication, input external clock after data is set to SC2TRB, or after start condition is input.

Table 12-3-1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
Master communication	Set the transmission data	Set dummy data
		Input start condition
Slave communication	Input clock after the transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■Transfer bit Count Setup

The transfer bit count can be selected from 1 bit to 8 bits. Set the SC2LNG 2 to 0 flag of the SC2MD0 register (at reset : 111). The SC2LNG 2 to 0 flag holds the former value, until it is set again.

The SBT2 pin is masked inside the serial interface, to prevent errors by noise, except during communication. At slave, input clock to the SBT2 pin after data is set to SC2TRB or after start condition is input.

■Start Condition Setup

The SC2STE flag of the SC2MD0 register sets if start condition is enable or not. If a start condition is enabled, the bit counter is cleared as start condition is input during communication. Then, the communication is automatically restarted. When the data line (SBI2 pin (with 3 channels) or SBO2 pin (with 2 channels)) changes from "H" to "L" as clock line(SBT2 pin) is "H", start condition is enabled.

■First Transfer bit Setup

The SC2DIR flag of the SC2MD0 register can set the first bit to be transferred. LSB or MSB can be selected.

■Transmission, Reception Data Buffer

The transmission / receiption shift register SC2TRB is used as the common data register for transmission / reception. The transmission data should be set to SC2TRB. Data is shifted in 1-bit unit by transfer clock, and the received data is shifted in 1-bit unit to SC2TRB to be stored.

■Transfer bit Count and First Transfer bit

When the transfer bit count is 1 to 7 bits, data storing method to the transmission / receiption shift register SC2TRB is different, depending on the first transfer bit selection. When MSB is the first bit to be transferred, use the upper bits of SC2TRB for storing. When there are 6 bits to be transferred, as shown in figure 12-3-1-1, if data "A" to "F" are stored to bp2 to bp7 of SC2TRB, the data is transferred from "F" to "A". When LSB is the first bit to be transferred, use the lower bits of SC2TRB for storing. When there are 6 bits to be transferred, as shown in figure 13-3-1-2, if data "A" to "F" are stored to bp0 to bp5 of SC2TRB, the data is transferred from "A" to "F".

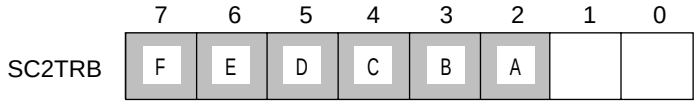


Figure 12-3-1-1 Transfer bit Count and First Transfer bit (MSB First)

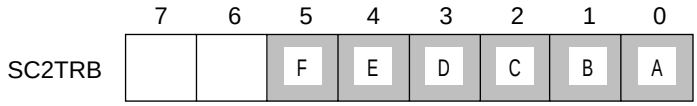


Figure 12-3-1-2 Transfer bit Count and First Transfer bit (LSB First)

■Receive bit Count and First Transfer bit

When the transfer bit count is 1 to 7 bits, data storing method to the transmit/receive shift register SC2TRB depending on the first transfer bit selection. When MSB is the first bit to be transferred, the lower bits of SC2TRB are used for storing. When there are 6 bits to be transferred, as shown in 12-3-1-3, data "A" to "F" are stored to bp0 to bp5 of SC2TRB in the order of "F" to "A". When LSB is the first bit to be transferred, use the upper bits of SC2TRB for storage. When there are 6 bits to be transferred, as shown in 12-3-1-4, data "A" to "F" are stored to bp2 to bp7 of SC2TRB in the order of "A" to "F".

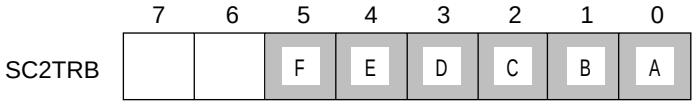


Figure 12-3-1-3 Receive bit Count and First Transfer bit (MSB First)

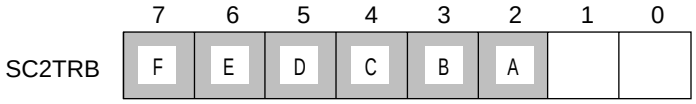


Figure 12-3-1-4 Receive bit Count and First Transfer bit (LSB First)

If start condition is input for activation again, during communication, the transmission data becomes invalid. If the transmission should be operated again, set the transmission data to SC2TRB, again.

■Clock Setup

Clock source is selected from the dedicated prescaler by using the SC2CKS register and timer 3 output. The dedicated prescaler is started to operate by selecting "prescaler operation" with the PSCMD (x'03F6F') register. The SC2MST flag of the SC2MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, the internal clock with same frequency as the external clock, should be set by the SC2CKS register, because the internal clock generates the interrupt flag SC2IRQ. Table 12-3-2 shows the internal clock source which can be set by the SC2CKS register.

Table 12-3-2 Synchronous Serial Interface Inside Clock Source

	Serial 2
Clock source (Internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/32
	fs/2
	fs/4
	timer 3 output

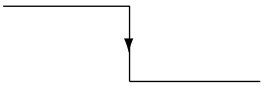
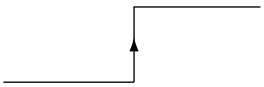
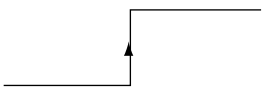
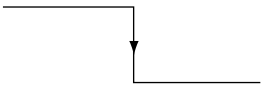
■BUSY flag Setup

If data is set to the transmission / receiption shift register SC2TRB, or start condition is enabled, the busy flag SC2BSY is set. That is cleared by the generation of the communication complete interrupt SC2IRQ.

■Input edge / output edge Setup

The SC2CE1 flag of the SC2MD0 register can set the output edge of the transmission data, and the input edge of the received data. Data at transmission is output at the falling edge of clock when the SC2CE1 flag = "0", and at the rising edge of clock when the SC2CE1 = "1". Data at reception is input at the rising edge of clock when the SC2CE1 = "0", and at the falling edge of clock as the SC2CE1 flag = "1".

Table 12-3-3 Input Edge / Output Edge of Transmission and Received Data

SC2CE1	Transmission data output edge	Received data input edge
0		
1		

■Data Input Pin Setup

There are 2 communication modes; 3 channels (clock pin(SBT2 pin), data output pin (SBO2 pin), data input pin (SBI2 pin)) and 2 channels (clock pin (SBT2 pin), data I/O pin (SBO2 pin)). The SBI2 pin can be used only for serial data input. The SBO2 pin can be selected for serial data input or output. The SC2IOM flag of the SC2MD1 register can specify if serial data is input from the SBI2 pin, or the SBO2 pin. When "data input from the SBO2 pin" is selected to communicate with 2 channels, the SBO2 pin's direction control by the P0DIR3 flag of the P0DIR register can switch the transmission / reception. At this time, the SBI2 pin is not used, so that it can be used as a general port.

The transfer speed should be up to 2.5 MHz. If the transfer clock is operated at more than 2.5 MHz, the transmission data may be output correctly.

■Emergency Reset for Communication

This LSI contains emergency reset function for abnormal operation. The emergency reset can be used by setting both of the SC2SBOS flag and the SC2SBIS flag of the SC2MD1 register to "0" (the SBO2 pin function : port, input data : input "1"). When the emergency reset is used, the SC2BSY flag of the SC2MD0 register is cleared, but other control registers hold their set values.

■Last bit of Transmission Data

Table 12-3-4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. At slave, setup for the internal clock is needed to keep data holding time at data transmission. After the last bit data output holding period, "H" is output.

Table 12-3-4 Last bit Data Length of Transmission Data

	at transmission Last bit data holding period	at reception Last bit data input period
at master	1 bit data length	1 bit data length (minimum)
at slave	[1 bit data length of external clock x 1/2] + [internal clock cycle x (1/2 to 1)]	

■Transmission Timing

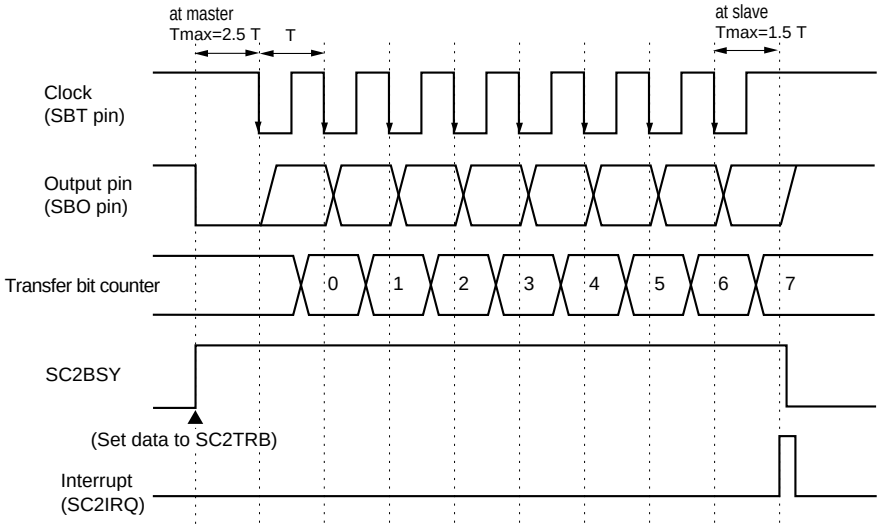


Figure 12-3-2 Transmission Timing (Falling edge, Start condition is enabled)

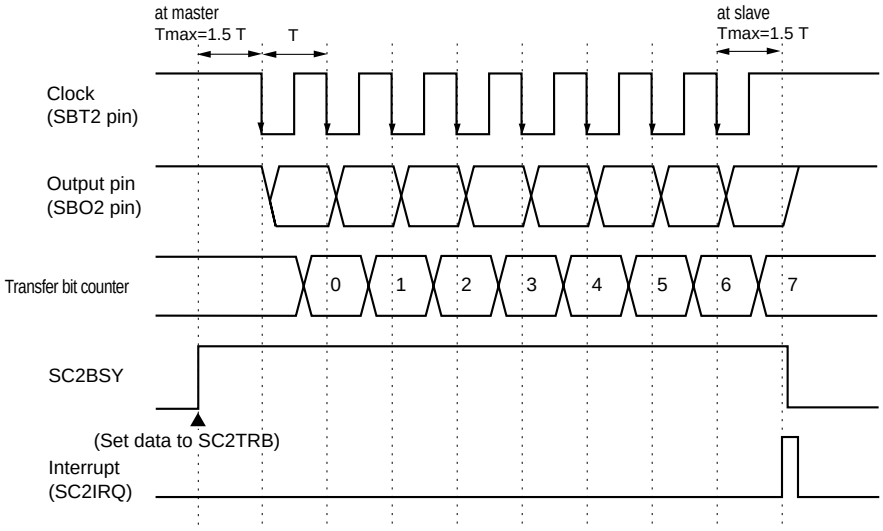


Figure 12-3-3 Reception Timing (Falling edge, Start condition is disabled)

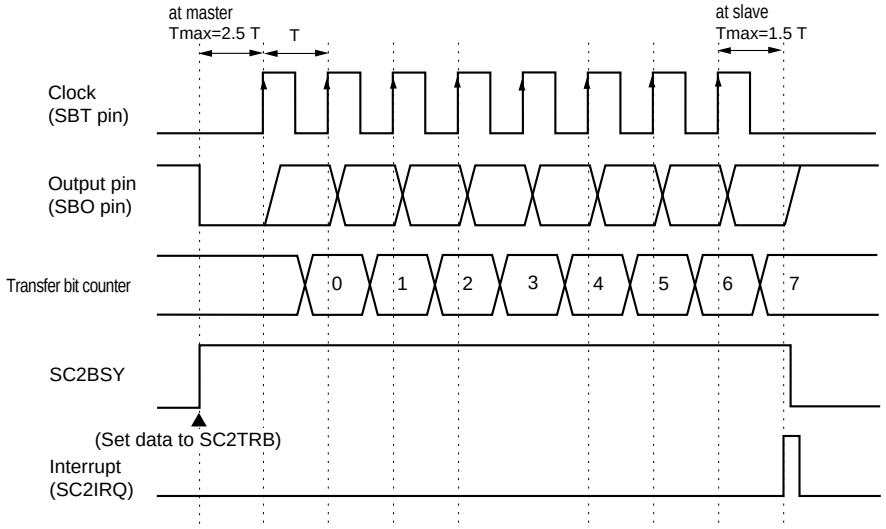


Figure 12-3-4 Transmission Timing (Rising edge, Start condition is enabled)

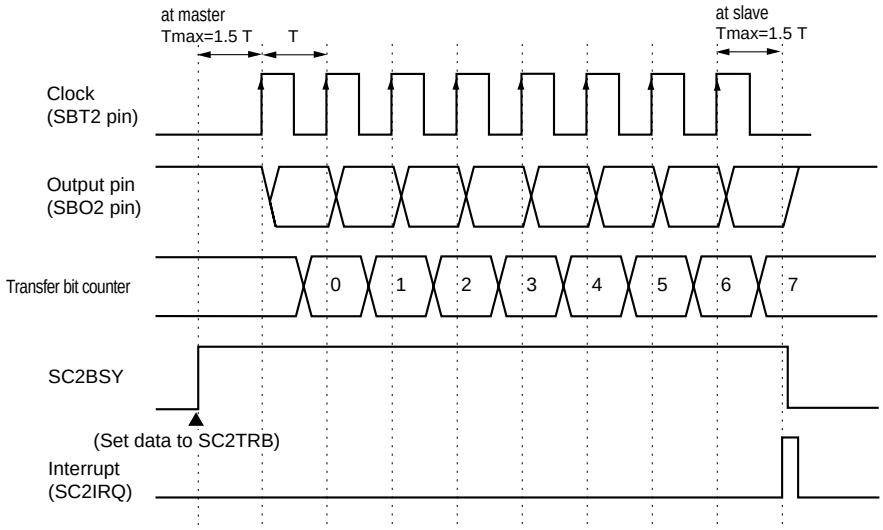


Figure 12-3-5 Transmission Timing (Rising edge, Start condition is disabled)

■Reception Timing

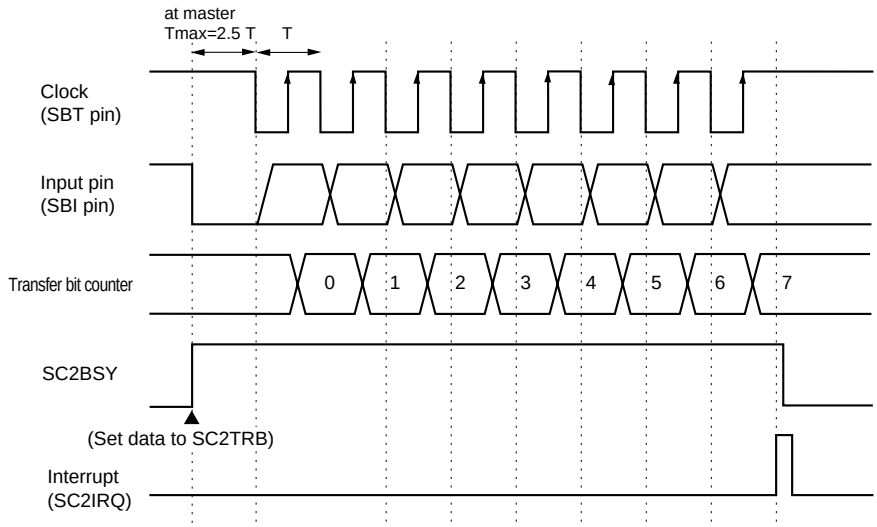


Figure 12-3-6 Reception Timing (Rising edge, Start condition is enabled)

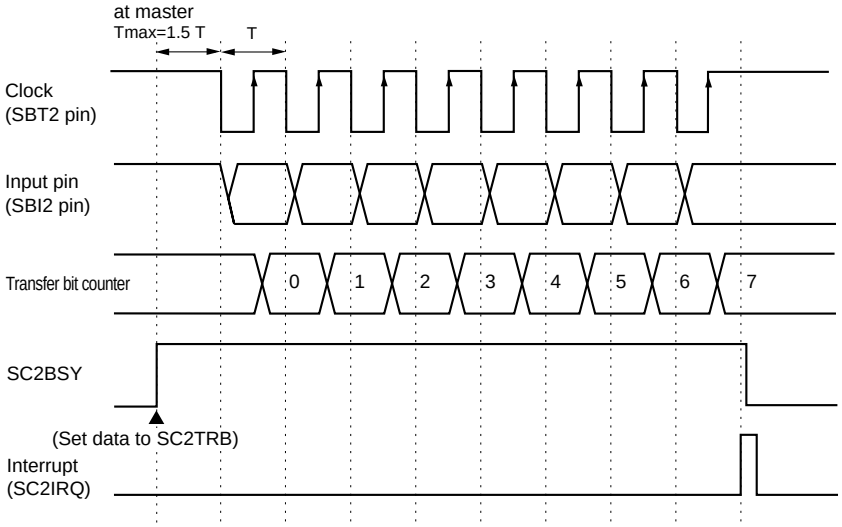


Figure 12-3-7 Reception Timing (Rising edge, Start condition is disabled)

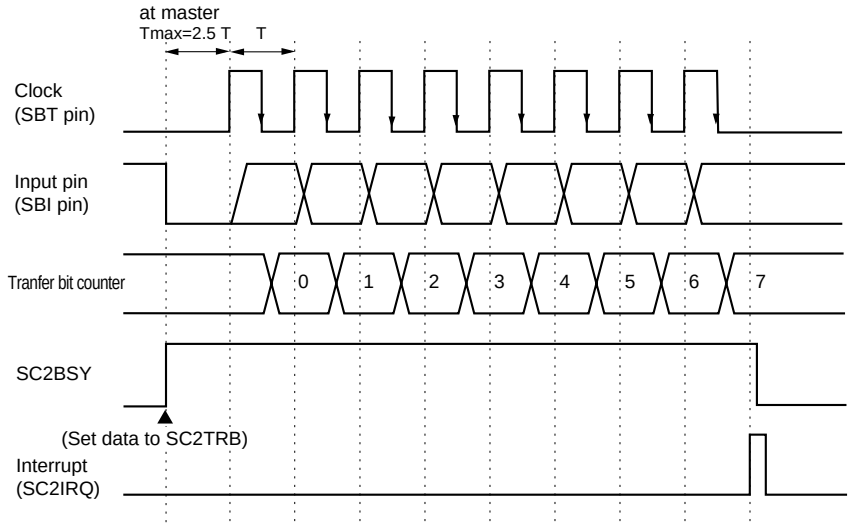


Figure 12-3-8 Reception Timing (Falling edge, Start condition is enabled)

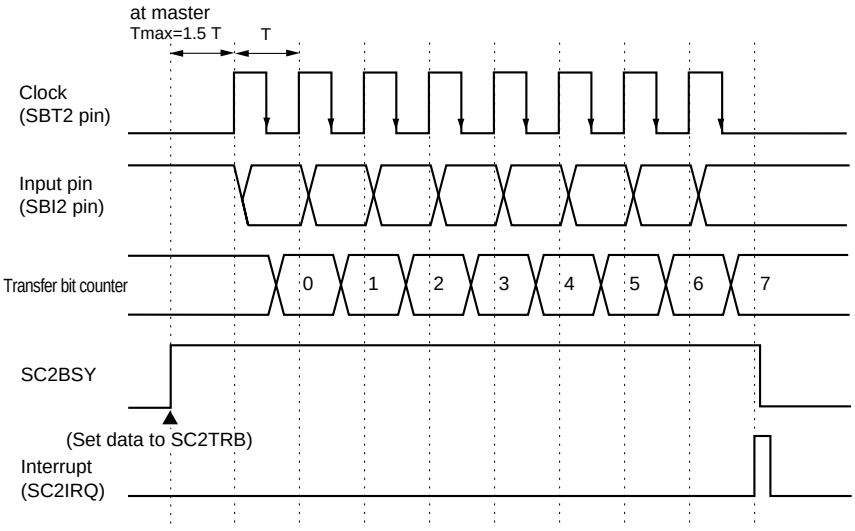


Figure 12-3-9 Reception Timing (Falling edge, Start condition is disabled)

■Transmission / Reception

When transmission and reception are operated at the same time, the reception timing has the opposite timing of the transmission data output edge .

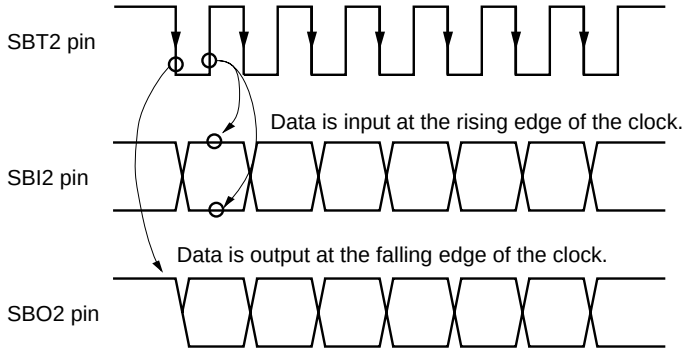


Figure 12-3-10 Transmission / Reception Timing (Reception : Rising edge, Transmission : Falling edge)

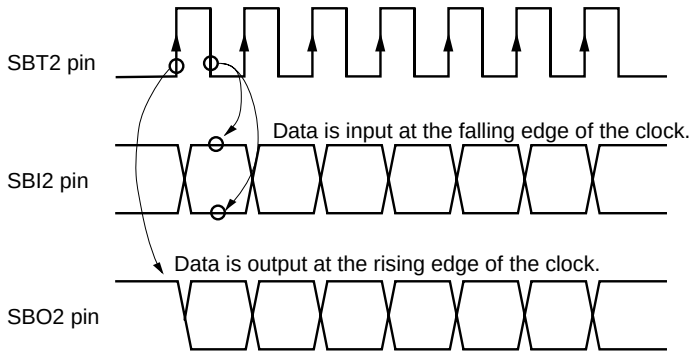


Figure 12-3-11 Transmission / Reception Timing (Reception : Falling edge, Transmission : Rising edge)

■Pins Setup (with 3 channels, at transmission)

Table 12-3-5 shows the pins setup at synchronous serial interface transmission with 3 channels (SBO2 pin, SBI2 pin, SBT2 pin).

Table 12-3-5 Synchronous Serial Interface Pins Setup (with 3 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Internal clock	External clock
Port pin	P03	P04	P05	
SBI2 / SBO2 pin	SBI2/SBO2 independent		-	
	SC2MD1(SC2IOM)			
Function	Serial data output	Input "1"	Serial clock I/O	Serial clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBTS)	
Type	Push-pull / N-ch open-drain	-	Push-pull / N-ch open-drain	Push-pull / N-ch open-drain
	SC2ODC(SC2ODC0)		SC2ODC(SC2ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR3)		P0DIR(P0DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P0PLUD(P0PLUD3)		P0PLUD(P0PLUD5)	

■Pins Setup (with 3 channels, at reception)

Table 12-3-6 shows the pins setup at synchronous serial interface reception with 3 channels (SBO2 pin, SBI2 pin, SBT2 pin).

Table 12-3-6 Synchronous Serial Interface Pins Setup (with 3 channels, at reception)

<table>
<tr><td rowspan="3">Item</td><td>Data output pin</td><td>Data input pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO2 pin</td><td rowspan="2">SBI2 pin</td><td colspan="2">SBT2 pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td>Port pin</td><td>P03</td><td>P04</td><td colspan="2">P05</td></tr>
<tr><td rowspan="2">SBI2 / SBO2 pins</td><td colspan="2">SBI2/SBO2 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC2MD1(SC2IOM)</td></tr>
<tr><td rowspan="2">Function</td><td>Port</td><td>Serial data input</td><td>Serial clock I/O</td><td>Serial clock I/O</td></tr>
<tr><td>SC2MD1(SC2SBOS)</td><td>SC2MD1(SC2SBIS)</td><td colspan="2">SC2MD1(SC2SBTS)</td></tr>
<tr><td rowspan="2">Type</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Push-pull /
N-ch open-drain</td><td>Push-pull /
N-ch open-drain</td></tr>
<tr><td colspan="2">SC2ODC(SC2ODC1)</td></tr>
<tr><td rowspan="2">I/O</td><td rowspan="2">-</td><td>Input mode</td><td>Output mode</td><td>Input mode</td></tr>
<tr><td>P0DIR(P0DIR4)</td><td colspan="2">P0DIR(P0DIR5)</td></tr>
<tr><td rowspan="2">Pull-up</td><td rowspan="2">-</td><td rowspan="2">-</td><td>added / not added</td><td>added / not added</td></tr>
<tr><td colspan="2">P0PLUD(P0PLUD5)</td></tr>
</table>

■Pins Setup (with 3 channels, at reception / transmission)

Table 12-3-7 shows the pins setup at synchronous serial interface transmission/reception with 3 channels (SBO2 pin, SBI2 pin, SBT2 pin).

Table 12-3-7 Synchronous Serial Interface Pins Setup (with 3 channels, at transmission / reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Internal clock	External clock
Port pin	P03	P04	P05	
SBI2 / SBO2 pins	SBI2/SBO2 independent		-	
	SC2MD1(SC2IOM)			
Function	Serial data output	Serial data input	Serial clock I/O	Serial clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBTS)	
Type	Push-pull / N-ch open-drain	-	Push-pull / N-ch open-drain	Push-pull / N-ch open-drain
	SC2ODC(SC2ODC0)		SC2ODC(SC2ODC1)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR(P0DIR3)	P0DIR(P0DIR4)	P0DIR(P0DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P0PLUD(P0PLUD3)		P0PLUD(P0PLUD5)	

■Pins Setup (with 2 channels, at transmission)

Table 12-3-8 shows the pins setup at synchronous serial interface transmission with 2 channels (SBO2 pin, SBT2 pin). The SBI2 pin is not used, so that it can be used as a general port.

Table 12-3-8 Synchronous Serial Interface Pins Setup (with 2 channels, at transmission)

<table>
<tr><td rowspan="3">Item</td><td>Data I/O pin</td><td>Serial unused pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO2 pin</td><td rowspan="2">SBI2 pin</td><td colspan="2">SBT2 pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td>Port pin</td><td>P03</td><td>P04</td><td colspan="2">P05</td></tr>
<tr><td rowspan="2">SBI2 / SBO2 pins</td><td colspan="2">SBI2/SBO2 connection</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC2MD1(SC2IOM)</td></tr>
<tr><td rowspan="2">Function</td><td>Serial data output</td><td>input "1"</td><td>Serial clock I/O</td><td>Serial clock I/O</td></tr>
<tr><td>SC2MD1(SC2SBOS)</td><td>SC2MD1(SC2SBIS)</td><td colspan="2">SC2MD1(SC2SBTS)</td></tr>
<tr><td rowspan="2">Type</td><td>Push-pull /
N-ch open-drain</td><td rowspan="2">-</td><td>Push-pull /
N-ch open-drain</td><td>Push-pull /
N-ch open-drain</td></tr>
<tr><td>SC2ODC(SC2ODC0)</td><td colspan="2">SC2ODC(SC2ODC1)</td></tr>
<tr><td rowspan="2">I/O</td><td>Output mode</td><td rowspan="2">-</td><td>Output mode</td><td>Input mode</td></tr>
<tr><td>P0DIR(P0DIR3)</td><td colspan="2">P0DIR(P0DIR5)</td></tr>
<tr><td rowspan="2">Pull-up</td><td>added / not added</td><td rowspan="2">-</td><td>added / not added</td><td>added / not added</td></tr>
<tr><td>P0PLUD(P0PLUD3)</td><td colspan="2">P0PLUD(P0PLUD5)</td></tr>
</table>

■Pins Setup (with 2 channels, at reception)

Table 12-3-9 shows the pins setup at synchronous serial interface reception with 2 channels (SBO2 pin, SBT2 pin). The SBI2 pin is not used, so that it can be used as a general port.

Table 12-3-9 Synchronous Serial Interface Pins Setup (with 2 channels, at reception)

<table>
<tr><td rowspan="3">Item</td><td>Data I/O pin</td><td>Serial unused pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO2 pin</td><td rowspan="2">SBI2 pin</td><td colspan="2">SBT2 pin</td></tr>
<tr><td>Internal clock</td><td>External clock</td></tr>
<tr><td>Port pin</td><td>P03</td><td>P04</td><td colspan="2">P05</td></tr>
<tr><td rowspan="2">SBI2 / SBO2 pins</td><td colspan="2">SBI2/SBO2 connection</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC2MD1(SC2IOM)</td></tr>
<tr><td rowspan="2">Functions</td><td>Port</td><td>Serial data input</td><td>Serial clock I/O</td><td>Serial clock I/O</td></tr>
<tr><td>SC2MD1(SC2SBOS)</td><td>SC2MD1(SC2SBIS)</td><td colspan="2">SC2MD1(SC2SBTS)</td></tr>
<tr><td rowspan="2">Type</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Push-pull /
N-ch open-drain</td><td>Push-pull /
N-ch open-drain</td></tr>
<tr><td colspan="2">SC2ODC(SC2ODC1)</td></tr>
<tr><td rowspan="2">I/O</td><td>Input mode</td><td rowspan="2">-</td><td>Output mode</td><td>Input mode</td></tr>
<tr><td>P0DIR(P0DIR3)</td><td colspan="2">P0DIR(P0DIR5)</td></tr>
<tr><td rowspan="2">Pull-up</td><td rowspan="2">-</td><td rowspan="2">-</td><td>added / not added</td><td>added / not added</td></tr>
<tr><td colspan="2">P0PLUD(P0PLUD5)</td></tr>
</table>

12-3-2 Setup Example

■Transmission / Reception Setup Example

Here is the setup example at transmission/reception with serial interface 2. Table 12-3-10 shows the conditions.

Table 12-3-10 Conditions for Synchronous Serial Interface at transmission / reception)

Item	set to	Item	set to
SBI2 / SBO2 pins	independent (with 3 channels)	clock	Internal clock
Transfer bit count	8 bits	clock source	fs/2
Start condition	enable	SBT2 / SBO2 pin type	N-ch open-drain
First bit to be transfered	MSB	SBT2 pin pull-up resistance	added
Input edge	at falling	SBO2 pin pull-up resistance	added
Output edge	at rising	Serial 2 interrupt	generate

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select prescaler operation.
(2) Select the clock source. SC2CKS (x'3FA7') bp2-0 : SC2PSC2-0= 100 bp3 = 0	(2) Set the SC2PSC2-0 flag of the SC2CKS register to "100" to select fs/2 at clock source. Set bp3 of the SC2CKS register always to "0".
(3) Control the pin type. SC2ODC (x'3F46') bp1-0 : SC2ODC1-0= 11 P0PLUD (x'3F40') bp5, 3 : P0PLUD5, 3= 1, 1	(3) Set the SC2ODC1-0 flag of the SC2ODC register to "11" to select N-ch open drain for the SBO2/SBT2 pin type. Set the P0PLUD5, 3 flag of the P0PLUD register to "1, 1" to add pull-up/pull-down resistor.
(4) Control the pin direction. P0DIR (X'3F30') bp5-3 : P0DIR5-3 = 101	(4) Set the P0DIR5-3 flag of the port 0 pin control direction register (P0DIR) to "101" to set P05, P03 to output mode, to set P04 to input mode.
(5) Select the transfer bit count. SC2MD0 (x'3FA0') bp2-0 : SC2LNG2-0= 111	(5) Set the SC2LNG2-0 flag of the serial 2 mode register (SC2MD0) to "111" to set the transfer bit count to 8 bits.

Setup Procedure	Description
(6) Select the start condition. SC2MD0 (x'3FA0') bp3 : SC2STE = 1	(6) Set the SC2STE flag of the SC2MD0 register to "1" to enable start condition.
(7) Select the first bit to be transferred. SC2MD0 (x'3FA0') bp4 : SC2DIR = 0	(7) Set the SC2DIR flag of the SC2MD0 register to "0" to set MSB as the first transfer bit.
(8) Select the transfer edge. SC2MD0 (x'3FA0') bp6 : SC2CE1 = 1	(8) Set the SC2CE1 flag of the SC2MD0 register to "1" to set the transmission data output edge to "rising", and the received data input edge to "falling".
(9) Select the transfer clock. SC2MD1 (x'3FA1') bp2 : SC2MST = 1	(9) Set the SC2MST flag of the SC2MD1 register to "1" to select clock master (internal clock).
(10) Control the pin function. SC2MD1 (x'3FA1') bp4 : SC2SBOS = 1 bp5 : SC2SBIS = 1 bp6 : SC2SBTS = 1 bp7 : SC2IOM = 0	(10) Set the SC2SBOS, SC2SBIS, SC2SBTS flags of the SC2MD1 register to "1" to set the SBO2 pin to serial data output, the SBI2 pin to serial data input, and the SBT2 pin to serial clock I/O. Set the SC2IOM flag to "0" to set "serial data input from the SBI2 pin".
(11) Set the interrupt level. SC2ICR (x'3FF8') bp7-6 : SC2LV1-0 = 10	(11) Set the interrupt level by the SCLV1-0 flag of the serial 2 interrupt control register (SC2ICR).
(12) Enable the interrupt. SC2ICR (x'3FF8') bp1 : SC2IE = 1	(12) Enable the interrupt to the SC2IE flag of the SC2ICR register. If the interrupt request flag (SC2IR of the SC2ICR register) is already set, clear SC2IR before the interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(13) Start serial transmission. Transmission data → SC2TRB (x'3FA2')	(13) Set the transmission data to the serial transmission/receiption shift register SC2TRB. The internal clock is generated to start transmisqsion/ reception. After the communication is finished, the serial 2 interrupt SC2IRQ is gener ated.

Note : In the above (5) to (8), each settings can be set at the same time.

If the communication is only for transmission, the data input by setting the SC2SBIS of the SC2MD1 register to "0" should be fixed to "1". The SBI2 pin can be used as a general port.

When only reception is operated, set the SC2SBOS of the SC2MD1 register to "0" to select port. The SBO2 pin can be used as a general port.

When operating communication with 2 channels by connecting the SBO2/SBI2 pins, the SBO2 pin inputs/outputs serial data. The port direction control register P0DIR switches I/O.

This LSI contains emergency communication reset function. When the communication should be stopped by force, set the SC2SBOS and the SC2SBIS of the SC2MD1 register to "0".

Setup for each flag should be done in order of the setup examples. The activation of communication should be operated after all control registers (except table 12-2-1 : SC2TRB) are set.

The rate of the transfer clock set with the SC2CKS register should be under 2.5 MHz.

Chapter 13 A/D Converter

13

13-1 Overview

This LSI has an A/D converter with 10 bits resolution. It contains a built-in sample hold circuit. The channels 0 to 15 (AN0 to AN15) of analog input can be switced by software. When A/D converter is stopped, the power consumption can be reduced by turning the built-in ladder resistance OFF. A/D conversion is activated by a register setup.

13-1-1 Functions

Table 13-1-1 shows the A/D converter functions.

Table 13-1-1 A/D Converter Functions

A/D Input Pins	16 pins
Pins	AN15 to AN0
Interrupt	ADIRQ
Resolution	10 bits
Conversion Time (Min.)	9.6 µs(TAD = as 800 ns)
Input range	V_{ref-} to V_{ref+}
Power Consumption	Built-in Ladder Resistance (ON/OFF)

13-1-2 Block Diagram

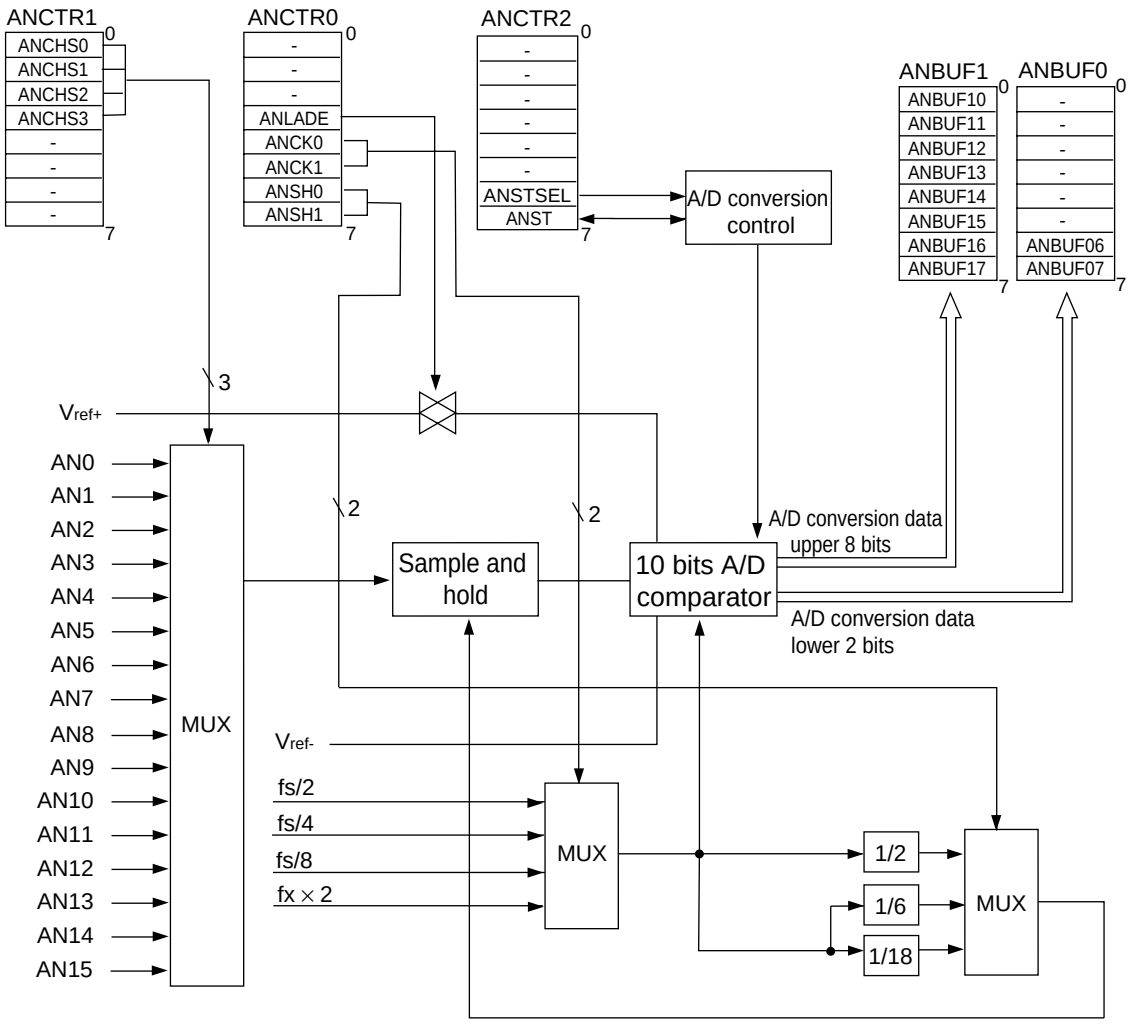


Figure 13-1-1 A/D Converter Block Diagram

13-2 Control Registers

A/D converter consists of the control register (ANCTRn) and the data storage buffer (ANBUFn).

13-2-1 Registers

Table 13-2-1 shows the registers used to control A/D converter.

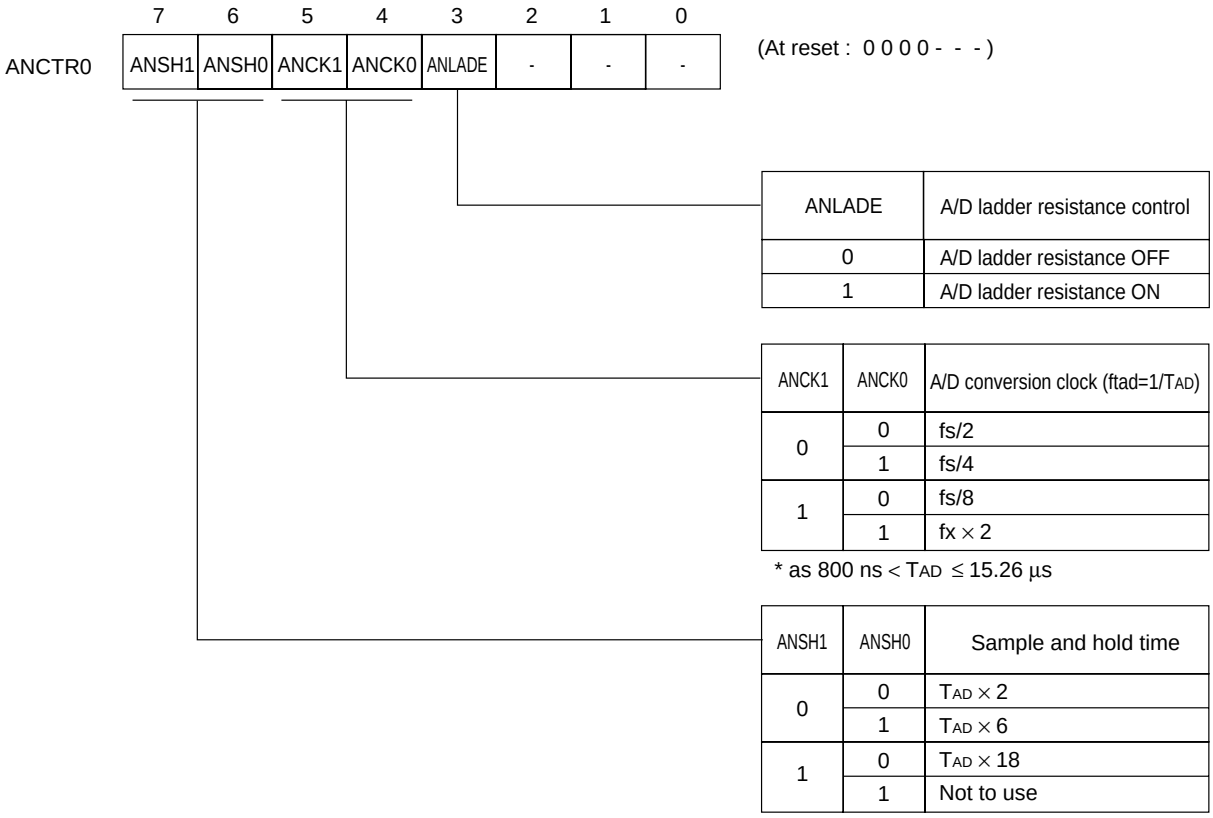
Table 13-2-1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ANCTR0	x'03FB0'	R/W	A/D converter control register 0	XIII - 5
ANCTR1	x'03FB1'	R/W	A/D converter control register 1	XIII - 6
ANCTR2	x'03FB2'	R/W	A/D converter control register 2	XIII - 6
ANBUF0	x'03FB3'	R	A/D converter data storage buffer 0	XIII - 7
ANBUF1	x'03FB4'	R	A/D converter data storage buffer 1	XIII - 7
ADICR	x'03FFA'	R/W	A/D converter interrupt control register	III - 39
PAIMD	x'03F3A'	R/W	Port A input mode register	IV - 58
PAPLUD	x'03F4A'	R/W	Port A pull-up/pull-down resistor control register	IV - 58
PBIMD	x'03F3D'	R/W	Port B input mode register	IV - 62
PBPLU	x'03F4B'	R/W	Port B pull-up/pull-down resistor control register	IV - 62

R/W : Readable/Writable
R : Readable only

13-2-2 Control Registers

■A/D Converter Control Register 0 (ANCTR0)



ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF
1	A/D ladder resistance ON

ANCK1	ANCK0	A/D conversion clock (ftad=1/TAD)
0	0	fs/2
	1	fs/4
1	0	fs/8
	1	fx × 2

* as 800 ns < TAD ≤ 15.26 µs

ANSH1	ANSH0	Sample and hold time
0	0	TAD × 2
	1	TAD × 6
1	0	TAD × 18
	1	Not to use

Figure 13-2-1 A/D Control Register 0 (ANCTR0 : x'03FB0', R/W)

■A/D Converter Control Register 1 (ANCTR1)

	7	6	5	4	3	2	1	0
ANCTR1	-	-	-	-	ANCHS3	ANCHS2	ANCHS1	ANCHS0

(At reset : - - - - 0 0 0 0)

ANCHS3	ANCHS2	ANCHS1	ANCHS0	Analog Input Channel
0	0	0	0	AN0 (PA0)
			1	AN1 (PA1)
		1	0	AN2 (PA2)
			1	AN3 (PA3)
	1	0	0	AN4 (PA4)
			1	AN5 (PA5)
		1	0	AN6 (PA6)
			1	AN7 (PA7)
1	0	0	0	AN8 (PB0)
			1	AN9 (PB1)
		1	0	AN10(PB2)
			1	AN11(PB3)
	1	0	0	AN12(PB4)
			1	AN13(PB5)
		1	0	AN14(PB6)
			1	AN15(PB7)

Figure 13-2-2 A/D Converter Control Register 1 (ANCTR1 : x'03FB1', R/W)

■A/D Converter Control Register 2 (ANCTR2)

	7	6	5	4	3	2	1	0
ANCTR2	ANST	Reserved	-	-	-	-	-	-

(At reset : 0 0 - - - - - -)

Reserved	Set always to "0".

ANST	A/D conversion status
0	Finish, Hold
1	Start, Converting

Figure 13-2-3 A/D Converter Control Register 2 (ANCTR2 : x'03FB2', R/W)

13-2-3 Data Buffers

■A/D Conversion Data Storage Buffer 0 (ANBUF0)

The lower 2 bits results from A/D conversion are stored to this register.

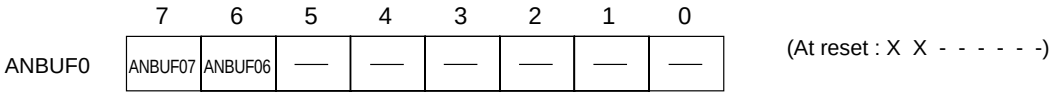


Figure 13-2-4 A/D Conversion Data Buffer 0 (ANBUF0 : x'03FB3', R)

■A/D Conversion Data Storage Buffer 1 (ANBUF1)

The upper 8 bits results from A/D conversion are stored to this register.

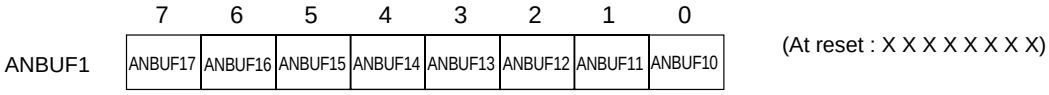


Figure 13-2-5 A/D Conversion Data Buffer 1 (ANBUF1 : x'03FB4', R)

13-3 Operation

Here is a description of A/D converter circuit setup procedure.

(1) Set the analog pins.
Set the analog input pin, set in (2), to "special function pin" by the port A input mode register (PAIMD) and the port B input mode register (PBIMD).
* Setup of the port A,B input mode register should be done before analog voltage is put to pins.

(2) Select the analog input pin.
Select the analog input pin from AN15 to AN0 (PB7 to PB0 and PA7 to PA0) by the ANCHS3 to ANCHS0 flag of the A/D converter control register 1 (ANCTR1).

(3) Select the A/D converter clock.
Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
Setup should be such a way that converter clock (TAD) does not drop less than 800 ns with any resonator.

(4) Set the sample hold time.
Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0). The sample hold time should be based on analog input impedance.

(5) Set the A/D ladder resistance.
Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1", and a current flow through the ladder resistance and A/D converter goes into the waiting.
* (2) to (5) are not in order. (3), (4) and (5) can be operated simultaneously.

(6) Select the A/D converter activation factor, then start A/D conversion.
Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start A/D converter.

(7) A/D conversion
After sampling with the sample and hold time, set in (3), A/D conversion is decided in comparison with MSB, in order.

(8) Complete the A/D conversion.
When A/D conversion is finished, the ANST flag is cleared to "0", and the result of the conversion is stored to the A/D buffer (ANBUF0, 1). At the same time, the A/D complete interrupt request (ADIRQ) is generated.

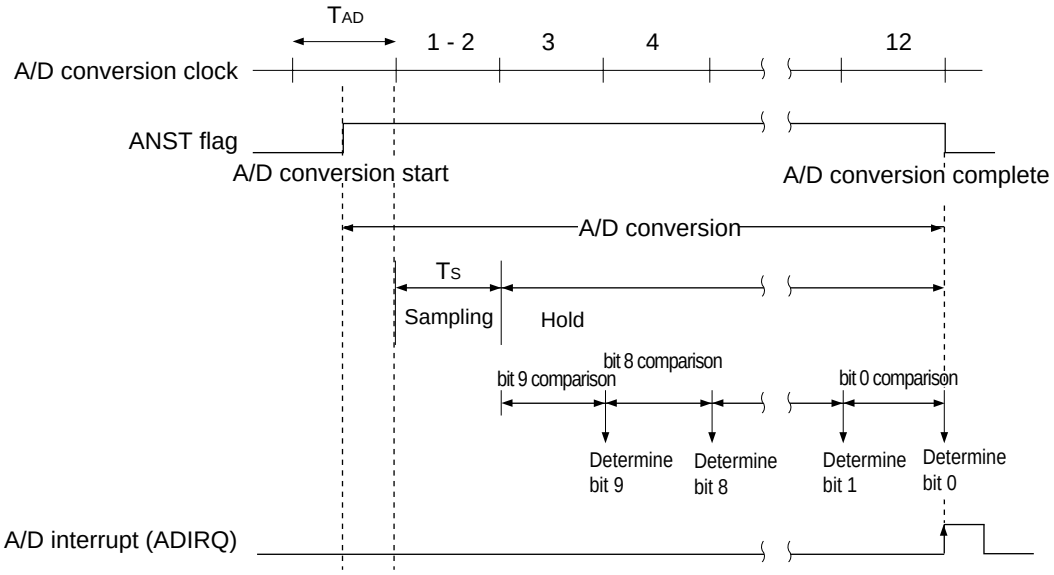


Figure 13-3-1 Operation of A/D Conversion

To read out the value of the A/D conversion, A/D conversion should be done several times to prevent noise error by confirming the match of level by program, or by using the average value.

There is no problem for reference voltage V_{ref+} to be below V_{DD}. However, there should be difference more than 2 V between V_{ref+} and V_{ref-}.

13-3-1 Setup

■Input Pins of A/D Converter Setup

Input pins for A/D converter is selected by the ANCH3 to 0 flag of the ANCTR1 register.

Table 13-3-1 Input Pins of A/D Converter Setup

ANCHS3	ANCHS2	ANCHS1	ANCHS0	A/D pin
0	0	0	0	AN0 pin
			1	AN1 pin
		1	0	AN2 pin
			1	AN3 pin
	1	0	0	AN4 pin
			1	AN5 pin
		1	0	AN6 pin
			1	AN7 pin
1	0	0	0	AN8 pin
			1	AN9 pin
		1	0	AN10 pin
			1	AN11 pin
	1	0	0	AN12 pin
			1	AN13 pin
		1	0	AN14 pin
			1	AN15 pin

■A/D Converter Clock Setup

The A/D converter clock is set with the ANCK1 to 0 flag of the ANCTR0 register. Set the A/D converter clock (T_{AD}) more than 800 ns and less than 15.26 µs. Table 13-3-2 shows the machine clock (fosc, fx, fs) and the A/D converter clock (T_{AD}). (calculated as fs = fosc/2, fx/4)

Table 13-3-2 A/D Conversion Clock and A/D Conversion Cycle

ANCK1	ANCK0	A/D conversion clock	A/D conversion cycle (T_{AD})		
			at high speed oscillation		at low speed oscillation
			at fosc=20 MHz	at fosc=8.38 MHz	at fx=32.768 kHz
0	0	fs/2	200.00 ns (unusable)	477.33 ns (unusable)	244.14 µs (unusable)
	1	fs/4	400.00ns (unusable)	954.65ns	488.28 µs (unusable)
1	0	fs/8	800.00 ns	1.91 µs	976.56 µs (unusable)
	1	fx x 2	15.26 µs	15.26 µs	15.26 µs

For the system clock (fs), refer to Chapter 2. 2-5 Clock Switching.

■A/D Converter Sampling Time (Ts) Setup

The sampling time of A/D converter is set with the ANSH1 to 0 flag of the ANCTR0 register. The sampling time of A/D converter depends on external circuit, so set the right value by analog input impedance.

Table 13-3-3 Sampling Time of A/D Conversion and A/D Conversion Time

ANSH1	ANSH0	Sampling time (Ts)	A/D conversion time			
			at TAD=800 ns	at TAD=954.65 ns	at TAD=1.91 µs	at TAD=15.26 µs
0	0	TAD x 2	9.60 µs	11.46 µs	22.92 µs	183.12 µs
	1	TAD x 6	12.80 µs	15.27 µs	30.56 µs	244.16 µs
1	0	TAD x 18	22.40 µs	26.73 µs	53.48 µs	427.28 µs
	1	Reserved	-	-	-	-

■Built-in Ladder Resistor Control

The ANLADE flag of the ANCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. When A/D converter is stopped, the ANLADE flag of the ANCTR0 register is set to "0" to save the power consumption.

Table 13-3-4 A/D Ladder Resistor Control

ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF (A/D conversion stopped)
1	A/D ladder resistance ON (A/D conversion operated)

■A/D Conversion Starting Setup

A/D conversion starting is set with the ANST flag of the ANCTR2 register. The ANST flag of the ANCTR2 register is set to "1" to start A/D conversion. Also, the ANST flag of the ANCTR2 register is set to "1" during A/D conversion, then cleared to "0" as the A/D conversion complete interrupt is generated.

Table 13-3-5 A/D Conversion Starting

ANST	A/D conversion activation factor
1	A/D conversion started or in progress.
0	A/D conversion completed or stopped

13-3-2 Setup Example

■Example of A/D Converter Setup by Registers

A/D conversion is started by setting registers. The analog input pins are set to AN0, the converter clock is set to fs/4, and the sampling hold time is set to TAD x 6. Then, A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD (x'3F3A') bp0 : PAIMD0 = 1 PAPLUD (x'3F4A') bp0 : PAPLUD0 = 0	(1) Set the analog input pin, set in (2), as the special function pin with the port A input mode register (PAIMD). Also, set no pull-up/pull-down resistance with the port A pull-up/pull-down resistance control register (PAPLUD).
(2) Select the analog input pin. ANCTR1 (x'3FB1') bp3-0 : ANCHS3-0 = 000	(2) Select the analog input pin from AN15-0 (PB7-0, PA7-0) by the ANCHS3-0 flag of the A/D converter control register 1 (ANCTR1).
(3) Select the A/D converter clock. ANCTR0 (x'3FB0') bp5-4 : ANCK1-0 = 01	(3) Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
(4) Set the sample and hold time. ANCTR0 (x'3FB0') bp7-6 : ANSH1-0 = 01	(4) Set the sample and hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0).
(5) Set the interrupt level. ADICR (x'3FFA') bp7-6 : ADLV1-0 = 00	(5) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag is already set, clear it. [☞ Chapter 3. 3-1-4 Interrupt Flag Setting]
(6) Enable the interrupt. ADICR (x'3FFA') bp1 : ADIE = 1	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1".
(7) Set the A/D ladder resistance. ANCTR0 (x'3FB0') bp3 : ANLADE = 1	(7) Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.

Setup Procedure	Description
(8) Start the A/D conversion operation. ANCTR2 (x'3FB2') bp7 : ANST = 1	(8) Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start the A/D conversion.
(9) Complete the A/D conversion. ANBUF0 (x'3FB3') ANBUF1 (x'3FB4')	(9) When the A/D conversion is finished, the A/D conversion complete interrupt is generated and the ANST flag of the A/D converter control register 2 (ANCTR2) is cleared to "0". The result of the conversion is stored to the A/D converter buffer (ANBUF0, 1).

Note : The above (3) to (4) can be set at the same time.

13-3-3 Cautions

A/D conversion can be damaged by noise easily, therefore, anti-noise measures should be taken adequately .

■Anti-noise measures

To A/D input (analog input pin), add condenser near the V_{SS} pins of micro controller.

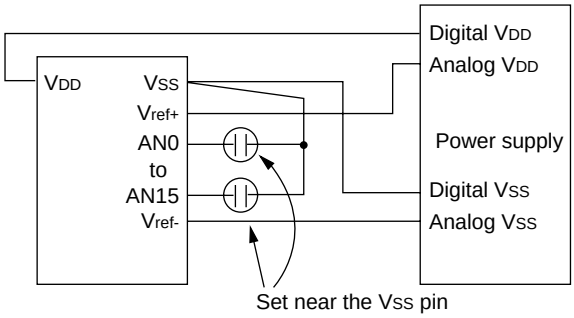


Figure 13-3-2 A/D Converter Recommended Example 1

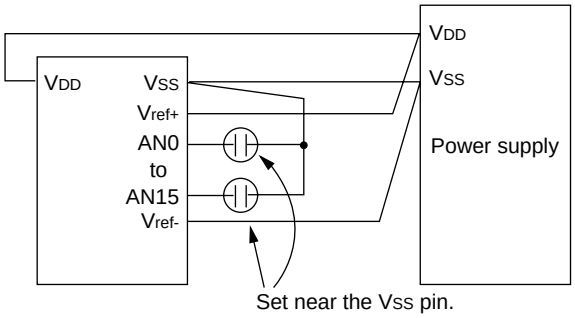
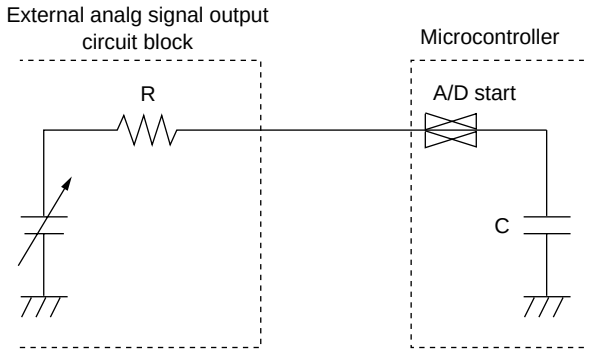


Figure 13-3-3 A/D Converter Recommended Example 2

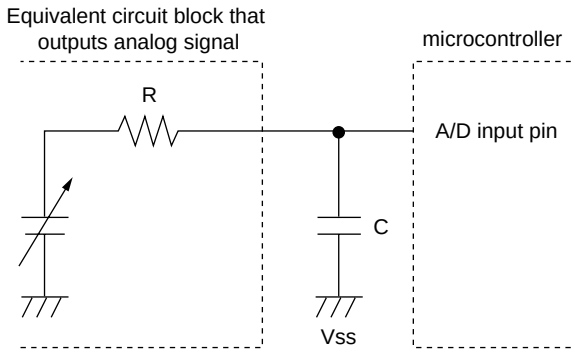
This microcontroller contains a sample hold capacitor (C) (app. 10 pF).
Set the sample hold time based on the capacitor (C) and the time constant of impedance R of the external analg signal output circuit.
For the sample hold time, 3 x the time constant CR or longer is recomended.
At A/D conversion cycle(T_{AD})=800 ns, 1.6 µs, 4.8 µs,and 14.4 µs can be selected as a sample hold time. Each impedance value of the external analog signal output circuit should be under the following values.

Sample hold time (At T_{AD}=800 ns)	Impedance of analog signal output circuit
T_{AD} x 2 = 1.6 µs	R < 1.6 µs / 10 pF / 3 = 53 kΩ
T_{AD} x 6 = 4.8 µs	R < 4.8 µs / 10 pF / 3 = 160 kΩ
T_{AD} x 18 = 14.4 µs	R < 14.4 µs / 10 pF / 3 = 480 kΩ



To maintain high precision of A/D conversion, following instructions on use of A/D converter should be strictly kept.

1. Input impedance R of A/D input pin should be under 500 kΩ*1. And connect the external capacitor C (over 1000 pF, under 1 µF)*1 between Vss and the A/D input pin.
2. Set the A/D conversion frequency depending on the time constant of R and C.
3. Changing the output level of the microcontroller or switching ON/OFF of the peripheral added circuit while the A/D conversion is in progress may lower the precision of A/D conversion, for these may fluctuate the values of the analog input pin and the power pin. Check the waveform of the analog input pin before the system evaluation.



*1 : That value is for reference.

Chapter 14 LCD

14

14-1 Functions

This LSI contains an internal LCD driver circuit with 47 segment pins and 4 common pins. The LCD driver circuit consists of a segment output latch, LCD control registers, a prescaler, a timing control circuit, a multiplexer, segment drivers, common drivers, a LCD voltage control circuit and voltage divider resistors.

14-1-1 Functions

Table 14-1-1 shows the functions of the LCD driver circuits.

Table 14-1-1 LCD Functions

	LCD
Duty	Static 1/2 Duty 1/3 Duty 1/4 Duty
Segment Output Pins	SEG0 to SEG46
Common Output Pins	COM0 to COM3
LCD Power Supply	V_{LC1} to V_{LC3}
Clock Source (LCDCLK)	$fosc/2^{11}$ $fosc/2^{12}$ $fosc/2^{13}$ $fosc/2^{14}$ $fosc/2^{15}$ $fosc/2^{16}$ $fosc/2^{17}$ $fosc/2^{18}$ $fx/2^{6}$ $fx/2^{7}$ $fx/2^{8}$ $fx/2^{9}$
fosc: Machine clock (High speed oscillation) fx: Machine clock (Low speed oscillation) LCDCLK: LCD clock source (selected with LCDCK0 to LCDCK3)	

When LCD function is unused, V_{LC1}, V_{LC2}, V_{LC3}, C1 and C2 pins should be fixed to V_{DD} level.

Use the LCD panel driver voltage V_{LCD} at $V_{DD} \leq V_{LCD} \leq 5.5$ V.

14-1-2 LCD Operation in Standby Mode

Certain LCD driver operation could be limited in standby mode.
Table 14-1-2 shows the LCD operation capabilities in standby mode.

Table 14-1-2 LCD Operation in Standby Mode

CPU Mode		LCD Clock	
		fosc	fx
Operation Mode	NORMAL	O	O
	SLOW	×	O
Standby Mode	HALT0	Δ	Δ
	HALT1	×	Δ
	STOP	×	×

O : LCD Operation is available
Δ : Holding Display is available
× : LCD Operation is not available.

For transition to CPU mode in which LCD operation is not available, turn the LCD off and switch segment output to port in advance.

14-1-3 Maximum Pixels

Table 14-1-3 shows the maximum pixels.

Table 14-1-3 Maximum Pixels

Duty	Maximum Pixels (Segment × Common)	8-segment LCD Panel	Common Pins	Segment Output Latch bits
Static	47(47 × 1)	5 rows	COM0	bit0, bit4
1/2	94(47 × 2)	11 rows	COM0 to COM1	bit0 to bit1, bit4 to bit5
1/3	141(47 × 3)	17 rows	COM0 to COM2	bit0 to bit2, bit4 to bit6
1/4	188(47 × 4)	23 rows	COM0 to COM3	bit0 to bit3, bit4 to bit7

14-1-4 Switching I/O ports and LCD segment pins

Switching of port output and segment output is controlled with the LCD output control register 1, 2, 3, 4 (LCCTR1, LCCTR2, LCCTR3, LCCTR4). [☞ Chapter 14-2 LCD Control Registers]
Switching of normal port and LCD common pin is controlled with the LCD mode control register 1 (LCCTR1). [☞ Chapter 14-2 LCD Control Registers]

Port 8 (SEG0 to 7) is switchable to I/O ports in 8-bit unit.
Port B(SEG39 to 46) is switchable to I/O ports in 1-bit unit.
Port 33 to 30 (SEG35 to 38) are switchable to I/O ports in 2-bit unit.
Port 34 (SEG34) is switchable to I/O ports in 1-bit unit.
Port 36, 35 (SEG8 to 9) are switchable to I/O ports in 2-bit unit.
Port 4, 6, 7 (SEG10 to 33) are switchable to I/O ports in 2-bit unit.
Port 9 (COM0 to 3) are switchable to I/O ports in 1-bit unit.

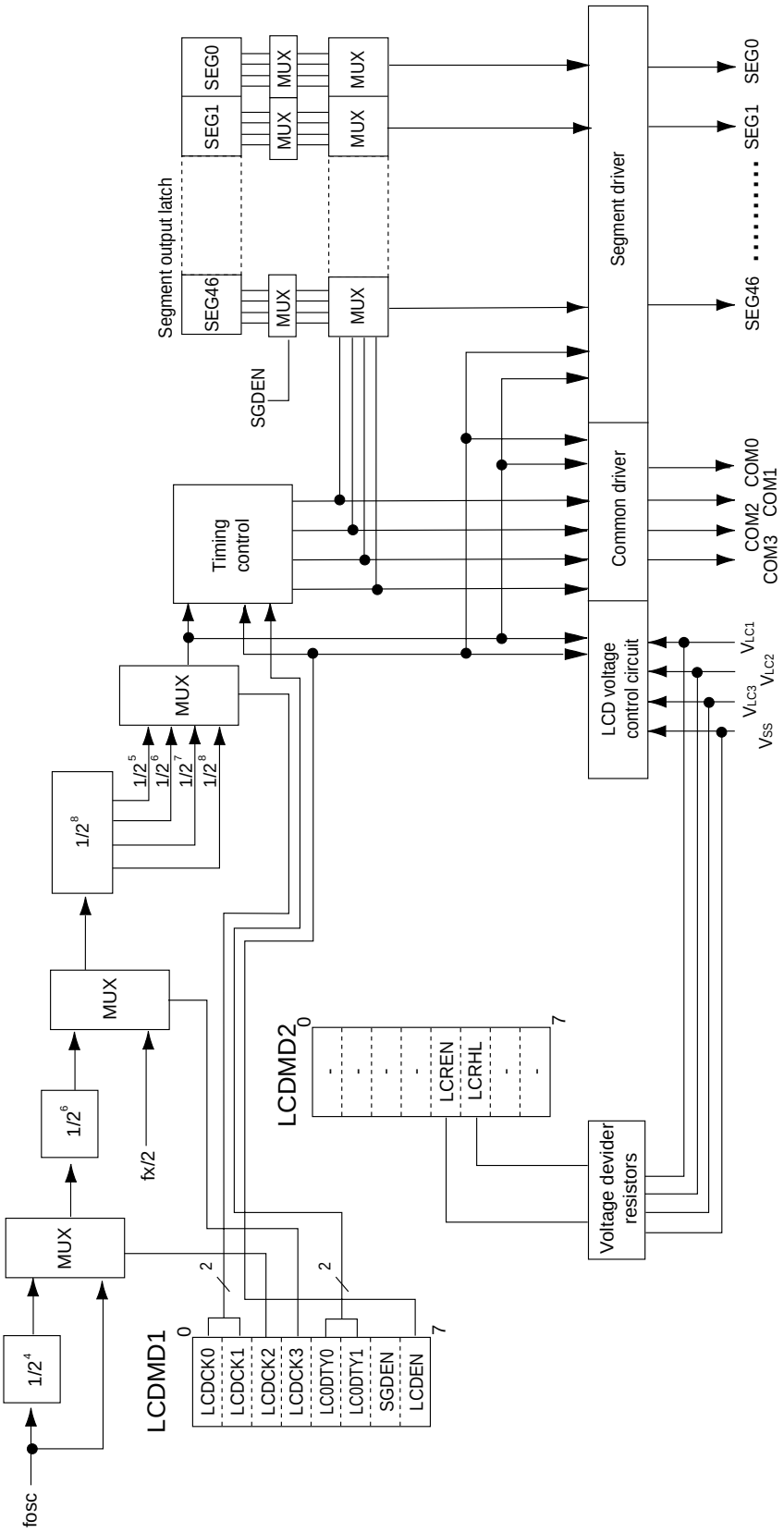


Figure 14-1-1 LCD Driver Circuit Block Diagram

14-2 Control Registers

The LCD is controlled by LCD mode control register 1 (LCDMD1), LCD mode control register 2 (LCDMD2), LCD output control register 1 (LCCTR1), LCD output control register 2 (LCCTR2), LCD output control register 3 (LCCTR3) and LCD output control register 4 (LCCTR4). The LCD display data is stored in the segment output latch.

14-2-1 Registers

Table 14-2-1 shows the LCD control registers.

Tabel 14-2-1 LCD Control Registers List

Registers	Address	R/W	Function	Page
LCDMD1	X'03FD9'	R/W	LCD mode control register 1	XIV - 7
LCDMD2	X'03FDA'	R/W	LCD mode control register 2	IV - 23, XIV - 8
LCCTR1	X'03FDB'	R/W	LCD output control register 1	IV - 23, 51, 55 XIV - 9
LCCTR2	X'03FDC'	R/W	LCD output control register 2	IV - 42, 46 XIV - 10
LCCTR3	X'03FDD'	R/W	LCD output control register 3	IV - 24, 32 XIV - 11
LCCTR4	X'03FDE'	R/W	LCD output control register 4	IV - 63 XIV - 12

R/W: Readable/Writable

* Address x'02E00' to x'02E17' are assigned to the segment output latch.
[☞ Chapter 14 14-2-8 Segment Output Latch]

14-2-2 Mode Control Register 1 (LCDMD1)

The LCD mode control register 1 (LCDMD1) is a 8-bit register that controls the LCD clock, LCD display ON/OFF and the display duty. The address assigned to this register is X'3FD9'. The value of the LCDMD1 register is initialized at reset.

	7	6	5	4	3	2	1	0	
LCDMD1	LCDEN	LCREN	LCDTY1	LCDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	(At reset: 0 0 0 0 0 0 0 0)

LCDCK3	LCDCK2	LCDCK1	LCDCK0	LCD clock source selection
0	0	0	0	$OSC1/2^{11}$
			1	$OSC1/2^{12}$
		1	0	$OSC1/2^{13}$
			1	$OSC1/2^{14}$
	1	0	0	$OSC1/2^{15}$
			1	$OSC1/2^{16}$
		1	0	$OSC1/2^{17}$
			1	$OSC1/2^{18}$
1	X	0	0	$XI/2^{6}$
			1	$XI/2^{7}$
		1	0	$XI/2^{8}$
			1	$XI/2^{9}$

LCDTY1	LCDTY0	LCD display duty selection
0	0	1/4 duty
	1	1/3 duty
1	0	1/2 duty
	1	Static

SGDEN	LCD display enable
0	enable
1	disable

LCDEN	LCD driver circuit start flag
0	Stop
1	Start

Figure 14-2-1 Mode Control Register1 (LCDMD1: X'3FD9', R/W)

14-2-3 Mode Control Register2 (LCDMD2)

The LCD mode control register 2 (LCDMD2) is a 7-bit register that controls ON/OFF and type selection of internal voltage divider registor. The address assigned to this register is x'3FDA'. The value of the LCDMD2 register is initialized at reset.

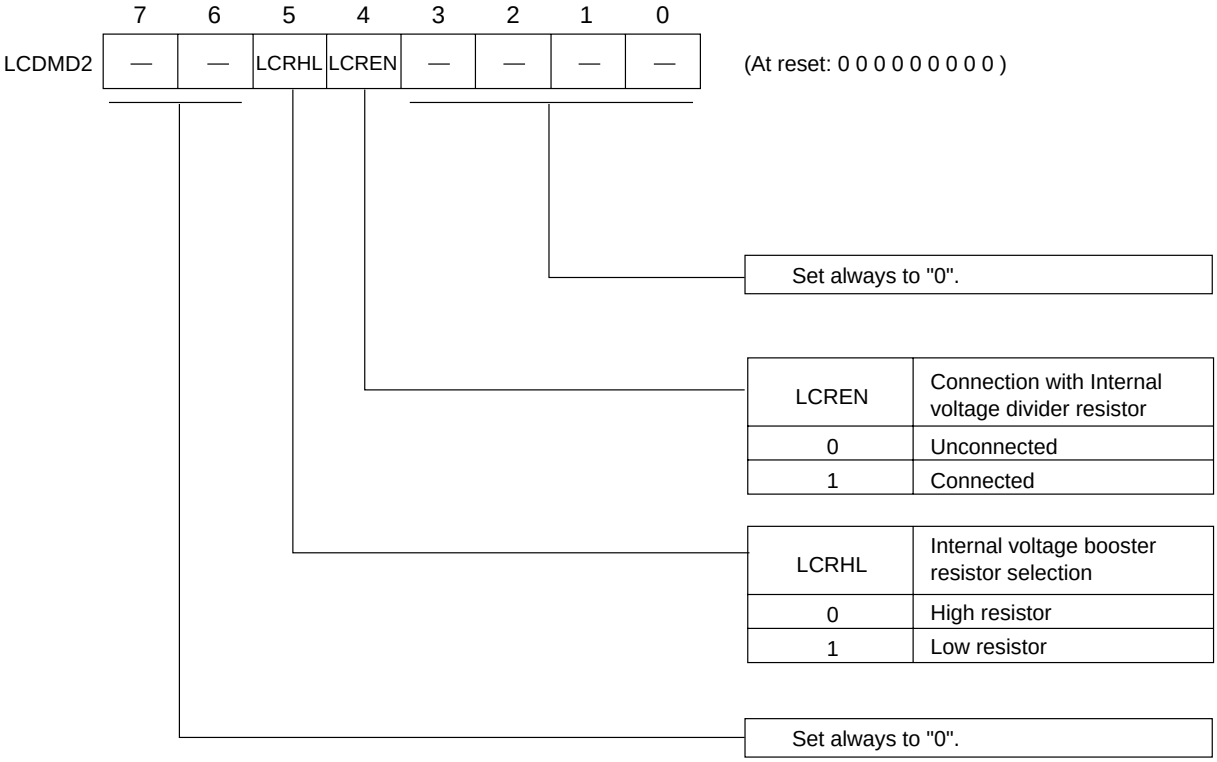


Figure 14-2-2 Mode Control Register 2 (LCDMD2: X'3FDA', R/W)

When internal voltage divider resistor is used, V_{LC1}, V_{LC2} and V_{LC3} voltage level might be dropped depending on used LCD panel, and that might lower the LCD display luminance. In this case, use the external voltage divider resistor.

14-2-4 Output Control Register 1 (LCCTR1)

The LCD output control register 1 (LCCTR1) switches port output (P35,P36,P8) and segment output (SEG8 to 9, SEG0 to SEG7), and switches port output (P9) and common output (COM0 to 3). The address assigned to this register is x'3FDB'. At reset, LCCTR1 is set to the input port values.

	7	6	5	4	3	2	1	0	
LCCTR1	-	-	COMSL3	COMSL2	COMSL1	COMSL0	LC1SL1	LC1SL0	(At reset: - - 0 0 0 0 0 0)

LC1SL0	SEG8-9/ Port (P36-35) selection
0	Port (P36-35) selection
1	SEG8-9 selection

LC1SL1	SEG0-7/Port (P80-87) selection
0	Port (P80-87) selection
1	SEG0-7 selection

COMSL0	COM0/Port(P90) selection
0	Port (P90) selection
1	COM0 selection

COMSL1	COM1/Port (P91) selection
0	Port (P91) selection
1	COM1 selection

COMSL2	COM2/Port (P92) selection
0	Port (P92) selection
1	COM2 selection

COMSL3	COM3/Port (P93) selection
0	Port(P93) selection
1	COM3 selection

Figure 14-2-3 Output Control Register 1 (LCCTR1: X'3FDB', R/W)

14-2-5 Output Control Register 2 (LCCTR2)

The LCD output control register 2 (LCCTR2) switches port output (P6, P7) and segment output (SEG10 to SEG25). The address assigned to this register is x'3FDC'. At reset, LCCTR2 is set to the input port values.

	7	6	5	4	3	2	1	0	
LCCTR2	LC2SL7	LC2SL6	LC2SL5	LC2SL4	LC2SL3	LC2SL2	LC2SL1	LC2SL0	(At reset: 0 0 0 0 0 0 0 0)

LC2SL0	SEG24-25 / Port (P61-60) selection
0	Port (P61-60) selection
1	SEG24-25 selection

LC2SL1	SEG22-23 / Port (P63-62) selection
0	Port (P63-62)
1	SEG22-23

LC2SL2	SEG20-21 / Port (P65-64) selection
0	Port (P65-64)
1	SEG20-21

LC2SL3	SEG18-19 / Port (P67-66) selection
0	Port (P67-66)
1	SEG18-19

LC2SL4	SEG16-17 / Port (P71-70) selection
0	Port (P71-70)
1	SEG16-17

LC2SL5	SEG14-15 / Port (P73-72) selection
0	Port (P73-72)
1	SEG14-15

LC2SL6	SEG12-13 / Port (P75-74) selection
0	Port (P75-74)
1	SEG12-13

LC2SL7	SEG10-11 / Port (P77-76) selection
0	Port (P77-76)
1	SEG10-11

Figure 14-2-4 Output Control Register 2 (LCCTR2: X'3FDC', R/W)

14-2-6 Output Control Register 3 (LCCTR3)

The LCD output control register 3 (LCCTR3) switches port output (P4, P30 to P34) and segment output (SEG26 to SEG38). The address assigned to this register is x'3FDD'. At reset, LCCTR3 is set to the input port values.

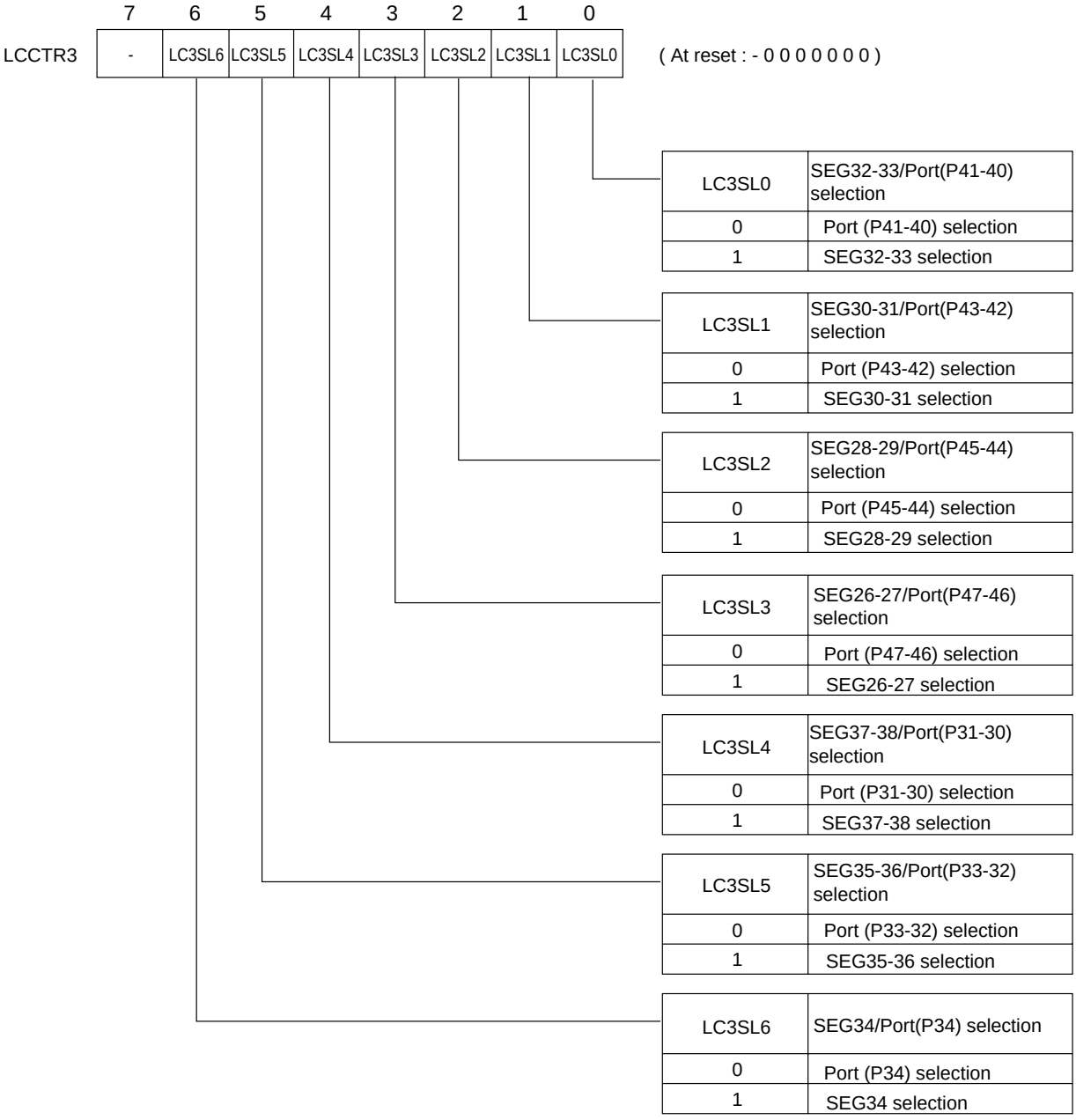

7 6 5 4 3 2 1 0
LCCTR3
- LC3SL6 LC3SL5 LC3SL4 LC3SL3 LC3SL2 LC3SL1 LC3SL0
(At reset : - 0 0 0 0 0 0 0)
LC3SL0 SEG32-33/Port(P41-40) selection
0 Port (P41-40) selection
1 SEG32-33 selection
LC3SL1 SEG30-31/Port(P43-42) selection
0 Port (P43-42) selection
1 SEG30-31 selection
LC3SL2 SEG28-29/Port(P45-44) selection
0 Port (P45-44) selection
1 SEG28-29 selection
LC3SL3 SEG26-27/Port(P47-46) selection
0 Port (P47-46) selection
1 SEG26-27 selection
LC3SL4 SEG37-38/Port(P31-30) selection
0 Port (P31-30) selection
1 SEG37-38 selection
LC3SL5 SEG35-36/Port(P33-32) selection
0 Port (P33-32) selection
1 SEG35-36 selection
LC3SL6 SEG34/Port(P34) selection
0 Port (P34) selection
1 SEG34 selection

Figure 14-2-5 Output Control Register 3 (LCCTR3: X'3FDD', R/W)

14-2-7 Output Control Register 4 (LCCTR4)

The LCD output control register 4 (LCCTR4) switches port output (PB) and segment output (SEG39 to SEG46). The address assigned to this register is x'3FDE'. At reset, LCCTR4 is set to the input port values.

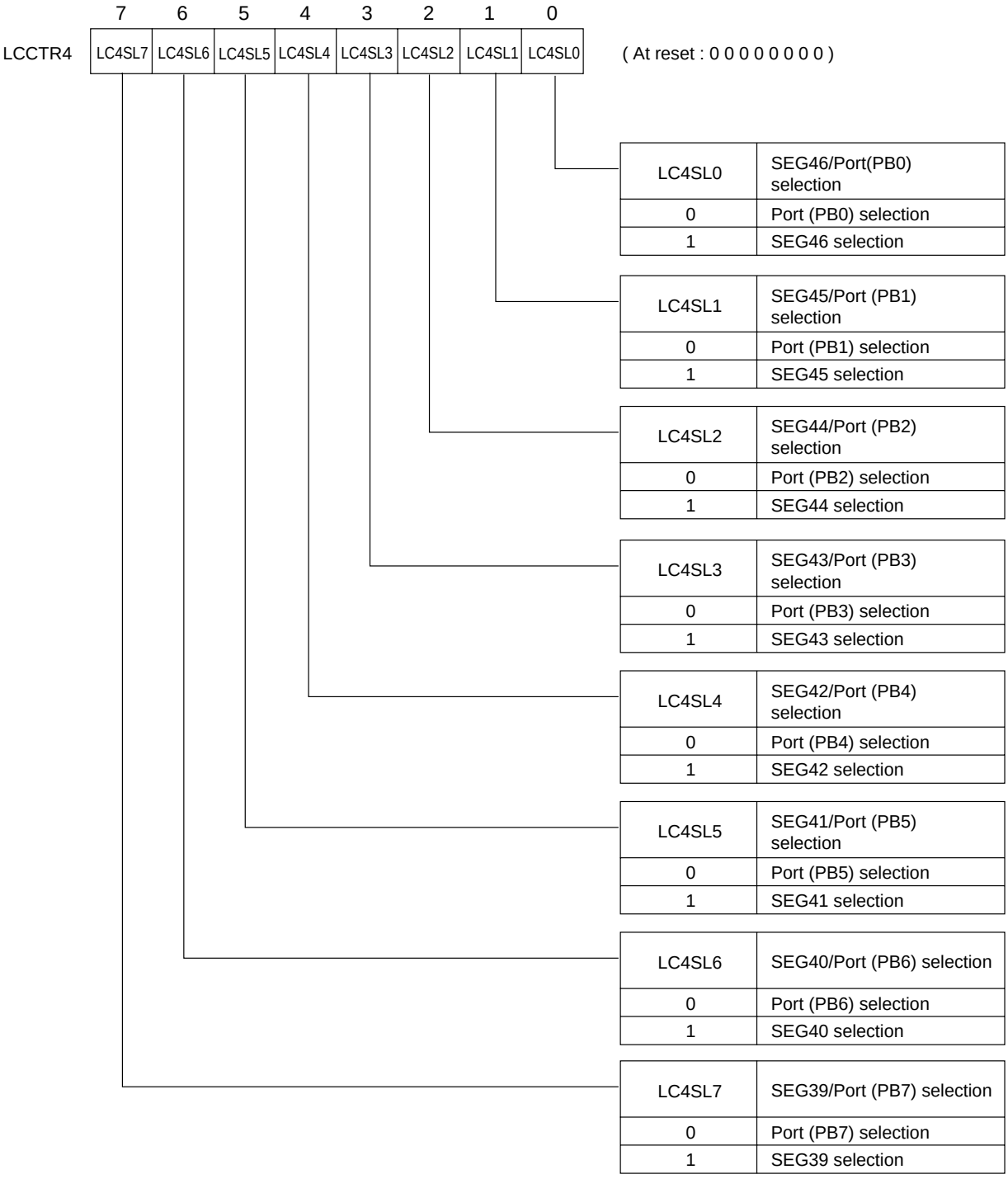

7 6 5 4 3 2 1 0
LCCTR4
LC4SL7 LC4SL6 LC4SL5 LC4SL4 LC4SL3 LC4SL2 LC4SL1 LC4SL0
(At reset : 0 0 0 0 0 0 0 0)
LC4SL0 SEG46/Port(PB0) selection
0 Port (PB0) selection
1 SEG46 selection
LC4SL1 SEG45/Port (PB1) selection
0 Port (PB1) selection
1 SEG45 selection
LC4SL2 SEG44/Port (PB2) selection
0 Port (PB2) selection
1 SEG44 selection
LC4SL3 SEG43/Port (PB3) selection
0 Port (PB3) selection
1 SEG43 selection
LC4SL4 SEG42/Port (PB4) selection
0 Port (PB4) selection
1 SEG42 selection
LC4SL5 SEG41/Port (PB5) selection
0 Port (PB5) selection
1 SEG41 selection
LC4SL6 SEG40/Port (PB6) selection
0 Port (PB6) selection
1 SEG40 selection
LC4SL7 SEG39/Port (PB7) selection
0 Port (PB7) selection
1 SEG39 selection

Figure 14-2-6 Output Control Register 4 (LCCTR4: X'3FDE', R/W)

14-2-8 Segment Output Latch

A 4-bit latch is allocated per segment. Bit0 and bit4 are read out at the timing of COM0, bit1 and bit5 are read out at that of COM1, bit2 and bit6 are read out at that of COM2, and bit3 and bit7 are read out at that of COM3. If a bit points “1”, the segment pin outputs the “selected voltage”, and if a bit points “0”, the segment pin outputs “non-selected voltage”.
The assigned address are X’2E00' to X’2E17', and segment output latch value is indefined at reset. Figure 14-2-7 shows the matching of the segment output latch and the segment/common pins.

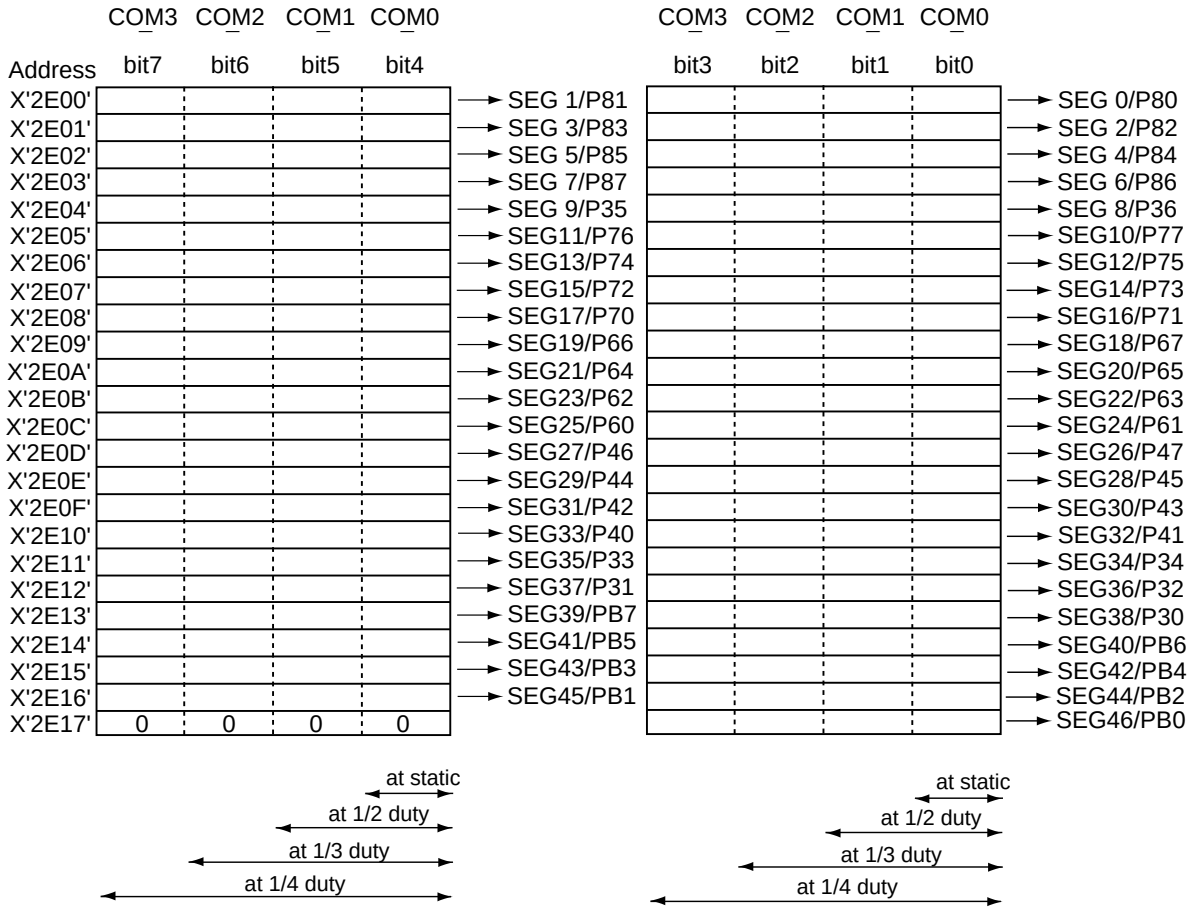


Figure 14-2-7 Matching of the Segment Output Latch and the Segment/Common Pins

> Upper 4 bits of x’2E17’ allocated to the segment output latch is unpopulated area. When data is read, “0” is read out from this area.

14-3 Operation

14-3-1 Operation

The LCD driver is capable of static display and dynamic display (1/2 duty 1/2 bias, 1/3 duty 1/3bias, 1/4 duty 1/3 bias) through the segment output pins (SEG0 to SEG46) and the common output pins (COM0 to COM3).

■The LCD driver circuit operation
The LCD driver circuit generates the timing siginals, which are necessary for controling 1/2 duty, 1/3 duty, 1/4 duty and static, at the timing control circuit, based on the LCD clock divided by the prescaler, and supplies them to the common driver and the multiplexer.

The common driver outputs the common signals which are necessary for the LCD display, based on the voltage from the LCD power supply. When the LCD is OFF V_{SS} is output and the potential difference between the LCD electrodes becomes 0 V.

The multiplexer selects the segment output latched data in response to the signal from the timing control circuit and supplies it to the segment driver. The segment driver converts the content of the segment output latch into the signals, which is capable of driving the LCD, based on the voltage supplied to LCD power supply, then outputs the segment signal.
When the LCD is OFF V_{SS} is output and the potential difference between the LCD electrodes becomes 0 V.

At reset, common pins and segment pins become high impedance.
Therefore, when reset input from external sources is long, there could be some adverse effects such as blinks of the LCD display.

In STOP mode, supplies from the main clocks is stopped, and the LCD drive cannnot be operated. Stop the LCD drive before enter STOP mode.

(1) Set “0” to the LCD display selection flag (SGDEN).
(2) Set “0” to the LCD drive starting flag (LCDEN).
(3) Set “0” to the voltage booster operation starting flag (UPEN).
(When voltage booster circuit is used)
(4) Set “1” to the pull-up resistor selection flag (LCDPUP).
(When voltage booster circuit is used)

To return from STOP mode for LCD drive, perform above procedure in the order of (4) to (1).

14-3-2 Power Supply

The LCD driver power pins are V_{LC1}, V_{LC2} and V_{LC3}. This LSI contains the voltage divider resistor for the LCD driver voltage. There are two ways to supply voltage to the LCD driver; to supply voltage to the V_{LC1}, V_{LC2} and V_{LC3} pins from external source (when external voltage divider resistor is used), and to supply voltage to the V_{LC1} pin from external source and use the internal voltage divider resistor.
The LCD driver voltage supplied through the LCD driver power pins (V_{LC1}, V_{LC2} and V_{LC3}) is converted by the LCD clock signal and the timing control signal, and then supplied to the segment driver and the common driver.

■Supplying voltage with the external voltage divider resistor

Table 14-3-1 LCD Power Supply

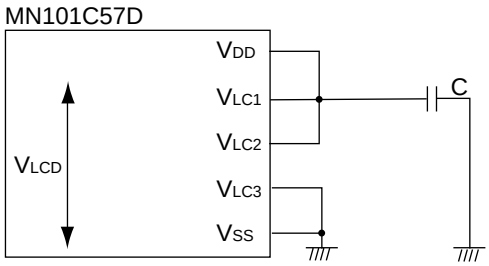
Bias Method / LCD Power Supply	Static	1/2	1/3
V_{LC1}	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$
V_{LC2}		$1/2V_{LCD} + V_{SS}$	$2/3\ V_{LCD} + V_{SS}$
V_{LC3}	V_{SS}		$1/3\ V_{LCD} + V_{SS}$

V_{LCD}: LCD panel driver voltage (Maximum voltage to the LCD panel)

Voltages of V_{LC1}, V_{LC2}, and V_{LC3} could be dropped depending on used LCD panel, and that may lower the brightness of LCD display. Use the external divider resistor when this is occured.

Figure 14-3-2 shows examples of the LCD power supply connection.

(a) Static (V_{DD}=V_{LCD})



(b) 1/3duty 1/3bias, 1/4duty 1/3bias (V_{DD}=V_{LCD})

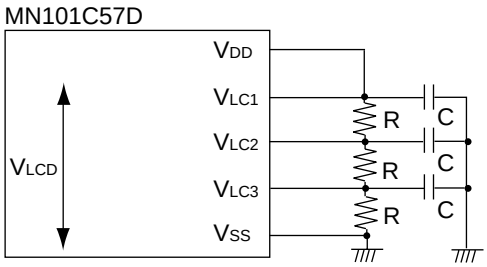


Figure 14-3-2 LCD Power Supply Connection (When Using External Voltage Divider Resistors)

1. In figure 14-3-2, current always flows through the voltage divider resistors. The following connection is used to cut the current flowing through these dividing resistors. (at $V_{LC1}=V_{DD}$)

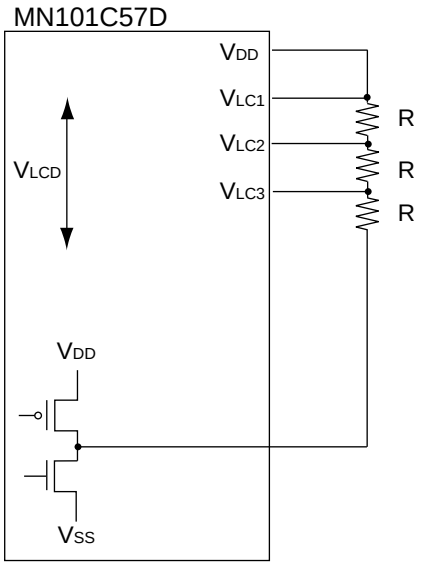


Figure 14-3-3 LCD Power Supply Connection

2. The LCD power supply V_{LC1} to 3 is supplied as shown in the following figure 14-3-4. V_{LCD} value varies depending on the type of LCD. Refer to the specifications of LCD for the appropreate value.

   $V_{LC1} = V_{LCD} + V_{SS}$

   $V_{LC2} = 2/3\ V_{DD} + V_{SS}$

   $V_{LC3} = 1/3\ V_{LCD} + V_{SS}$

   Usually $V_{DD} - V_{SS}$ are divided by resistors and supplied to the LCD. Standard registance voltage ranges from tens to several hundreds kΩ. In figure 14-3-4, a bypass capacitor C (0.01 µF to 0.1 µF) is used to lower the impedance of power supply. .

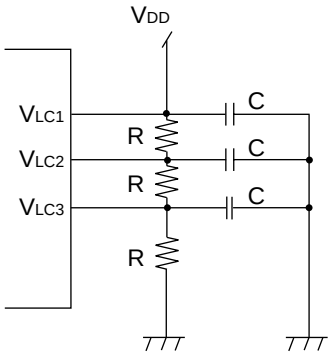


Figure 14-3-4 Supplying voltage to V_{LC1} to 3

■Supplying voltage when using the internal voltage divider circuit
Supply the voltage as shown in table 14-3-2.

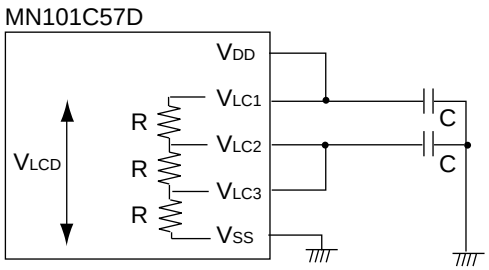
Table 14-3-2 LCD Power Supply

Bias / LCD Powersullpy	Static	1/2	1/3
V_{LC1}	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$	$V_{LCD} + V_{SS}$
V_{LC2}		1/2 $V_{LCD} + V_{SS}$	2/3 $V_{LCD} + V_{SS}$
V_{LC3}	V_{SS}		1/3 $V_{LCD} + V_{SS}$

V_{LCD}: LCD panel driver voltage (Maximum voltage to the LCD panel)

Figure 14-3-5 shows examples of the LCD power supply connection.

(a) 1/2duty 1/2bias ($V_{DD}=V_{LCD}$)



(b) 1/3duty 1/3bias, 1/4duty 1/3bias ($V_{DD}=V_{LCD}$)

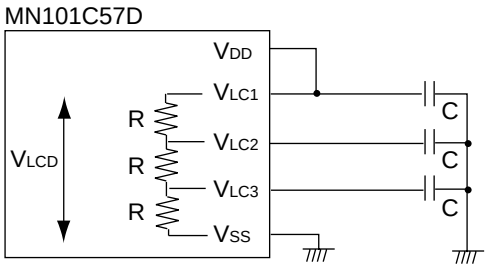


Figure 14-3-5 LCD Power Supply Connection

14-3-3 Frame Cycle

■Setup of the LCD frame cycle

The clock fosc or fx is divided by the prescaler and supplied as the LCD clock. Set the LCD clock with bit0 to 3 and set the LCD frame cycle with bit4 to 5 of the LCDMD1 register. Table 14-3-3 shows reference input frequencies and the matching of the LCD clock and the LCD frame cycle.

Table 14-3-3 Input Frequency and the LCD Clock

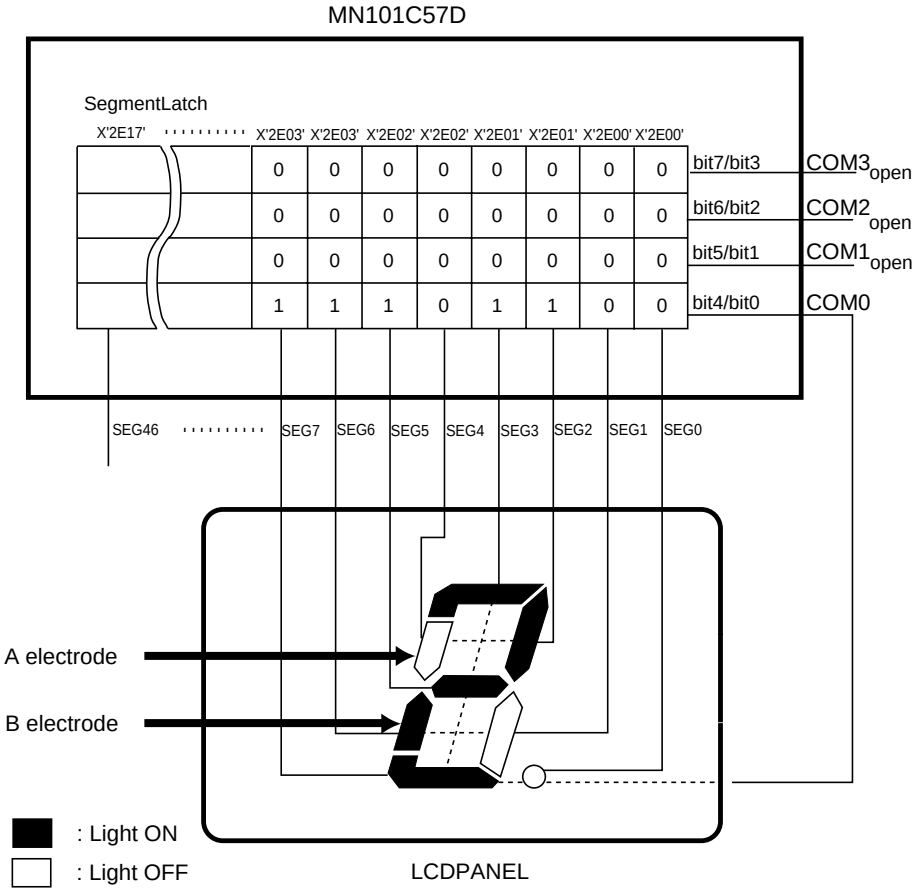
		Input frequency									
Input clock	Duty	20 MHz		16 MHz		8 MHz		4 MHz		32.768 kHz	
LCDCK3 to 0	LCDTY1 to 0	LCD clock	frame	LCD clock	frame	LCD clock	frame	LCD clock	flame	LCD clock	frame
0000 (OSC1/2^{11})	00 (1/4 duty)	9766 Hz	2441 Hz	7813 Hz	1953 Hz	3906 Hz	977 Hz	1953 Hz	488 Hz		
	01 (1/3 duty)		3255 Hz		2604 Hz		1302 Hz		651 Hz		
	10 (1/2 duty)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
	11 (static)		9766 Hz		7813 Hz		3906 Hz		1953 Hz		
0001 (OSC1/2^{12})	00 (1/4 duty)	4883 Hz	1221 Hz	3906 Hz	977 Hz	1953 Hz	488 Hz	977 Hz	244 Hz		
	01 (1/3 duty)		1628 Hz		1302 Hz		651 Hz		326 Hz		
	10 (1/2 duty)		2441 Hz		1953 Hz		977 Hz		488 Hz		
	11 (static)		4883 Hz		3906 Hz		1953 Hz		977 Hz		
0010 (OSC1/2^{13})	00 (1/4 duty)	2441Hz	610 Hz	1953 Hz	488 Hz	977 Hz	244 Hz	488 Hz	122 Hz		
	01 (1/3 duty)		814 Hz		651 Hz		326 Hz		163 Hz		
	10 (1/2 duty)		1221 Hz		977 Hz		488 Hz		244 Hz		
	11 (static)		2441 Hz		1953 Hz		977 Hz		488 Hz		
0011 (OSC1/2^{14})	00 (1/4 duty)	1221 Hz	305 Hz	977 Hz	244 Hz	488 Hz	122 Hz	244 Hz	61 Hz		
	01 (1/3 duty)		407 Hz		326 Hz		163 Hz		81 Hz		
	10 (1/2 duty)		610 Hz		488 Hz		244 Hz		122 Hz		
	11 (static)		1221 Hz		977 Hz		488 Hz		244 Hz		
0100 (OSC1/2^{15})	00 (1/4 duty)	610 Hz	153 Hz	488 Hz	122 Hz	244 Hz	61 Hz	122 Hz	31 Hz		
	01 (1/3 duty)		203 Hz		163Hz		81 Hz		41 Hz		
	10 (1/2 duty)		305 Hz		244 Hz		122 Hz		61 Hz		
	11 (static)		610 Hz		488 Hz		244 Hz		122 Hz		
0101 (OSC1/2^{16})	00 (1/4 duty)	305 Hz	76 Hz	244 Hz	61 Hz	122 Hz	31 Hz	61 Hz	15 Hz		
	01 (1/3 duty)		102 Hz		81 Hz		41 Hz		20 Hz		
	10 (1/2 duty)		153 Hz		122 Hz		61 Hz		31 Hz		
	11 (static)		305 Hz		244 Hz		122 Hz		61 Hz		
0110 (OSC1/2^{17})	00 (1/4 duty)	153 Hz	38 Hz	122 Hz	31 Hz	61 Hz	15 Hz	31 Hz	8 Hz		
	01 (1/3 duty)		51 Hz		41 Hz		20 Hz		10 Hz		
	10 (1/2 duty)		76 Hz		61 Hz		31 Hz		15 Hz		
	11 (static)		153 Hz		122 Hz		61 Hz		31 Hz		
0111 (OSC1/2^{18})	00 (1/4 duty)	76 Hz	19 Hz	61 Hz	15 Hz	31 Hz	8 Hz	15 Hz	4 Hz		
	01 (1/3 duty)		25 Hz		20 Hz		10 Hz		5 Hz		
	10 (1/2 duty)		38 Hz		31 Hz		15 Hz		8 Hz		
	11 (static)		76 Hz		61 Hz		31 Hz		15 Hz		
1X00 (XI/2^{6})	00 (1/4 duty)									512 Hz	128 Hz
	01 (1/3 duty)										171 Hz
	10 (1/2 duty)										256 Hz
	11 (static)										512 Hz
1X01 (XI/2^{7})	00 (1/4 duty)									256 Hz	64 Hz
	01 (1/3 duty)										85 Hz
	10 (1/2 duty)										128 Hz
	11 (static)										256 Hz
1X10 (XI/2^{8})	00 (1/4 duty)									128 Hz	32 Hz
	01 (1/3 duty)										43 Hz
	10 (1/2 duty)										64 Hz
	11 (static)										128 Hz
1X11 (XI/2^{9})	00 (1/4 duty)									64 Hz	16 Hz
	01 (1/3 duty)										21 Hz
	10 (1/2 duty)										32 Hz
	11 (static)										64 Hz

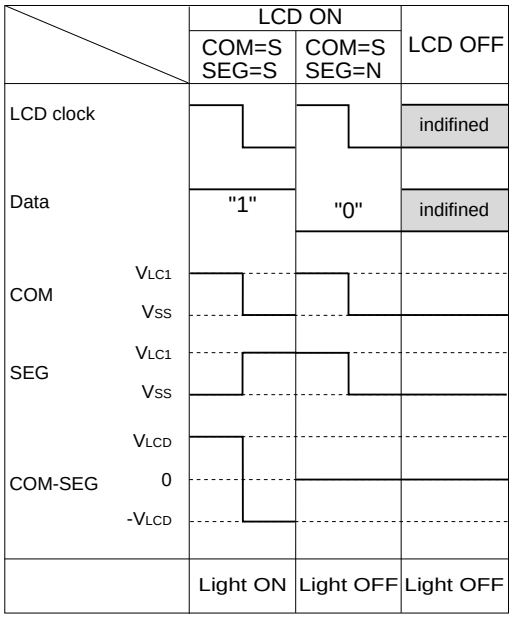
14-4 Display

Figures 14-4-1 to 14-4-5 show examples of connections, displays and waveforms of the LCD panel in these condition - in 1/2 duty, 1/3 duty, 1/4 duty and static.

14-4-1 Static

■**Static**


MN101C57D
SegmentLatch
X'2E17'
X'2E03' X'2E03' X'2E02' X'2E02' X'2E01' X'2E01' X'2E00' X'2E00'
0 0 0 0 0 0 0 0 bit7/bit3 COM3open
0 0 0 0 0 0 0 0 bit6/bit2 COM2open
0 0 0 0 0 0 0 0 bit5/bit1 COM1open
1 1 1 0 1 1 0 0 bit4/bit0 COM0
SEG46
SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0
A electrode
B electrode
: Light ON
: Light OFF
LCDPANEL



S:selected voltage N:non-selected voltage V_{LCD}:LCD driver voltage

COM(COM0) always outputs the selected voltage in static.

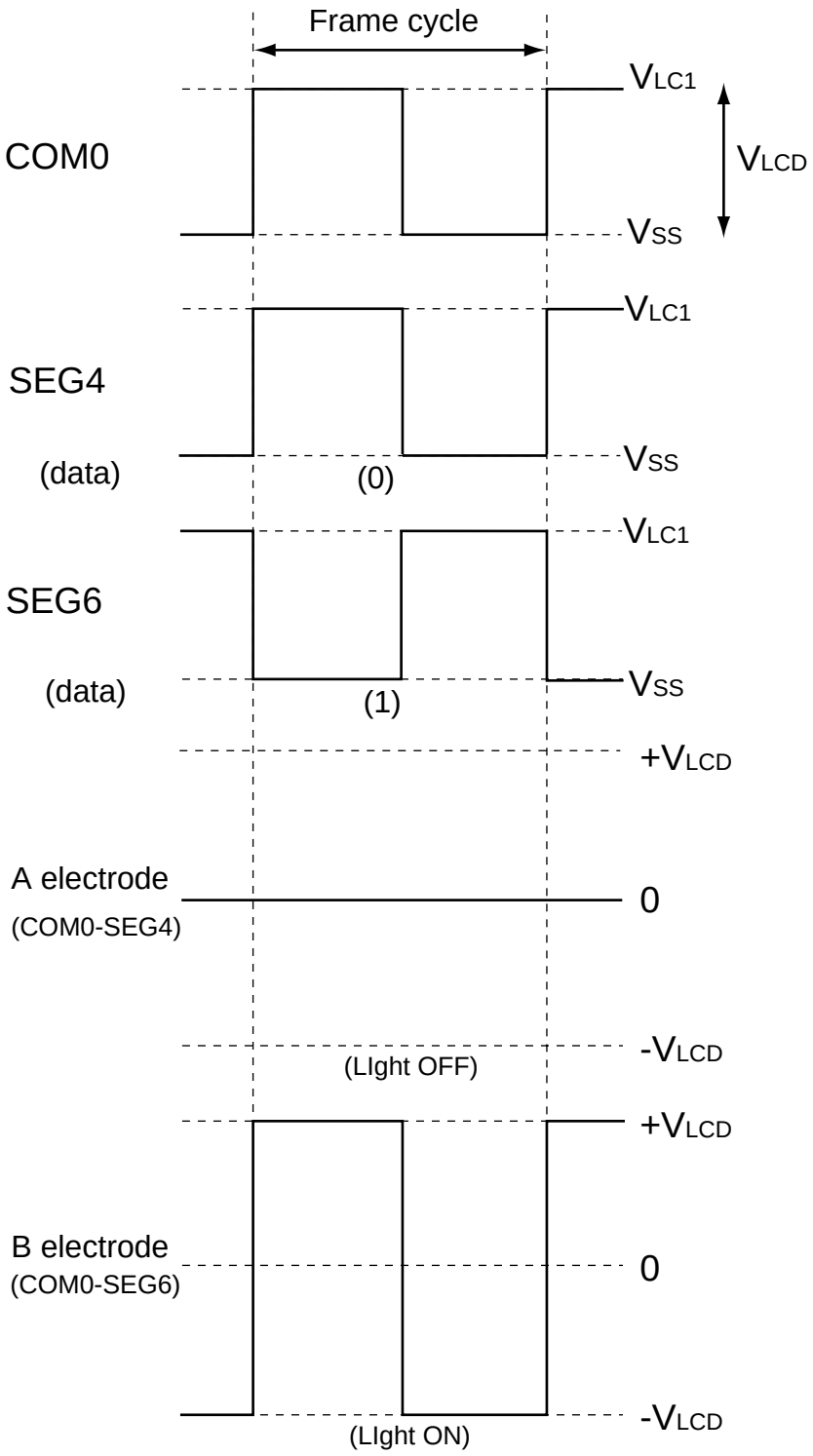


Figure 14-4-1 LCD Display in Static

14-4-2 Setup Example (static)

■Setup example of the LCD (static)

An example of setup procedure to display “23” with both segment signals (SEG0 to SEG7) and common signals (COM0), using an external divider resistor is shown below.

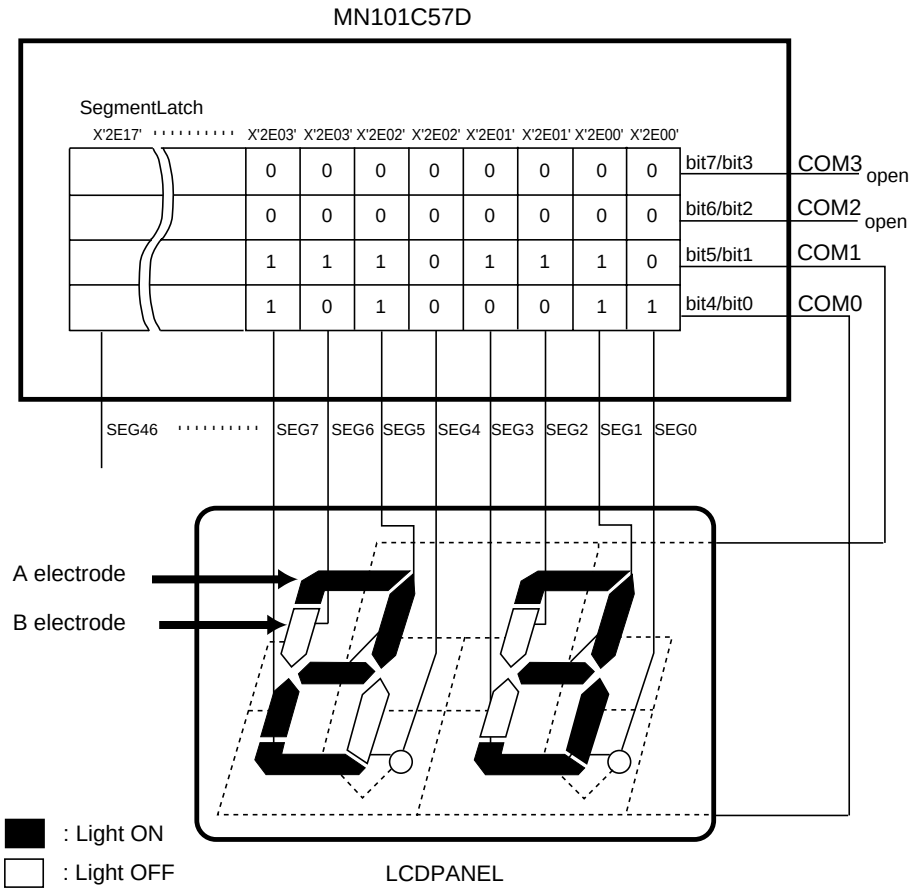
[☞ Chapter 14 14-4-1. LCD Display (static)]

Clock source fosc=4 MHz, a LDC clock source fosc/2^{15} =122 Hz, and flame cycle=122 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCMD1(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register (LCMD) to stop the LCD operation.
(2) Setup the display duty LCMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 11	(2) Set “0” to the LC1SEL flag of the LCD mode control register (LCMD) to enter the static drive mode.
(3) Select the LCD clock source LCMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0100	(3) Select fosc/2^{15} as a LCD clock source with LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Select the segment output/port pin Select the common output/port pin LCCTR(X’3FDB’) bp1 :LC1SL1 = 1 bp2 :COMSL0 = 1	(4) Select SEG0 to 7 with the output control register (LCCTR1), and select COM1 with the COMSL0.
(5) Setup the LCD panel display data Segment output latch SEG1-0 (X’2E00’) = X’00’ Segment output latch SEG3-2 (X’2E01’) = X’11’ Segment output latch SEG5-4 (X’2E02’) = X’10’ Segment output latch SEG7-6 (X’2E03’) = X’11’	(5) Display “23” on the display panel with the address X’2E00’ to X’2E03’ of the segment output latch SEG0-7. [☞Chapter 14 14-4-1 the LCD display example (static)]
(6) Start the LCD operation LCMD(X’3FCD’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register (LCMD1) to start the LCD operation.

14-4-3 1/2 duty

■1/2 Duty


MN101C57D
SegmentLatch
X'2E17'
X'2E03' X'2E03' X'2E02' X'2E02' X'2E01' X'2E01' X'2E00' X'2E00'
0 0 0 0 0 0 0 0 bit7/bit3 COM3 open
0 0 0 0 0 0 0 0 bit6/bit2 COM2 open
1 1 1 0 1 1 1 0 bit5/bit1 COM1
1 0 1 0 0 0 1 1 bit4/bit0 COM0
SEG46
SEG7 SEG6 SEG5 SEG4 SEG3 SEG2 SEG1 SEG0
A electrode
B electrode
: Light ON
: Light OFF
LCDPANEL

	LCD ON				LCD OFF
	COM=S SEG=S	COM=N SEG=S	COM=S SEG=N	COM=N SEG=N	
LCD clock					indifined
Data	"1"		"0"		indifined
COM	V_{LC1} / V_{LC2}=V_{LC3} / V_{SS}				
SEG	V_{LC1} / V_{LC2}=V_{LC3} / V_{SS}				
COM-SEG	V_{LCD} / 1/2V_{LCD} / 0 / -1/2V_{LCD} / -V_{LCD}				
	Light ON	Light OFF	Light OFF	Light OFF	Light OFF

S:selected voltage N:non-selected voltage V_{LCD}:LCD driver voltage

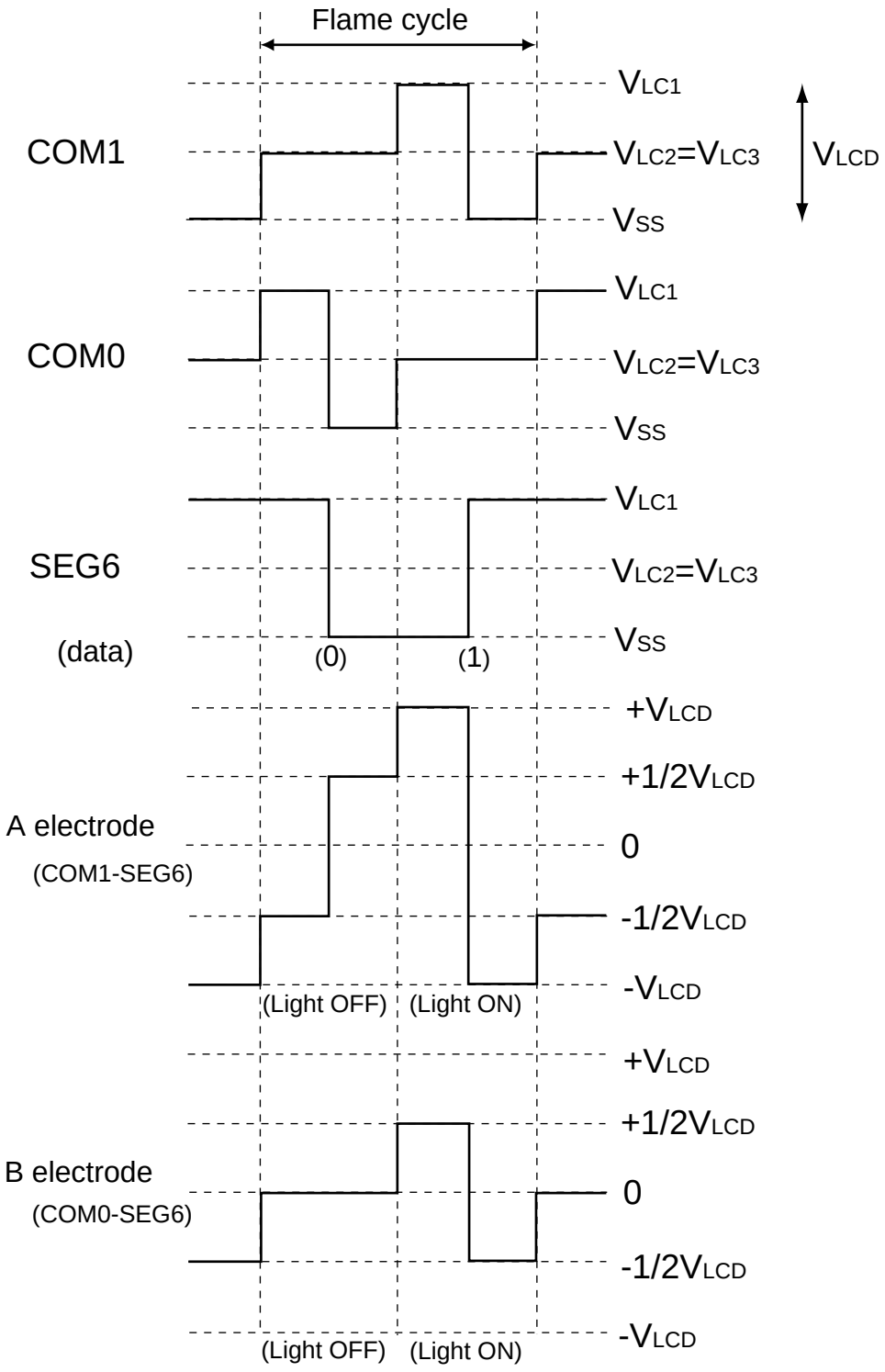


Figure 14-4-2 LCD Display (1/2 Duty)

14-4-4 Setup Example (1/2 duty)

■Setup example of the LCD (1/2 duty)

An example of setup procedure to display 8-shaped double figures “23” with both segment signals (SEG0 to SEG7) and common signals (COM0 to COM1) in 1/2 duty, 1/2 bias, using an external divider resistor is shown below.

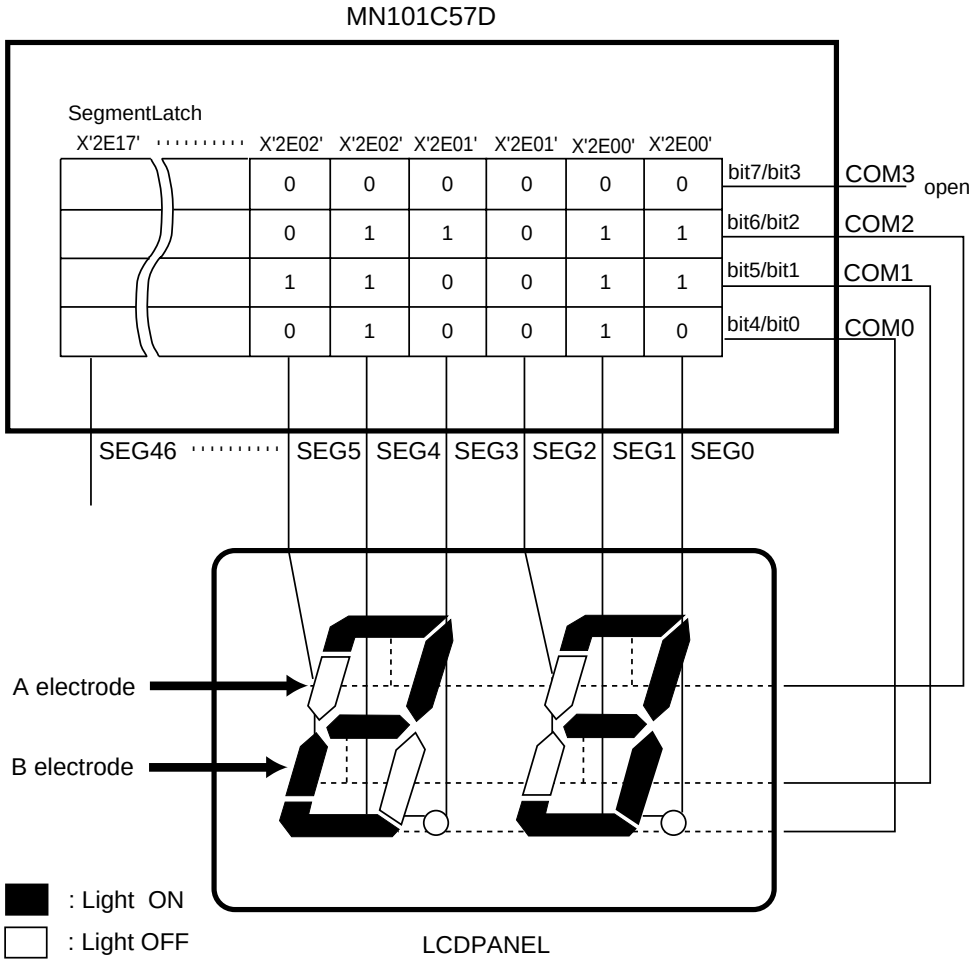
[☞ Chapter 14 14-4-3. LCD Display (1/2 duty)]

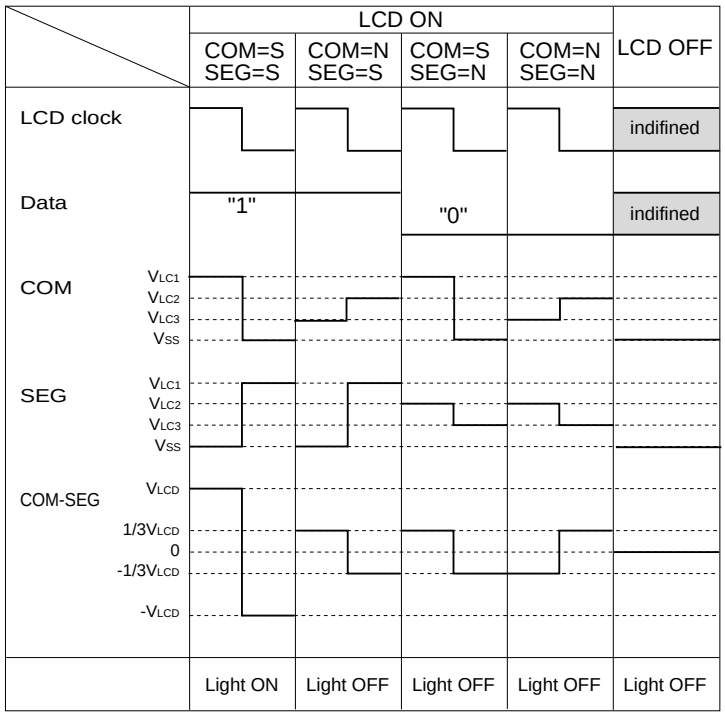
Clock source fosc=4 MHz, LDC clock source fosc/2^{15} =122 Hz, and flame cycle=61 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCMD1(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register (LCMD) to stop the LCD operation.
(2) Setup the display duty LCMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 11	(2) Set “0” to the LC1SEL flag of the LCD mode control register (LCMD) to enter the static drive mode.
(3) Select the LCD clock source LCMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0100	(3) Select fosc/2^{15} as the LCD clock source with LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Select the segment output/port pin Select the common output/port pin LCCTR(X’3FDB’) bp1 :LC1SL1 = 1 bp3-2 :COMSL1-0 = 1	(4) Select SEG0 to 7 with the LC1SL1 of the output control register (LCCTR1), and select COM1-0 with the COMSL1-0.
(5) Setup the LCD panel display data Segment output latch SEG1-0 (X’2E00’) = X’31’ Segment output latch SEG3-2 (X’2E01’) = X’22’ Segment output latch SEG5-4 (X’2E02’) = X’30’ Segment output latch SEG7-6 (X’2E03’) = X’32’	(5) Display “23” on the display panel with the address X’2E00’ to X’2E03’ of the segment output latch SEG0-7. [☞ Chapter 14 14-4-3 the LCD display example (1/2 duty)]
(6) Start the LCD operation LCMD(X’3FCD’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register (LCMD1) to start the LCD operation.

14-4-5 1/3 duty

■1/3 Duty





S:selected voltage N:non-selected voltage V_{LCD}:LCD driver voltage

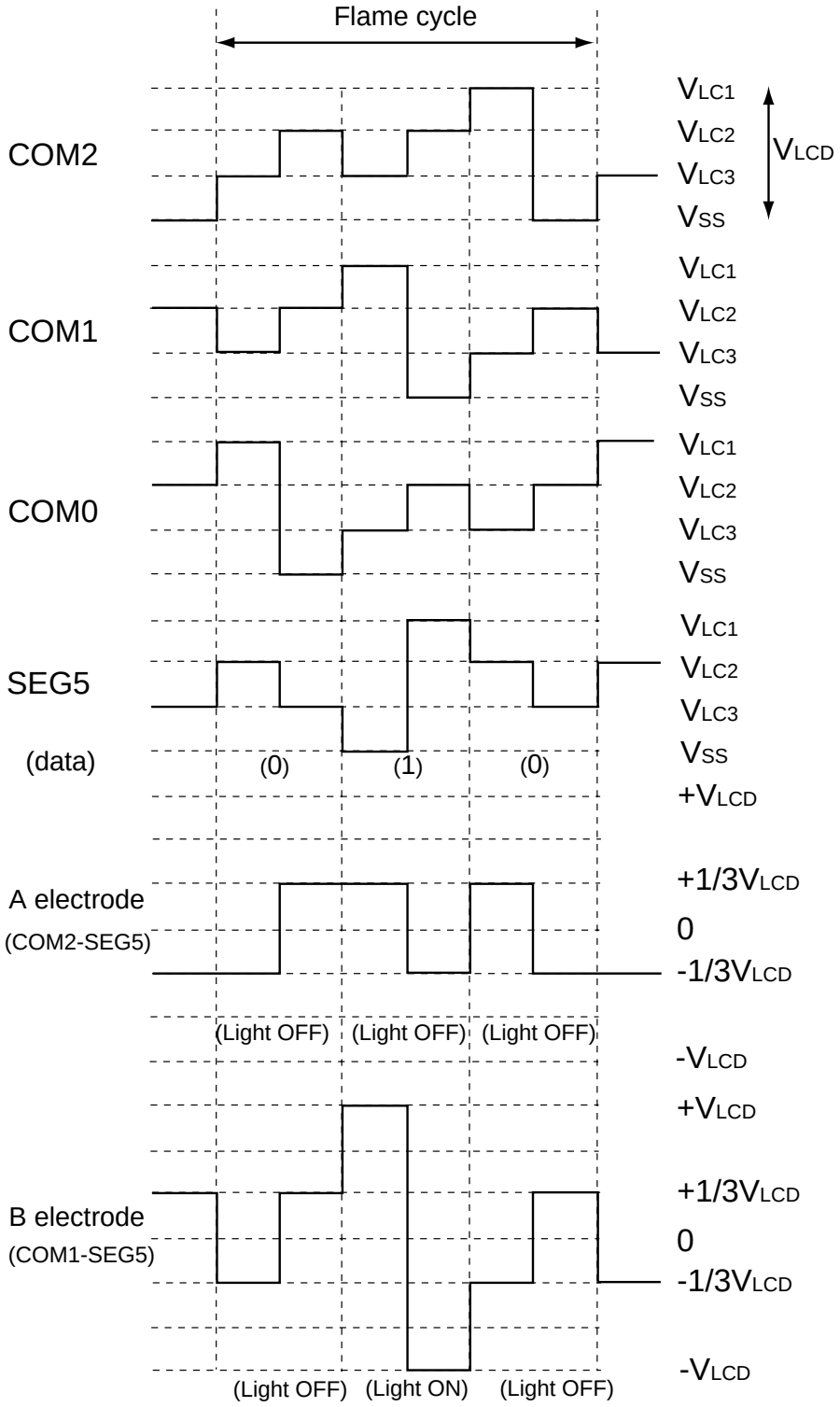


Figure 14-4-3 LCD Display (1/3 Duty)

14-4-6 Setup Example (1/3 duty)

■Setup example of the LCD (1/3 duty)

An example of setup procedure to display 8-shaped double figures “23” with both segment signals (SEG0 to SEG5) and common signals (COM0 to COM2) in 1/3 duty, 1/3 bias, using an external divider resistor is shown below.

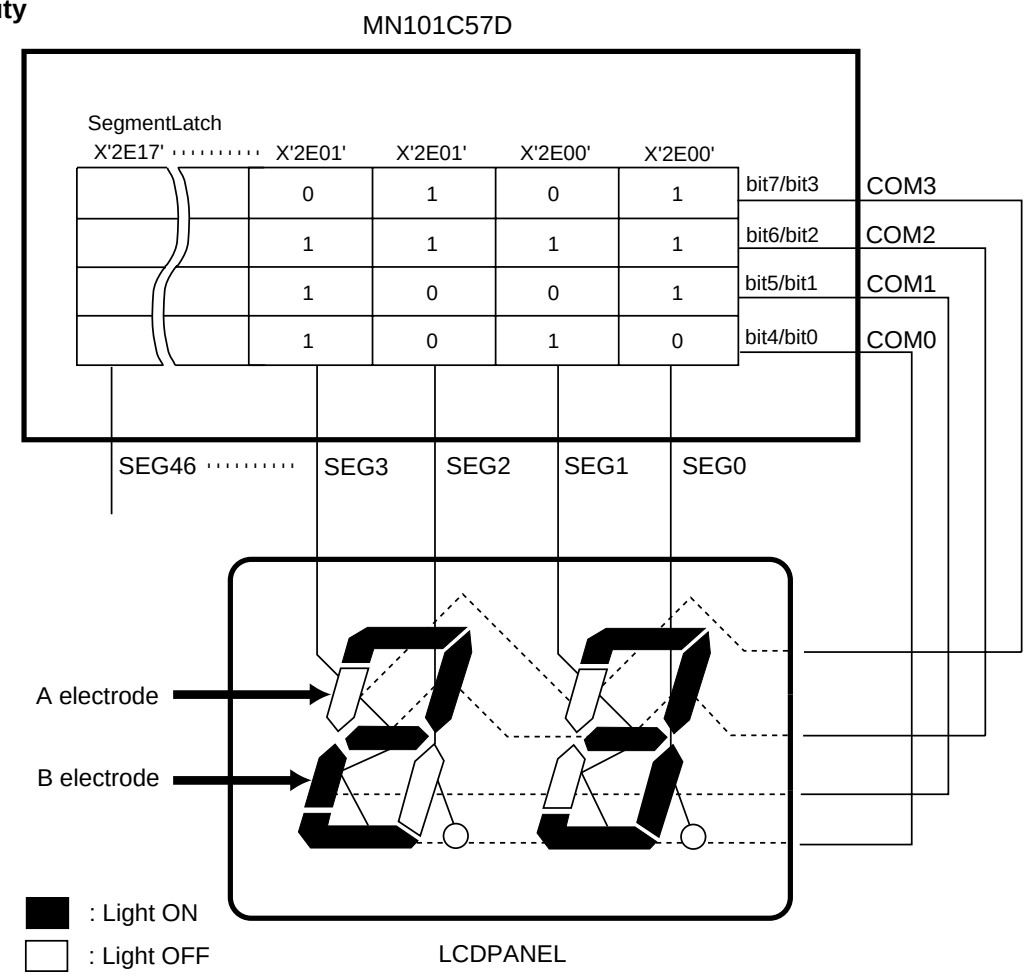
[☞ Chapter 14 14-4-5. LCD Display (1/3 duty)]

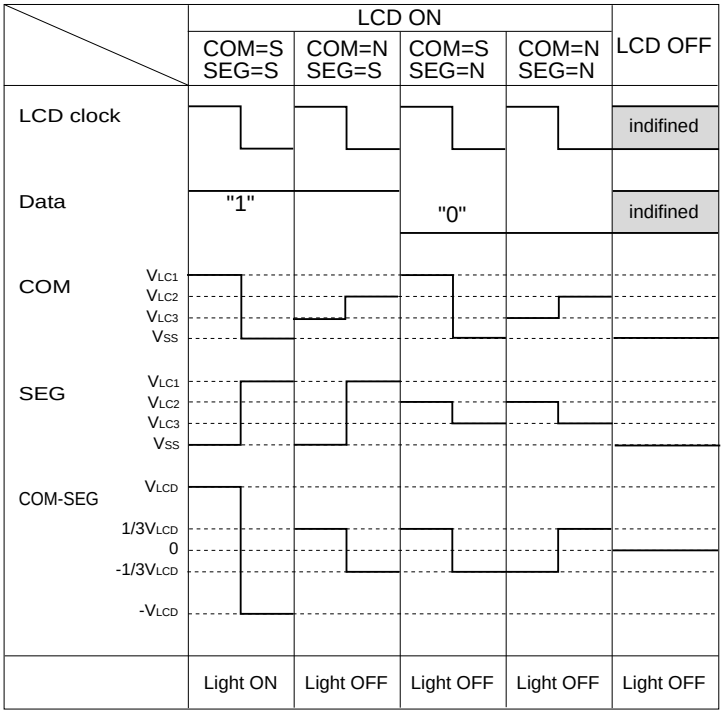
Clock source fosc=4 MHz, LDC clock source fosc/2^{15} =122 Hz, and flame cycle=41 Hz are selected in this example.

Setup Procedure	Description
(1) Stop the LCD operation LCMD1(X’3FD9’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register (LCMD) to stop the LCD operation.
(2) Setup the display duty LCMD1(X’3FD9’) bp5-4 : LCDDTY1-0 = 11	(2) Set “0” to the LC1SEL flag of the LCD mode control register (LCMD) to enter the static drive mode.
(3) Select the LCD clock source LCMD1(X’3FD9’) bp3-0 :LCDCK3-0 = 0100	(3) Select fosc/2^{15} as the LCD clock source with LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Select the segment output/port pin Select the common output/port pin LCCTR(X’3FDB’) bp1 :LC1SL1 = 1 bp4-2 :COMSK2-0 = 111	(4) Select SEG0 to 7 with the LC1SL1 of the output control register (LCCTR1), and select COM2-0 with the COMSL2-0.
(5) Setup the LCD panel display data Segment output latch SEG1-0 (X’2E00’) = X’76’ Segment output latch SEG3-2 (X’2E01’) = X’40’ Segment output latch SEG5-4 (X’2E02’) = X’27’	(5) Display “23” on the display panel with the address X’2E00’ to X’2E02’ of the segment output latch SEG0-7. [☞ Chapter 14 14-4-5. the LCD display example (1/3 duty)]
(6) Start the LCD operation LCMD(X’3FCD’) bp7 :LCDEN = 1	(6) Set “1” to the LCDEN flag of the LCD mode control register (LCMD1) to start the LCD operation.

14-4-7 1/4 duty

■**1/4 Duty**





S:selected voltage N:non-selected voltage V_{LCD}:LCD driver voltage

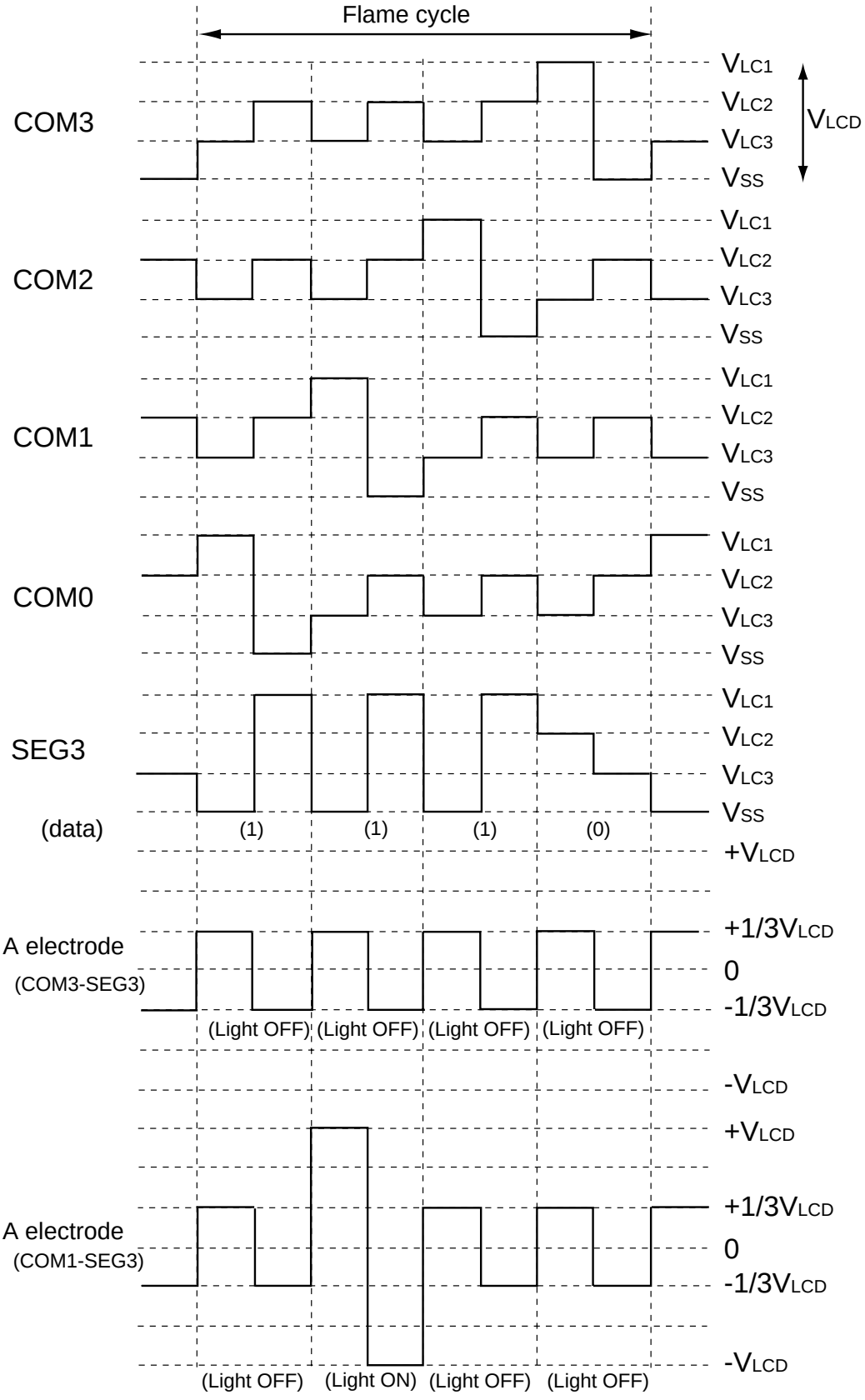


Figure 14-4-4 LCD Display (1/4 Duty)

14-4-8 Setup Example (1/4 duty)

■Setup example of the LCD (1/4 duty)

An example of setup procedure to display 8-shaped 15 figures “323232323232323” with both segment signals (SEG0 to SEG29) and common signals (COM0 to COM3) in 1/4 duty, 1/3 bias, using an external divider resistor is shown below.

[☞ Chapter 14 14-4-7. LCD Display (1/4 duty)]

Clock source fosc=4 MHz, LDC clock source fosc/2^{15} =122 Hz, and flame cycle=31 Hz are selected in this exmple.

Setup Procedure	Description
(1) Stop the LCD operation LCMD(X’3FCD’) bp7 : LCDEN = 0	(1) Set “0” to the LCDEN flag of the LCD mode control register (LCMD) to stop the LCD operation.
(2) Setup the display duty LCMD(X’3FCD’) bp5-4 : LCDDTY1-0 = 00	(2) Set the display duty 1/4 with the LC0DTY1-0 flag of the LCD mode control register (LCMD).
(3) Select the LCD clock source LCMD(X’3FCD’) bp3-0 : LCDCK3-0 = 0100	(3) Select fosc/2^{15} as the LCD clock source with LCDCK3 to 0 flags of the LCD mode control register (LCMD).
(4) Select the segment output/port pin Select the common output/port pin LCCTR1(X’3FDB’) bp1 :LC1SL1-0 = 11 LCCTR2(X’3FDC’) bp7-0 :LC2SL7-0 = 11111111 LCCTR3(X’3FDD’) bp3-2 :LC3SL3-2 = 11 LCCTR(X’3FDB’) bp1 :LC1SL1 = 1 bp5-2 :COMSL3-0 = 1111	(4) Select SEG0 to 29 with the output control registers(LCCTR1), (LCCTR2), (LCCTR3), and select COM3-0 with the COSL3-0.
(5) Setup the LCD panel display data Segment output latch SEG1-0 X’2E00’ = X’5E’ Segment output latch SEG3-2 X’2E01’ = X’7C’ Segment output latch SEG5-4 X’2E02’ = X’5E’	(5) Display “323232323232323” on the display panel with the address X’2E00’ to X’2E2E’ of the segment output latch SEG0-29. [☞ Chapter 14 14-4-7. the LCD display example (1/4 duty)]

Setup Procedure	Description
Segment output latch SEG7-6 X'2E03' = X'7C' Segment output latch SEG9-8 X'2E04' = X'5E' Segment output latch SEG11-10 X'2E05' = X'7C' Segment output latch SEG13-12 X'2E06' = X'5E' Segment output latch SEG15-14 X'2E07' = X'7C' Segment output latch SEG17-16 X'2E08' = X'5E' Segment output latch SEG19-18 X'2E09' = X'7C' Segment output latch SEG21-20 X'2E0A' = X'5E' Segment output latch SEG23-22 X'2E0B' = X'7C' Segment output latch SEG25-24 X'2E0C' = X'5E' Segment output latch SEG27-26 X'2E0D' = X'7C' Segment output latch SEG29-28 X'2E0E' = X'5E'	
(6) Start the LCD operation LCMD(X'3FCD') bp7 :LCDEN = 1	(6) Set "1" to the LCDEN flag of the LCD mode control register (LCMD1) to start the LCD operation.

Chapter 15 Remote Control Functions

15-1 Overview

The remote control reception pin (P25) of this LSI is also used as port input pin. The remote control reception fuction is compatible with the Kaseikyo format and others.

15-1-1 Overview

Table 15-1-1 shows the functions of the remote control reception.

Table 15-1-1 Functions of Remote Control Reception

	Remote control	
Interrupt source	Remote control	shift baffer header counter overflow data error
Pins	P25	
Receivable format	Kaseikyo format Input data rising / falling inversion format Long time (T) format Headerless format	
Data determination	User definable count margin Header only / header + 8-bit data	
1T data	Option	
0/1 data	Option	
Header system	Headerless format Header H/L interval count	
Sampling clock	fx, fx/2, fx/2^2, fx/2^3, fosc/2^9,fosc/2^{10},fosc/2^{11},fosc/2^{12} *Remote control reception is enable at low speed clock (SLOW, HALT1)	
Noise filter	Selectable	
Edge recognition	Rising / falling / both edges	
fosc: Machine clock (High frequency oscillation) fx: Machine clock (Low frequency oscillation)		

15-1-2 Block Diagram

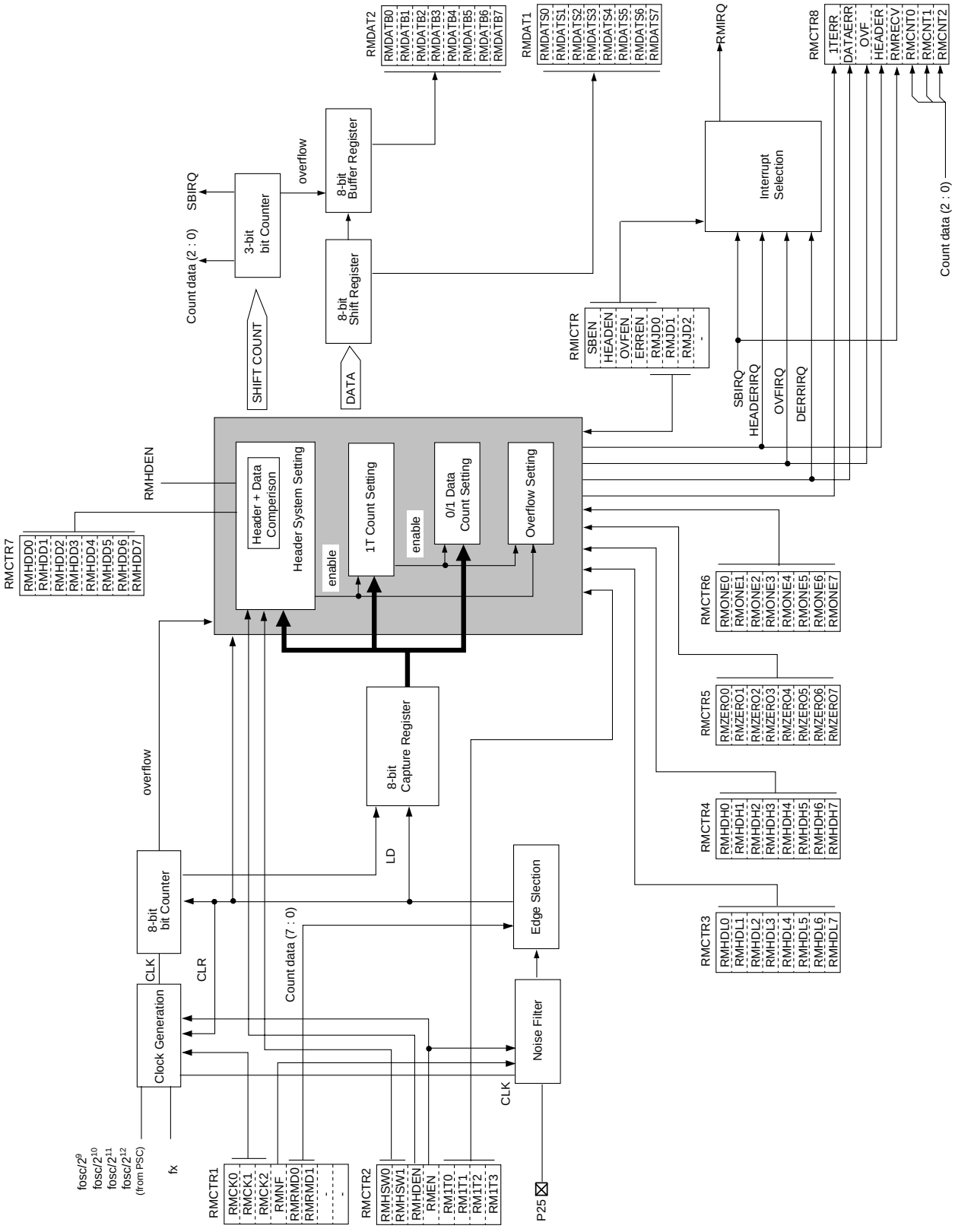


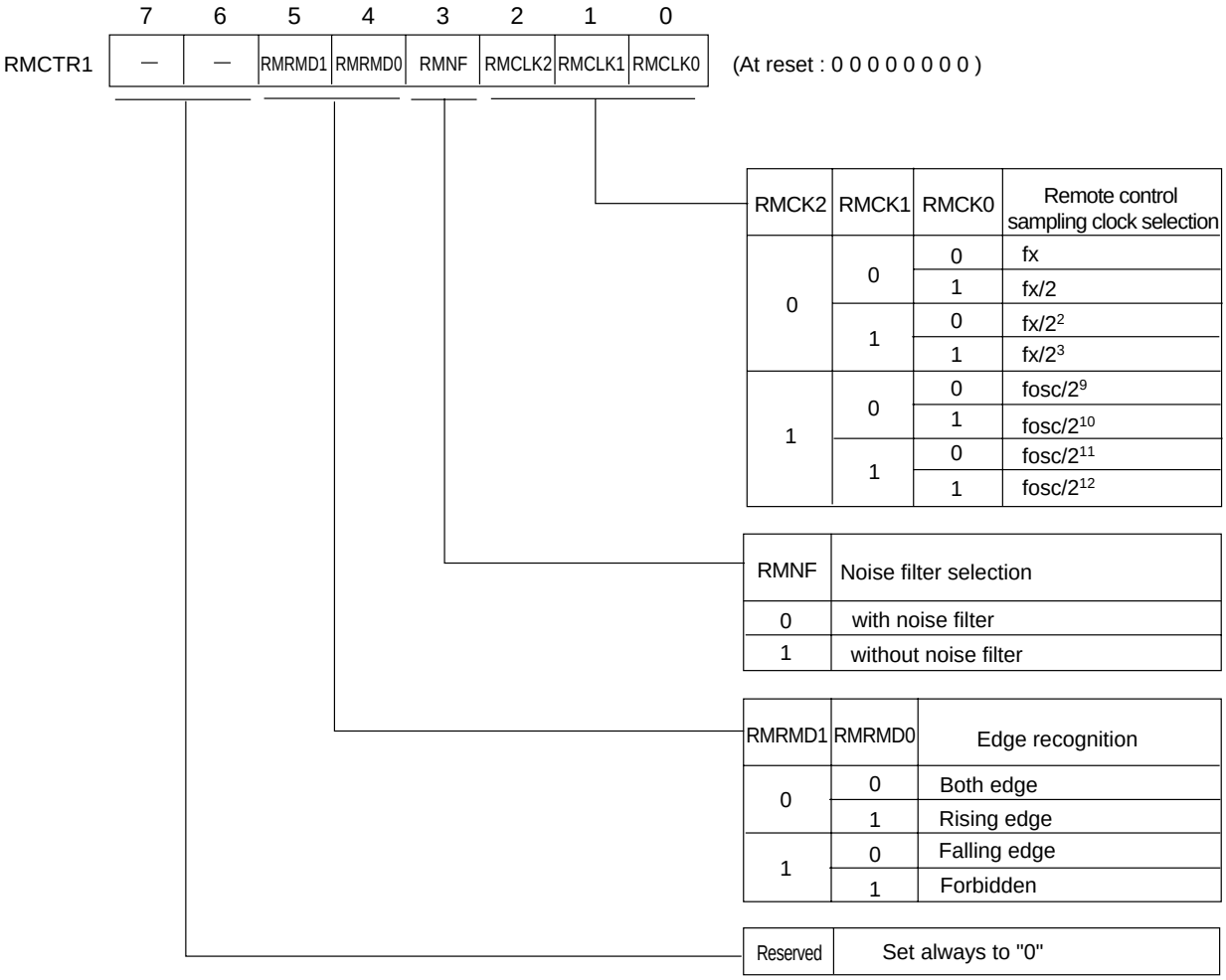
Figure 15-1-1 Block Diagram of Remote Control Reception Function

15-2 Control Registers

Table 15-2-1 shows a list of the control registers for remote control reception functions.

Tabel 15-2-1 Control Registers List

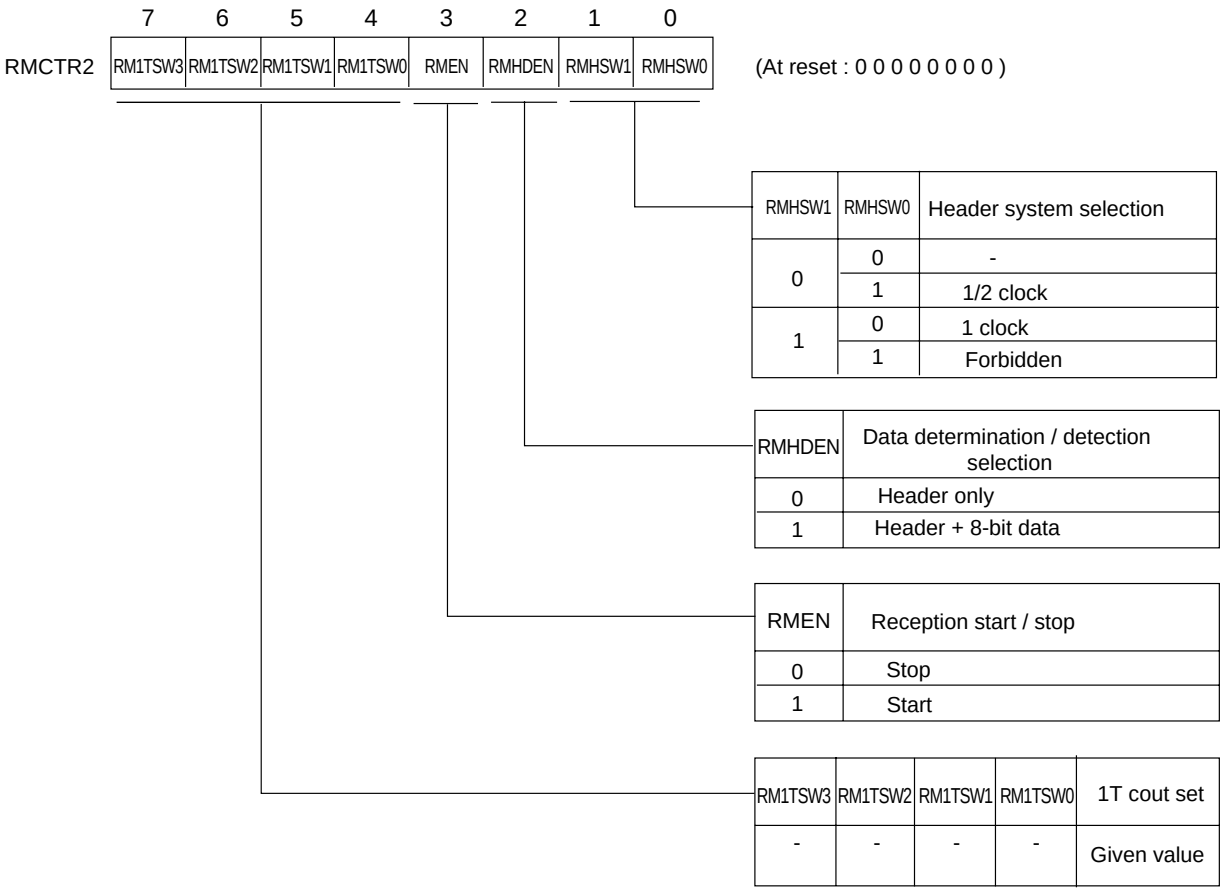
	Register	Address	R/W	Function	Page
Remote Control Reception	RMCTR1	X'03FC5'	R/W	Remote Control Register 1	XV - 5
	RMCTR2	X'03FC6'	R/W	Remote Control Register 2	XV - 6
	RMCTR3	X'03FC7'	R/W	Remote Control Register 3	XV - 7
	RMCTR4	X'03FC8'	R/W	Remote Control Register 4	XV - 7
	RMCTR5	X'03FC9'	R/W	Remote Control Register 5	XV - 8
	RMCTR6	X'03FCA'	R/W	Remote Control Register 6	XV - 8
	RMCTR7	X'03FCB'	R/W	Remote Control Register 7	XV - 8
	RMCTR8	X'03FCC'	R	Remote Control Register 8	XV - 9
	RMDAT1	X'03FCD'	R	Remote Control Shift Data	XV - 10
	RMDAT2	X'03FCE'	R	Remote Control Buffer Data	XV - 10
	RMICTR	X'03FCF'	R/W	Remote Control Interrupt Set Register	XV - 11



Tabel 15-2-1 Remote Control Register1 (RMCTR1 : x'03FC5')

Set the prescaler count enable in advance when using sampling clock derived from fosc.
[☞ Chepter 5 5-2-2. Control Registers]

When sampling clock derived from fx is used, the remote control reception functions works even when the prescaler count is disabled.


7 6 5 4 3 2 1 0
RMCTR2
RM1TSW3 RM1TSW2 RM1TSW1 RM1TSW0 RMEN RMHDEN RMHSW1 RMHSW0
(At reset : 0 0 0 0 0 0 0 0)
RMHSW1 RMHSW0 Header system selection
0 0 -
1 1/2 clock
1 0 1 clock
1 Forbidden
RMHDEN Data determination / detection selection
0 Header only
1 Header + 8-bit data
RMEN Reception start / stop
0 Stop
1 Start
RM1TSW3 RM1TSW2 RM1TSW1 RM1TSW0 1T cout set
- - - - Given value

Tabel 15-2-2 Remote Control Register2 (RMCTR2: x'03FC6')

	7	6	5	4	3	2	1	0	
RMCTR3	RMHDL7	RMHDL6	RMHDL5	RMHDL4	RMHDL3	RMHDL2	RMHDL1	RMHDL0	(At reset : 0 0 0 0 0 0 0 0)

RMHDL7	RMHDL6	RMHDL5	RMHDL4	RMHDL3	RMHDL2	RMHDL1	RMHDL0	Header L interval count setup
-	-	-	-	-	-	-	-	Given value

Tabel 15-2-3 Remote Control Register3 (RMCTR3: x'03FC7')

	7	6	5	4	3	2	1	0	
RMCTR4	RMHDH7	RMHDH6	RMHDH5	RMHDH4	RMHDH3	RMHDH2	RMHDH1	RMHDH0	(At reset : 0 0 0 0 0 0 0 0)

RMHDH7	RMHDH6	RMHDH5	RMHDH4	RMHDH3	RMHDH2	RMHDH1	RMHDH0	Header H interval count setup
-	-	-	-	-	-	-	-	Given value

Tabel 15-2-4 Remote Control Register4 (RMCTR4: x'03FC8')

Set "0" to the header "L" and "H" intervals when they are unused. Do not set less than 2 counts as the count setup value when they are used. (More than 5 counts is recommended.)

	7	6	5	4	3	2	1	0	
RMCTR5	RMZERO7	RMZERO6	RMZERO5	RMZERO4	RMZERO3	RMZERO2	RMZERO1	RMZERO0	(At reset : 0 0 0 0 0 0 0 0)

RMZERO7	RMZERO6	RMZERO5	RMZERO4	RMZERO3	RMZERO2	RMZERO1	RMZERO0	0 data count setup
-	-	-	-	-	-	-	-	Given value

Tabel 15-2-5 Remote Control Register5 (RMCTR5: x'03FC9')

	7	6	5	4	3	2	1	0	
RMCTR6	RMONE7	RMONE6	RMONE5	RMONE4	RMONE3	RMONE2	RMONE1	RMONE0	(At reset : 0 0 0 0 0 0 0 0)

RMONE7	RMONE6	RMONE5	RMONE4	RMONE3	RMONE2	RMONE1	RMONE0	1 data count setup
-	-	-	-	-	-	-	-	Given value

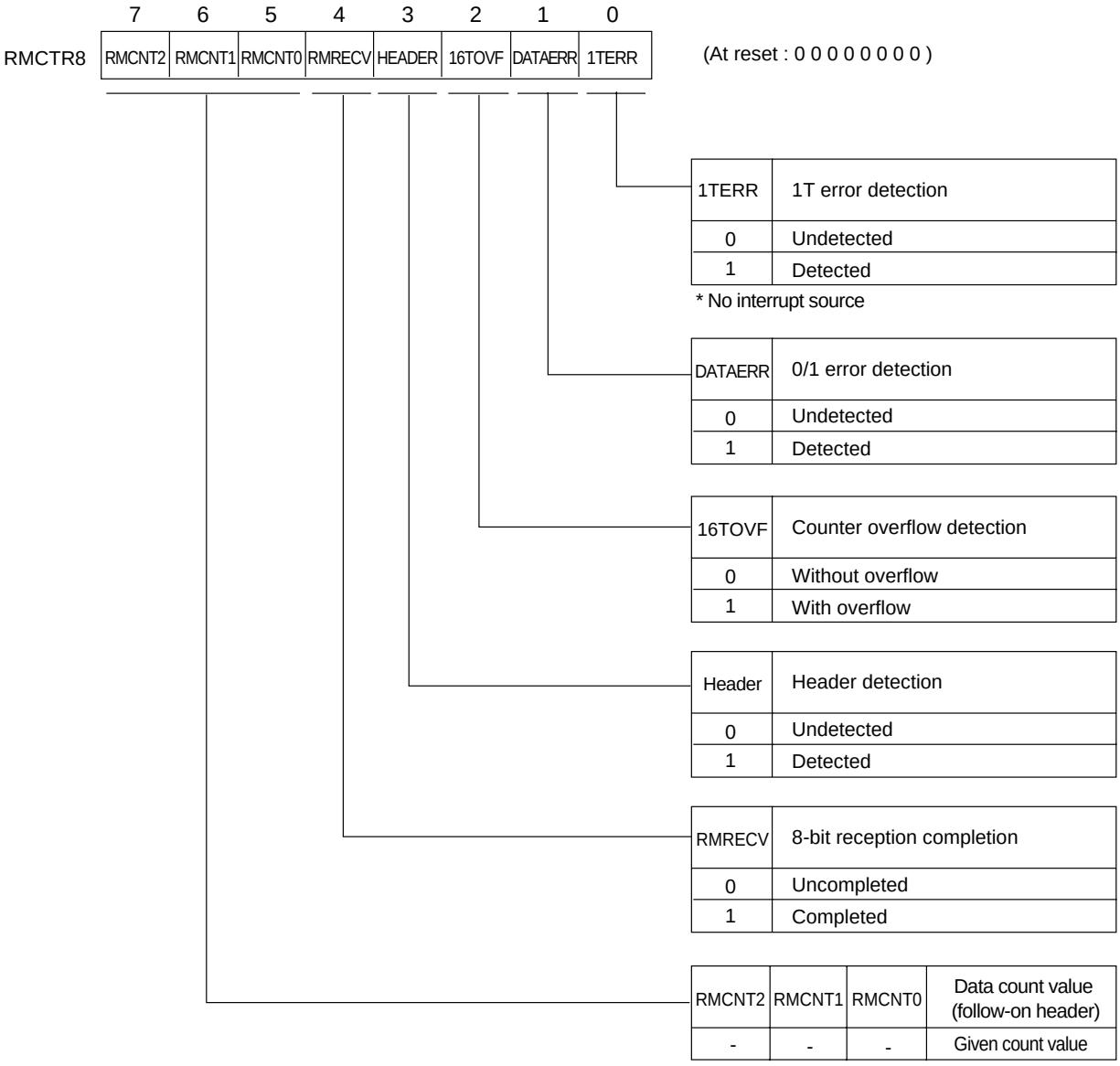
Tabel 15-2-6 Remote Control Register6 (RMCTR6: x'03FCA')

	7	6	5	4	3	2	1	0	
RMCTR7	RMHDD7	RMHDD6	RMHDD5	RMHDD4	RMHDD3	RMHDD2	RMHDD1	RMHDD0	(At reset : 0 0 0 0 0 0 0 0)

RMHDD7	RMHDD6	RMHDD5	RMHDD4	RMHDD3	RMHDD2	RMHDD1	RMHDD0	Header + 8-bit data detection data set
-	-	-	-	-	-	-	-	Given value

Tabel 15-2-7 Remote Control Register7 (RMCTR7: x'03FCB')

Do not set less than 2 counts as the 0 data and 1 data count setup value.
(More than 5 counts is recommended.)


7 6 5 4 3 2 1 0
RMCTR8
RMCNT2 RMCNT1 RMCNT0 RMRECV HEADER 16TOVF DATAERR 1TERR
(At reset : 0 0 0 0 0 0 0 0)
1TERR 1T error detection
0 Undetected
1 Detected
* No interrupt source
DATAERR 0/1 error detection
0 Undetected
1 Detected
16TOVF Counter overflow detection
0 Without overflow
1 With overflow
Header Header detection
0 Undetected
1 Detected
RMRECV 8-bit reception completion
0 Uncompleted
1 Completed
RMCNT2 RMCNT1 RMCNT0 Data count value (follow-on header)
- - - Given count value

Tabel 15-2-8 Remote Control Register8 (RMCTR8: x'03FCC')

Writing optional deta to the RMCTR8 register during remote control reception (when the RMEN flag of the RMCTR2 register is "1") clears 1Terr, DATAERR, 16TOVF, and RMRECV flags. And writing any given deta to the RMCTR8 register when remote control reception is halted (when the RMEN flag of the RMCTR2 register is "0"), clears all the bit of the RMCTR register.

	7	6	5	4	3	2	1	0	
RMDAT1	RMDATS7	RMDATS6	RMDATS5	RMDATS4	RMDATS3	RMDATS2	RMDATS1	RMDATS0	(At reset : X X X X X X X X)

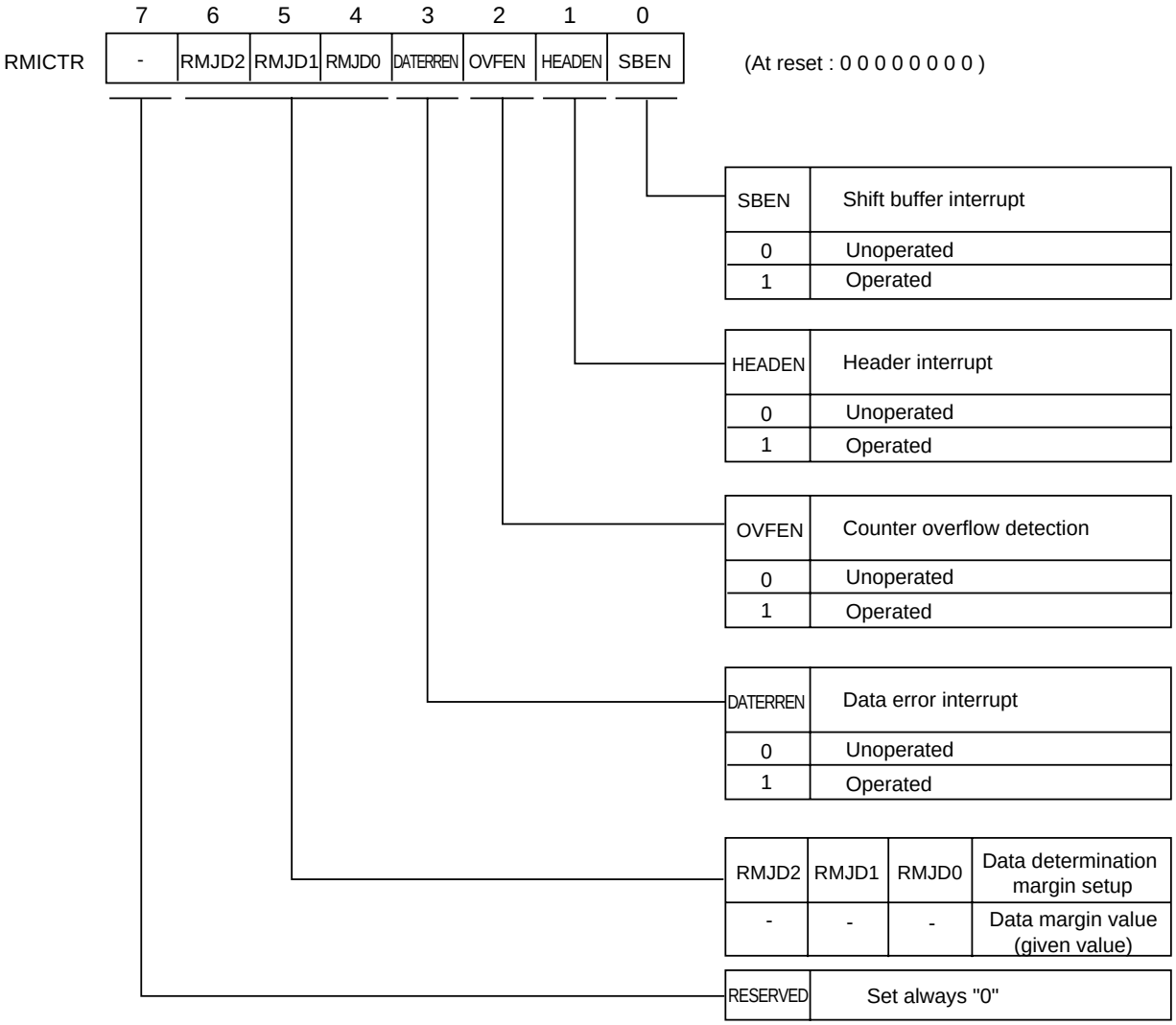
Tabel 15-2-9 Remote Control Shift Data (RMDAT1: x'03FCD')

	7	6	5	4	3	2	1	0	
RMDAT2	RMDATB7	RMDATB6	RMDATB5	RMDATB4	RMDATB3	RMDATB2	RMDATB1	RMDATB0	(At reset : X X X X X X X X)

Tabel 15-2-10 Remote Control Buffer Data (RMDAT2: x'03FCE')

The RMDAT1 register can be cleared manually by writing any given deta to the RMCTR8 register when remote control reception is halted (when the RMEN flag of the RMCTR2 register is "0"). At the same time, the RMCTR8 register is cleared .

RMCTR2 register is cleared after the reading is completed.

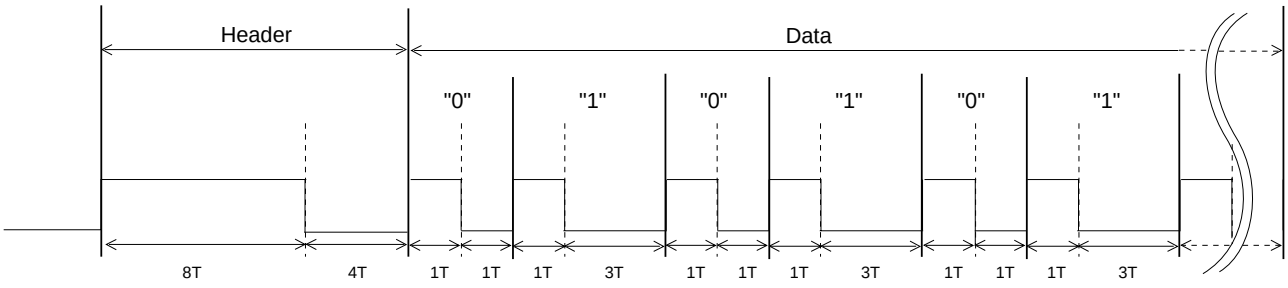

7 6 5 4 3 2 1 0
RMICTR
- RMJD2 RMJD1 RMJD0 DATERREN OVFEN HEADEN SBEN
(At reset : 0 0 0 0 0 0 0 0)
SBEN Shift buffer interrupt
0 Unoperated
1 Operated
HEADEN Header interrupt
0 Unoperated
1 Operated
OVFEN Counter overflow detection
0 Unoperated
1 Operated
DATERREN Data error interrupt
0 Unoperated
1 Operated
RMJD2 RMJD1 RMJD0 Data determination margin setup
- - - Data margin value (given value)
RESERVED Set always "0"

Tabel 15-2-11 Remote Control Interrupt Control Register (RMICTR: x'03FCF')

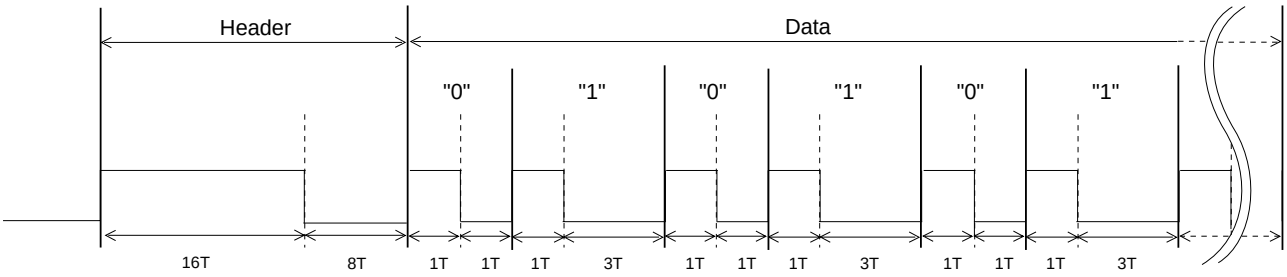
When using the data determination margin function, set different count values to between header "H" and header "L" and to between 0 data, 1 data and 1T data.

15-3 Setup Example

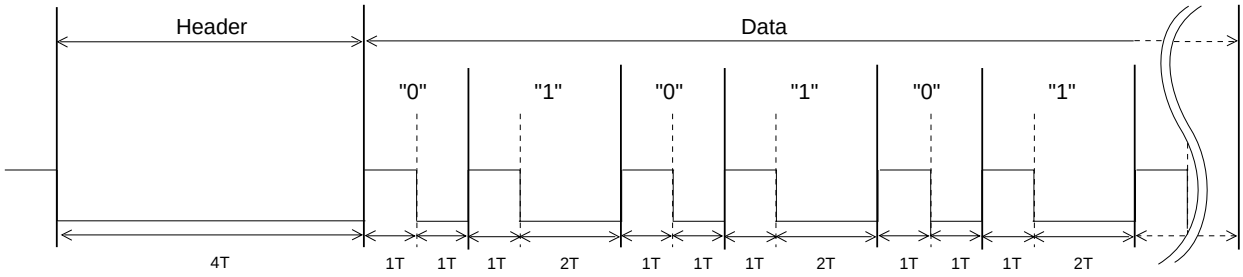
Setup exalples of the remote control reception for 4 waveform formats are shown below.



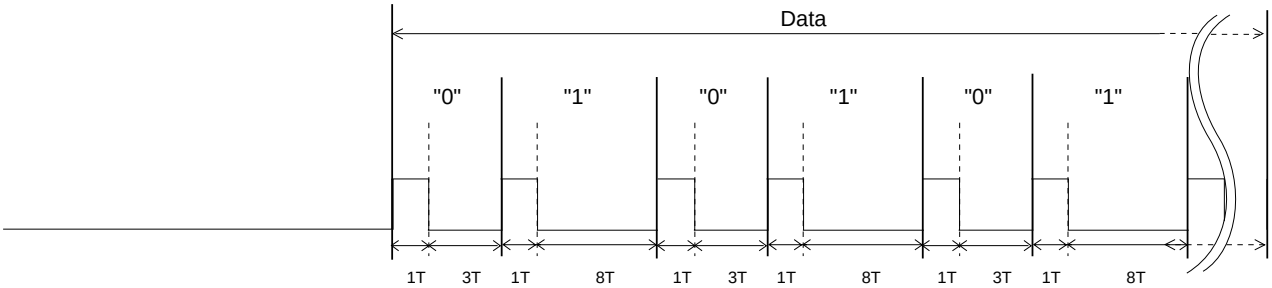
Tabel 15-3-1 Setup example of waveform format 1



Tabel 15-3-2 Setup example of waveform format 2



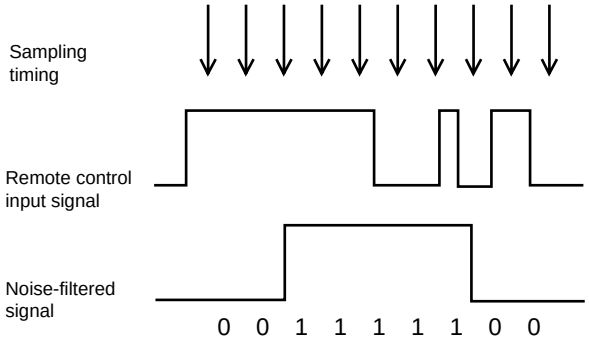
Tabel 15-3-3 Setup example of waveform format 3



Tabel 15-3-4 Setup example of waveform format 4

■Noise filter function (P25)

Signals are input to the remote control pin (P25) and sampled in the setup sample time. If three signals of same level are input consecutively, the level is sent to the internal parts of the LSI. Otherwise, the previous input level is sent. That is, only the signal with amplitude longer than “sampling time x 3 sampling clock” can pass through the noise filter, and signals with shorter amplitude than this are removed.



Tabel 15-3-5 Noise Filter Function

15-3-1 Setup Example 1 (Waveform 1)

■Setup for remote control reception

An example of the setup for the waveform format 1 (Fig. 15-3-1) with descriptions are shown below.

Sampling clock	fosc/2^{10}
Noise filter selection	√
Edge recognition	Both edge
Header setup	√ (1 clock)
Header detection system	Header + 8-bit data
1T count value	11 counts
Header “L” interval count value	44 counts (4T)
Header “H” interval count value	88 counts (8T)
“0” data interval count value	11 counts (1T)
“1” data interval count value	33 counts (3T)
8-bit data for expaneded header detection setup	x’55’
Interrupts	Header interrupt
	Shift buffer interrupt
	Counter overflow interrupt
	Data error interrupt
Data margin setup	3 counts

Setup Procedure	Description
(1) Select the prescaler operation PSCMD (X’3F6F’) bp0 : PSCEN = 1	(1) Set “1” to the PSCEN flag of the PSCMD register to select the prescaler operation.
(2) Select the clock source RMCTR1 (X’3FC5’) bp2-0 : RMCLK2-0 = 101	(2) Set “101” to the RMCLK2-0 flag of the RMCTR1 register to select fosc/2^9 as a sampling clock.
(3) Select the noise filter RMCTR1 (X’3FC5’) bp3 : RMNF = 1	(3) Set “1” to the RMNF flag of the RMCTR1 register to select the noise filter.
(4) Edge recognition RMCTR1 (X’3FC5’) bp4-5 : RMRMD1-0 = 00	(4) Set “00” to the RMRMD1-0 flag of the RMCTR1 register to select both edges interrupt.
(5) Select the header system RMCTR2 (X’3FC6’) bp1-0 : RMHSW1-0 = 10	(5) Set “10” to the RMHSW1-0 flag of the RMCTR2 register to select 1 clock.

Setup Procedure	Description
(6) Select the header detection system RMCTR2 (X'3FC6') bp2 : RMHDEN = 1	(6) Set "1" to the RMHDEN flag of the RMCTR2 register to enable the header + initial 8-bit data detection.
(7) Set the 1T count value RMCTR2 (X'3FC6') bp7-4 : RM1TSW3-0 = X'b'	(7) Set X'b' to the RMTSW3-0 flag of the RMCTR2 register to set 1T count value to be 11.
(8) Set the "L" interval count value RMCTR3 (X'3FC7') bp7-0 : RMHDL7-0 = X'2c'	(8) Set X'2c' to the RMHDL7-0 flag of the RMCTR3 register to set the header "L" interval count value to be 44.
(9) Set the header "H" interval count value RMCTR4 (X'3FC8') bp7-0 : RMHDH7-0 = X'58'	(9) Set X'58' to the RM1HDL7-0 flag of the RMCTR4 register to set the header "H" interval count value to be 88.
(10) Set the "0" data interval count value RMCTR5 (X'3FC9') bp7-0 : RMZER07-0 = X'0b'	(10) Set X'0b' to the RMZER07-0 flag of the RMCTR5 register to set the "0" data interval count value to be 11.
(11) Set the "1" data interval count value RMCTR6 (X'3FCA') bp7-0 : RMONE7-0 = X'21'	(11) Set X'21' to the RMONE7-0 flag of the RMCTR6 register to set the "1" data interval count value to be 33.
(12) Set the header detection data RMCTR7 (X'3FCB') bp7-0 : RMHDD7-0 = X'55'	(12) Set X'55'' to the RMHDD7-0 flag of the RMCTR7 register to set the 8-bit data for header detection.
(13) Set the shift buffer interrupt RMICTR (X'3FCE') bp0 : SBEN = 1	(13) Set "1" to the SBEN flag of the RMICTR register to enable the shift buffer interrupt.
(14) Set the header interrupt RMICTR (X'3FCF') bp1 : HEADEN = 1	(14) Set "1" to the HEADEN flag of the RMICTR register to enable the header detection interrupt.
(15) Set the counter overflow interrupt RMICTR (X'3FCF') bp2 : OVFEN = 1	(15) Set "1" to the OVFEN flag of the RMICTR register to enable the counter overflow interrupt.

Setup Procedure	Description
(16) Set the data error interrupt RMICTR (X'3FCF') bp3 : DATERREN = 1	(16) Set "1" to the DATERREN flag of the RMICTR register to enable the data error detection interrupt.
(17) Set the data detection margin RMICTR (X'3FCF') bp6-4 : RMJD2-0 = 011	(17) Set "011" to the RMJD2-0 flag of the RMICTR register to set the data detection margin to be 3 counts.
(18) Set the interrupt level RMICR (X'3FEE') bp7-6 : RMLV1-0 = 10	(18) Set "10" to the RMLV1-0 flag of the RMICR register to set the remote control interrupt level to be 2.
(19) Enable the Interrupt RMCIR (X'3FEE') bp1 :RMIE = 1	(19) Set "1" to the RMIE flag of the RMICR register to enable the interrupt. If the interrupt request flag (RMIR flag of the RMICR register) is already set, enable the interrupt after clearing the RMIR flag.
(20) Start the remote control reception RMCTR2 (X'3FC6') bp3 :RMEN = 1	(20) Set "1" to the RMEN flag of the RMCTR2 register to start the remote control reception.

15-3-2 Setup Example 2 (Waveform 2)

■Setup for remote control reception

An example of the setup for the waveform format 2 (Fig. 15-3-2) with descriptions are shown below.

Sampling clock	fosc/2^{10}
Noise filter selection	√
Edge recognition	Both edge
Header setup	√ (1 clock)
Header detection system	Header + 8-bit data
1T count value	11 counts
Header “L” interval count value	88 counts (8T)
Header “H” interval count value	176 counts (16T)
“0” data interval count value	11 counts (1T)
“1” data interval count value	33 counts (3T)
8-bit data for expaneded header detection setup	x’55’
Interrupts	Header interrupt
	Shift buffer interrupt
	Counter overflow interrupt
	Data error interrupt
Data margin setup	3 counts

Setup Procedure	Description
(1) Set the prescaler operation PSCMD (X’3F6F’) bp0 : PSCEN = 1	(1) Set “1” to the PSCEN flag of the PSCMD register to select the prescaler operation.
(2) Select the clock source RMCTR1 (X’3FC5’) bp2-0 : RMCLK2-0 = 101	(2) Set “101” to the RMCLK2-0 flag of the RMCTR1 register to select fosc/2^9 as a sampling clock.
(3) Select the noise filter RMCTR1 (X’3FC5’) bp3 : RMNF = 1	(3) Set “1” to the RMNF flag of the RMCTR1 register to select the noise filter.
(4) Edge recognition RMCTR1 (X’3FC5’) bp4-5 : RMRMD1-0 = 00	(4) Set “00” to the RMRMD1-0 flag of the RMCTR1 register to select both edges interrupt.
(5) Select the header system RMCTR2 (X’3FC6’) bp1-0 : RMHSW1-0 = 10	(5) Set “10” to the RMHSW1-0 flag of the RMCTR2 register to select the 1 clock.

Setup Procedure	Description
(6) Select the header detection system RMCTR2 (X'3FC6') bp2 : RMHDEN = 1	(6) Set "1" to the RMHDEN flag of the RMCTR2 register to enable the header + initial 8-bit data detection.
(7) Set the 1T count value RMCTR2 (X'3FC6') bp7-4 : RM1TSW3-0 = X'b'	(7) Set X'b' to the RMTSW3-0 flag of the RMCTR2 register to set 1T count value to be 11.
(8) Set the "L" interval count value RMCTR3 (X'3FC7') bp7-0 : RMHDL7-0 = X'58'	(8) Set X'58' to the RMHDL7-0 flag of the RMCTR3 register to set the header "L" interval count value to be 88.
(9) Set the header "H" interval count value RMCTR4 (X'3FC8') bp7-0 : RMHDH7-0 = X'b0'	(9) Set X'b0' to the RMHDL7-0 flag of the RMCTR4 register to set the header "H" interval count value to be 176.
(10) Set the "0" data interval count value RMCTR5 (X'3FC9') bp7-0 : RMZER07-0 = X'0b'	(10) Set X'0b' to the RMZER07-0 flag of the RMCTR5 register to set the "0" data interval count value to be 11.
(11) Set the "1" data interval count value RMCTR6 (X'3FCA') bp7-0 : RMONE7-0 = X'21'	(11) Set X'21' to the RMONE7-0 flag of the RMCTR6 register to set the "1" data interval count value to be 33.
(12) Set the header detection data RMCTR7 (X'3FCB') bp7-0 : RMHDD7-0 = X'55'	(12) Set X'55'' to the RMHDD7-0 flag of the RMCTR7 register to set 8-bit data for the header detection.
(13) Set the shift buffer interrupt RMICTR (X'3FCE') bp0 : SBEN = 1	(13) Set "1" to the SBEN flag of the RMICTR register to enable the shift buffer interrupt.
(14) Set the header interrupt RMICTR (X'3FCF') bp1 : HEADEN = 1	(14) Set "1" to the HEADEN flag of the RMICTR register to enable the header detection interrupt.
(15) Set the counter overflow interrupt RMICTR (X'3FCF') bp2 : OVFEN = 1	(15) Set "1" to the OVFEN flag of the RMICTR register to enable the counter overflow interrupt.

Setup Procedure	Description
(16) Set the data error interrupt RMICTR (X'3FCF') bp3 : DATERREN = 1	(16) Set "1" to the DATERREN flag of the RMICTR register to enable the data error detection interrupt.
(17) Set the data detection margin RMICTR (X'3FCF') bp6-4 : RMJD2-0 = 011	(17) Set "011" to the RMJD2-0 flag of the RMICTR register to set the data detection margin to be 3 counts.
(18) Set the interrupt level RMICR (X'3FEE') bp7-6 : RMLV1-0 = 10	(18) Set "10" to the RMLV1-0 flag of the RMICR register to set the remote control interrupt level to be 2.
(19) Enable the Interrupt RMICR (X'3FEE') bp1 : RMIE = 1	(19) Set "1" to the RMIE flag of the RMICR register to enable the Interrupt. If the interrupt request flag (RMIR flag of the RMICR register) is already set, enable the interrupt after clearing the RMIR flag.
(20) Start the remote control reception RMCTR2 (X'3FC6') bp3 : RMEN = 1	(20) Set "1" to the RMEN flag of the RMCTR2 register to start the remote control reception.

15-3-3 Setup Example 3 (Waveform 3)

■Setup for remote control reception

An example of the setup for the waveform format 3 (Fig. 15-3-3) with descriptions are shown below.

Sampling clock	fx/2
Noise filter selection	√
Edge recognition	Both edge
Header setting	√ (1/2 clock)
Header detection system	Header only
1T count value	10 counts
Header “L” interval count value	40 counts (4T)
Header “H” interval count value	0 count
“0” data interval count value	10 counts (1T)
“1” data interval count value	20 counts (2T)
8-bit data for expaneded header detection setup	x’ab’
Interrupts	Header interrupt
	Shift buffer interrupt
	Counter overflow interrupt
	Data error interrupt
Data margin setup	4 counts

Setup Procedure	Description
(1) Select the clock source RMCTR1 (X’3FC5’) bp2-0 : RMCLK2-0 = 001	(1) Set “001” to the RMCLK2-0 flag of the RMCTR1 register to select fx/2 as a sampling clock.
(2) Select the noise filter RMCTR1 (X’3FC5’) bp3 : RMNF = 1	(2) Set “1” to the RMNF flag of the RMCTR1 register to select the noise filter.
(3) Edge recognition RMCTR1 (X’3FC5’) bp4-5 : RMRMD1-0 = 00	(3) Set “00” to the RMRMD1-0 flag of the RMCTR1 register to select both edges interrupt.
(4) Select the header system RMCTR2 (X’3FC6’) bp1-0 : RMHSW1-0 = 01	(4) Set “01” to the RMHSW1-0 flag of the RMCTR2 register to select 1/2 clock.
(5) Select the header detection system RMCTR2 (X’3FC6’) bp2 : RMHDEN = 1	(5) Set “0” to the RMHDEN flag of the RMCTR2 register to accept the header detection interrupt with only header data detection.

Setup Procedure	Description
(6) Set the 1T count value RMCTR2 (X'3FC6') bp7-4 : RM1TSW3-0 = X'a'	(6) Set X'a' to the RM1TSW3-0 flag of the RMCTR2 register to set 1T count value to be 10.
(7) Set the "L" interval count value RMCTR3 (X'3FC7') bp7-0 : RMHDL7-0 = X'28'	(7) Set X'28' to the RMHDL7-0 flag of the RMCTR3 register to set the header "L" interval count value to be 40.
(8) Set the header "H" interval count value RMCTR4 (X'3FC8') bp7-0 : RMHDH7-0 = X'00'	(8) Set X'00' to the RMHDL7-0 flag of the RMCTR4 register to set the header "H" interval count value to be invalid.
(9) Set the "0" data interval count value RMCTR5 (X'3FC9') bp7-0 : RMZER07-0 = X'0a'	(9) Set X'0a' to the RMZER07-0 flag of the RMCTR5 register to set the "0" data interval count value to be 10.
(10) Set the "1" data interval count value RMCTR6 (X'3FCA') bp7-0 : RMONE7-0 = X'14'	(10) Set X'14' to the RMONE7-0 flag of the RMCTR6 register to set the "1" data interval count value to be 20.
(11) Set the shift buffer interrupt RMICTR (X'3FCF') bp0 : SBEN = 1	(11) Set "1" to the SBEN flag of the RMICTR register to enable the shift buffer interrupt.
(12) Set the header interrupt RMICTR (X'3FCF') bp1 : HEADEN = 1	(12) Set "1" to the HEADEN flag of the RMICTR register to enable the header detection interrupt.
(13) Set the counter overflow interrupt RMICTR (X'3FCF') bp1 : OVFEN = 1	(13) Set "1" to the OVFEN flag of the RMICTR register to enable the counter overflow interrupt.
(14) Set the data error interrupt RMICTR (X'3FCF') bp3 : DATEREEN = 1	(14) Set "1" to the DATEREEN flag of the RMICTR register to enable the data error interrupt.
(15) Set the data detection margin RMICTR (X'3FCF') bp6-4 : RMJD2-0 = 100	(15) Set "100" to the RMJD2-0 flag of the RMICTR register to set the data detection margin to be 4 counts.

Setup Procedure	Description
(16) Set the interrupt level RMICR (X'3FEE') bp7-6 : RMLV1-0 = 10	(16) Set "10" to the RMLV1-0 flag of the RMICR register to set the remote control interrupt level to be 2.
(17) Enable the Interrupt RMICR (X'3FEE') bp1 : RMIE = 1	(17) Set "1" to the RMIE flag of the RMICR register to enable the remote control reception interrupt. If the interrupt request flag (RMIR flag of the RMICR register) is already set, enable the interrupt after clearing the RMIR flag.
(18) Start the remote control reception RMCTR2 (X'3FC6') bp3 : RMEN = 1	(18) Set "1" to the RMEN flag of the RMCTR2 register to start the remote control reception.

15-3-4 Setup Example 4 (Waveform 4)

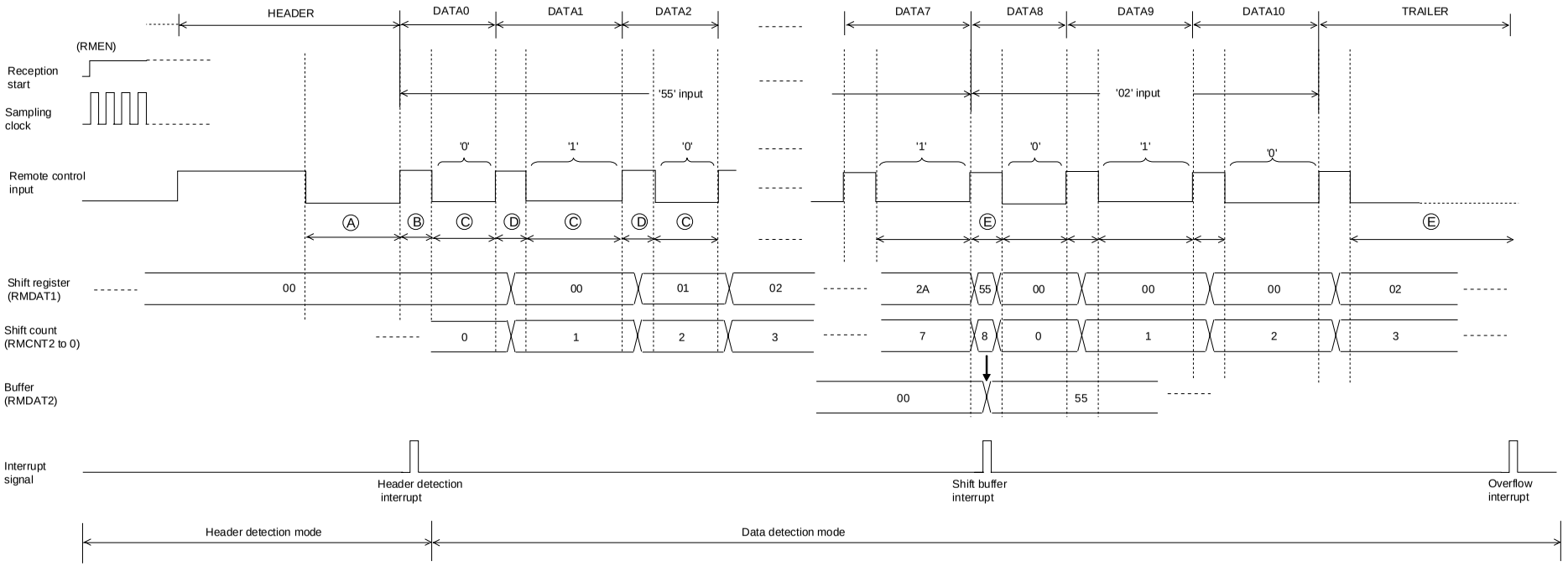
■Setup for remote control reception

An example of the setup for the waveform format 4 (Fig. 15-3-4) with descriptions are shown below.

Sampling clock	fx
Noise filter selection	√
Edge recognition	Rising edge
Header setting	–
1T count value	9 counts (1T)
“0” data interval count value	27counts (3T)
“1” data interval count value	72 counts (8T)
Interrupts	
	Shift buffer interrupt
	Counter overflow interrupt
	Data error interrupt
Data margin setup	0 count

Setup Procedure	Description
(1) Select the clock source RMCTR1 (X’3FC5’) bp2-0 : RMCLK2-0 = 000	(1) Set “00” to the RMCLK2-0 flag of the RMCTR1 register to select fx as a sampling clock.
(2) Select the noise filter RMCTR1 (X’3FC5’) bp3 : RMNF = 1	(2) Set “1” to the RMNF flag of the RMCTR1 register to select the noise filter.
(3) Edge recognition RMCTR1 (X’3FC5’) bp4-5 : RMRMD1-0 = 01	(3) Set “01” to the RMRMD1-0 flag of the RMCTR1 register to select both edges interrupt.
(4) Select the header system RMCTR2 (X’3FC6’) bp1-0 : RMHSW1-0 = 00	(4) Set “00” to the RMHSW1-0 flag of the RMCTR2 register to select no header.
(5) Set the 1T count value RMCTR2 (X’3FC6’) bp7-4 : RM1TSW3-0 = X’9’	(5) Set X’9’ to the RM1TSW3-0 flag of the RMCTR2 register to set 1T count value to be 9.

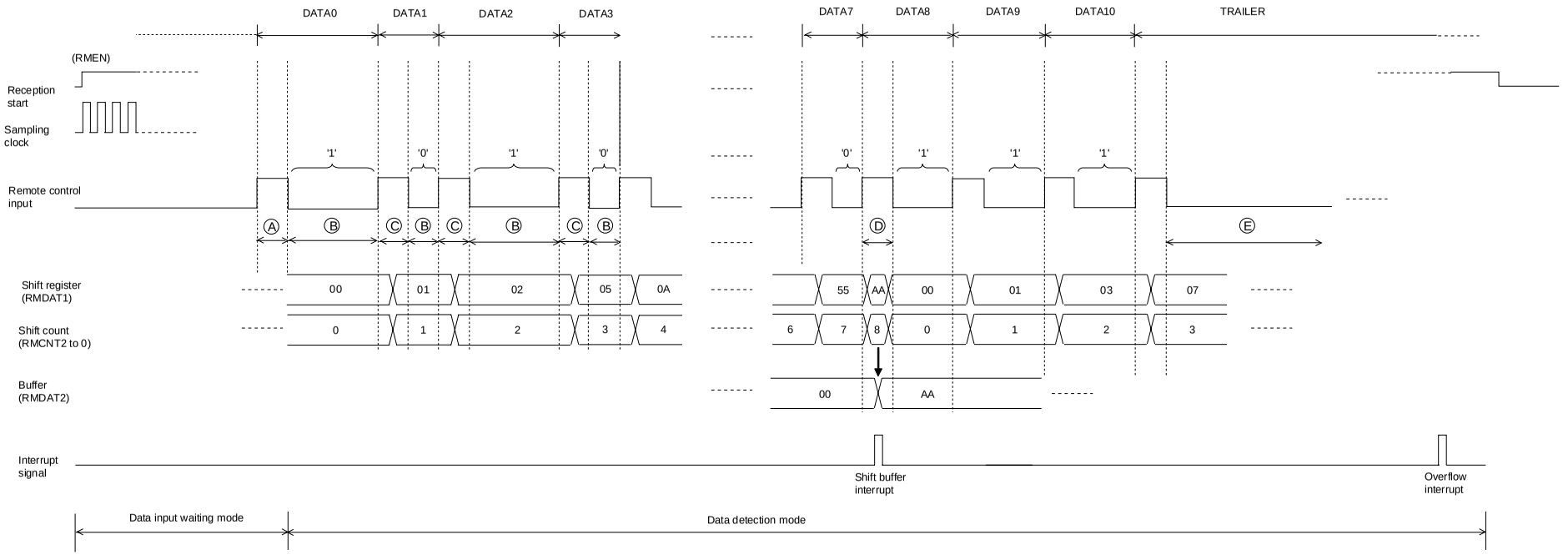
Setup Procedure	Description
(6) Set the "0" data interval count value RMCTR5 (X'3FC9') bp7-0 : RMZER07-0 = X'1b'	(6) Set X'1b' to the RMZER07-0 flag of the RMCTR5 register to set the "0" data interval count value to be 27.
(7) Set the "1" data interval count value RMCTR6 (X'3FCA') bp7-0 : RMONE7-0 = X'48'	(7) Set X'48' to the RMONE7-0 flag of the RMCTR6 register to set the "1" data interval count value to be 72.
(8) Set the shift buffer interrupt RMICTR (X'3FCF') bp0 : SBEN = 1	(8) Set "1" to the SBEN flag of the RMICTR register to enable the shift buffer interrupt.
(9) Set the counter overflow interrupt RMICTR (X'3FCF') bp2 : OVFEN = 1	(9) Set "1" to the OVFEN flag of the RMICTR register to enable the counter overflow interrupt.
(10) Set the data error interrupt RMICTR (X'3FCF') bp3 : DATEREEN = 1	(10) Set "1" to the DATEREEN flag of the RMICTR register to enable the data error interupt.
(11) Set the data detection margin RMICTR (X'3FCF') bp6-4 : RMJD2-0 = 100	(11) Set "000" to the RMJD2-0 flag of the RMICTR register to set the data detection margin to be 0 count.
(12) Set the interrupt level RMICR (X'3FEE') bp7-6 : RMLV1-0 = 10	(12) Set "10" to the RMLV1-0 flag of the RMICR register to set the remote control interrupt level to be 2.
(13) Enable the Interrupt RMICR (X'3FEE') bp1 : RMIE = 1	(13) Set "1" to the RMIE flag of the RMICR register to accept the interrupt. If the interrupt request flag (RMIR flag of the RMICR register) is already set, enable the interrupt after clearing the RMIR flag.
(14) Start the remote control reception RMCTR2 (X'3FC6') bp3 : RMEN = 1	(14) Set "1" to the RMEN flag of the RMCTR2 register to start the remote control reception.



A), B) interval : Operate header detection and output interrupt signal in B) interval.
C) Interval : Operate 1T detection (1T error flag is put if no error is detected).
D) Interval : Operate data determination and input the data to the shift register, ("1" is input if error data is detected), at the same time, number of shift is coutnted.
E) Interval : Data in the shift register is transferred to the buffer when the count number reaches 8, and shift buffer interrupt is occured.
At the same time, shift register is cleared, and the buffer is cleared after it is read out.
F) Interval : Overflow interrupt is occured when the binary counter in the remote control reception circuit counts up to 255
If the data is shorter than 8-bit, the data is left in the shift register.

Note : Set the sampling clock in such a way that the count number per interval is more than 3
If overflow interrupt is set in header detection mode, overflow interrupt could be occurred before the header detection.

Figure 15-3-6 Setup Example of Header Format 1 to 3



A) interval : Start the data detection.
B) interval : Operate 1T detection and output interrupt signal.
C) interval : Operate data detection (1T error flag is put if no error is detected).
D) interval : Operate data determination and input the data to the shift register ("1" is input if error data is detected), at the same time, number of shifts is counted.
E) interval : Data in the shift register is transferred to the buffer when the count number reaches 8, and shift buffer interrupt is occured.
At the same time, shift register is cleared, and the buffer is cleared after it is read out.
F) interval : Overflow interrupt is occured when the binary counter in the remote control reception circuit counts up to 255.
If the data is shorter than 8-bit, the data is left in the shift register.

Note : Set the sampling clock in such a way that the count number per interval is more than 3.
If overflow interrupt is set in header detection mode, overflow interrupt could be occurred before the header detection.

Figure 15-3-7 Setup Example 4 without Header Format

Remote control input settup time				
Example	Header	1T	"1" data	"0" data
1	3.5 ms	0.44 ms	1.31 ms	1T
2	9.0 ms	0.56 ms	1.69 ms	1T
3	2.4 ms	0.6 ms	1.2 ms	1T
4	-	0.264 ms	2.1 ms	0.786 ms

Count setup examples (count number)					
fx (32 kHZ, T=31.25 μs)	Example 1	112.0	14.1	41.9	1T
	Example 2	288.0	17.9	54.1	1T
	Example 3	76.8	19.2	38.4	1T
	Example 4	-	8.4	67.2	25.2
fx/2 (16 kHZ, T=62.5 μs)	Example 1	56.0	7.0	21.0	1T
	Example 2	144.0	9.0	27.0	1T
	Example 3	38.4	9.6	19.2	1T
	Example 4	-	4.2	33.6	12.6
fx/4 (8 kHZ, T=125.0 μs)	Example 1	28.0	3.5	10.5	1T
	Example 2	72.0	4.5	13.5	1T
	Example 3	19.2	4.8	9.6	1T
	Example 4	-	2.1	16.8	6.3
fx/8 (4 kHZ, T=250.0 μs)	Example 1	14.0	1.8	5.2	1T
	Example 2	36.0	2.2	6.8	1T
	Example 3	9.6	2.4	4.8	1T
	Example 4	-	1.1	8.4	3.1
fx/16 (2 kHZ, T=500.0 μs)	Example 1	7.0	0.9	2.6	1T
	Example 2	18.0	1.1	3.4	1T
	Example 3	4.8	1.2	2.4	1T
	Example 4	-	0.5	4.2	1.6
fx/32 (1 kHZ, T=1000.0 μs)	Example 1	3.5	0.4	1.3	1T
	Example 2	9.0	0.6	1.7	1T
	Example 3	2.4	0.6	1.2	1T
	Example 4	-	0.3	2.1	0.8
fx/64 (0.5 kHZ, T=2000.0 μs)	Example 1	1.8	0.2	0.7	1T
	Example 2	4.5	0.3	0.8	1T
	Example 3	1.2	0.3	0.6	1T
	Example 4	-	0.1	1.1	0.4
$fosc/2^{9}$ (39.06 kHZ, T=25.60 μs)	Example 1	136.7	17.2	51.2	1T
	Example 2	351.6	21.9	66.0	1T
	Example 3	93.8	23.4	46.9	1T
	Example 4	-	10.3	82.0	1T
$fosc/2^{10}$ (19.53 kHZ, T=51.20 μs)	Example 1	68.4	8.6	25.6	1T
	Example 2	175.8	10.9	33.0	1T
	Example 3	46.9	11.7	23.4	1T
	Example 4	-	5.2	41.0	15.4
$fosc/2^{11}$ (9.77 kHZ, T=102.40 μs)	Example 1	34.2	4.3	12.8	1T
	Example 2	87.9	5.5	16.5	1T
	Example 3	23.4	5.9	11.7	1T
	Example 4	-	2.6	20.5	7.7
$fosc/2^{12}$ (4.88 kHZ, T=204.80 μs)	Example 1	17.1	2.1	6.4	1T
	Example 2	43.9	2.7	8.3	1T
	Example 3	11.7	2.9	5.9	1T
	Example 4	-	1.3	10.3	3.8
$fosc/2^{13}$ (2.44 kHZ, T=409.60 μs)	Example 1	8.5	1.1	3.2	1T
	Example 2	22.0	1.4	4.1	1T
	Example 3	5.9	1.5	2.9	1T
	Example 4	-	0.6	5.1	1.9
$fosc/2^{14}$ (1.22 kHZ, T=819.2 μs)	Example 1	4.3	0.5	1.6	1T
	Example 2	11.0	0.7	2.1	1T
	Example 3	2.9	0.7	1.5	1T
	Example 4	-	0.3	2.6	1.0
$fosc/2^{15}$ (0.61 kHZ, T=1638.4 μs)	Example 1	2.1	0.3	0.8	1T
	Example 2	5.5	0.3	1.0	1T
	Example 3	1.5	0.4	0.7	1T
	Example 4	-	0.2	1.3	0.5

Tabel 15-3-8 Remote Control Input Time Setting and Count Number

16-1 Overview

In the memory expansion mode, or the processor mode, the AC timing of the control signal to the external connected device can be changed by the software. This function can set each of the AC timing of the data strobe signal (p51/NRE) at reading and the data strobe signal (p50/NWE) at writing independently. The setup time and the hold time are set to the AC timing control register (ACTMD) by the software.

■AC Timing Control Register (ACTMD)

	7	6	5	4	3	2	1	0
ACTMD	WTSUP1	WTSUP0	WTHLD1	WTHLD0	RDSUP1	RDSUP0	RDHLD1	RDHLD0

(At reset : 0 0 0 0 0 0 0 0)

RDHLD1	RDHLD0	2 bits field that specify the hold time at reading
0	0	No expanded cycle
	1	fs/2 × (+1)cycle expanded
1	0	fs/2 × (+2)cycle expanded
	1	fs/2 × (+3)cycle expanded

RDSUP1	RDSUP0	2 bits field that specify the setup time at reading
0	0	No expanded cycle
	1	fs/2 × (+1)cycle expanded
1	0	fs/2 × (+2)cycle expanded
	1	fs/2 × (+3)cycle expanded

WTHLD1	WTHLD0	2 bits field that specify the hold time at writing
0	0	No expanded cycle
	1	fs/2 × (+1)cycle expanded
1	0	fs/2 × (+2)cycle expanded
	1	fs/2 × (+3)cycle expanded

WTSUP1	WTSUP0	2 bits field that specify the setup time at writing
0	0	No expanded cycle
	1	fs/2 × (+1)cycle expanded
1	0	fs/2 × (+2)cycle expanded
	1	fs/2 × (+3)cycle expanded

Figure 16-1-1 AC Timing Control Register (ACTMD : x'03F06', R/W)

16-2 Operation

16-2-1 Setup

■AC Timing Setup

AC timing variable function can set each of the timing of the data strobe signal (p51/NRE) at reading, and the data strobe signal (p50/NWE) at writing independently. The setup time and the hold time are set to the AC timing control register (ACTMD) by the software.

The AC timing control register (ACTMD) has 4 fields that set the setup time and the hold time at reading (the cycle for reading data from the external device) and, at writing (the cycle for writing data to the external device).

WTSUP : 2 bits field that specify the setup time at writing.
WTHLD : 2 bits field that specify the hold time at writing.
RDSUP : 2 bits field that specify the setup time at reading.
RDHLD : 2 bits field that specify the hold time at reading.

On each field, the expanded cycle count is specified with 1 unit : a half cycle of system clock (fs). "The set value of field" and "the expanded cycle count" are shown on figure 16-1-1.

■Caution 1 on AC Timing Variable Function

When AC timing variable function is used, the external wait count set by the memory control register (MEMCTR) should be set longer than "the setup time + the hold time", both at reading and at writing. If the external wait count is set shorter than "the setup time + the hold time", the setup time and the hold time set by the ACTMD register, are not valid.

Set the external wait count of the memory control register (MEMCTR) longer than "the setup time + the hold time".

The external wait count ≥ WTSUP + WTHLD
The external wait count ≥ RDSUP + RDHLD

■Caution 2 on AC Timing Variable Function

When the hand shake mode is specified with the memory control register (MEMCTR), AC timing variable function can not be operated. At hand shake mode, even if the setup time and the hold time are set, AC timing variable function is not valid and the operation is at normal hand shake mode. Use it at the fixed wait mode.

At hand shake mode, AC timing variable function cannot be used.
Select the fixed wait mode.

■Caution 3 on AC Timing Variable Function

The hold time at reading, set by RDHLD, is valid only for the output waveform of the data strobe signal to the external device. This is not used for the timing of storing data inside microcontroller. In microcontroller, the reading data is latched at the same timing as the hold time is set to "0", regardless of the ACTMD register setup.

RDHLD should be "x'00", and the hold time at reading should not be set, except when the special signal control is needed at the external device. And when the special signal control needs to be operated using the RDHLD setup, the system design should be done with calculation of the operation inside the microcontroller.

The hold time (RDHLD) should be always set to "x'00"', unless the special signal control needs to be operated.

16-2-2 Operation

■AC Timing Features of Data Strobe Signal

AC timing of data strobe signal that sets the setup time and the hold time to the external device with AC timing variable function, is shown as follows.

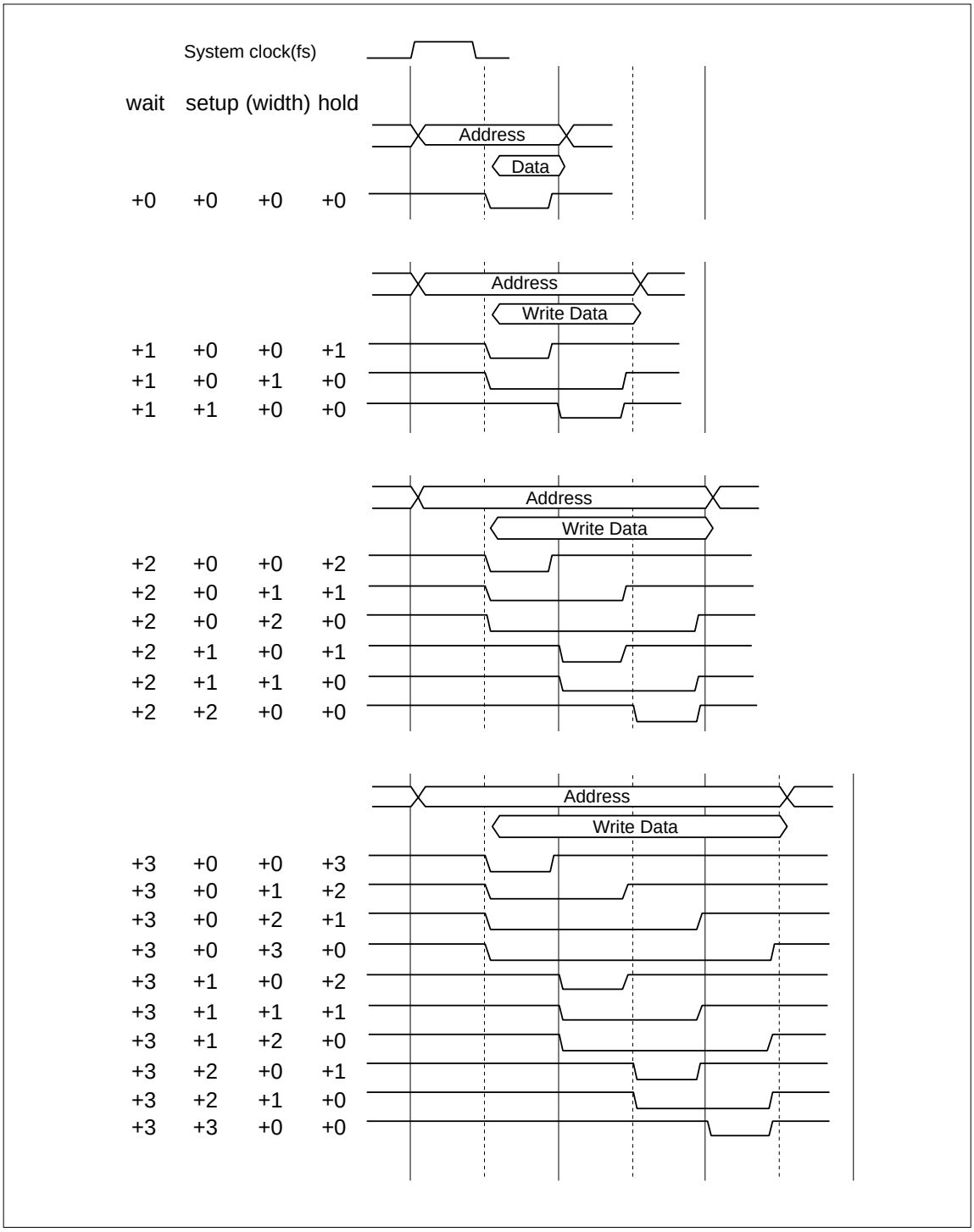


Figure 16-2-1 AC Timing Features of Data Strobe Signal

The values in figure 16-2-1 are the expanded cycle counts as 1 unit is a half cycle of system clock (fs). "Wait" means the external wait count specified with the memory control register (MEMCTR), "Setup" means the setup time at reading or writing, "hold" means the expanded cycle of the hold time.

16-2-3 Setup Example

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the external wait count. MEMCTR (x'3F01') bp3 : EXWH = 1 bp1-0 : EXW1-0 = wait count	(1) Set the wait count by the EXW1-0 flag of the MEMCTR register. At this time, set the EXWH flag to "1", and select the fixed wait mode. [☞ Chapter 2. 2-3-2 Control Registers]
(2) Set the ACTMD register. bp7-6 : WTSUP1-0 bp5-4 : WTHLD1-0 bp3-2 : RDSUP1-0 bp1-0 : RDHLD1-0 = x'00'	(2) Set the setup time and the hold time by the ACTMD register. Normally, set the hold time (RDHLD) at reading to x'00'. The set timing is valid from the next cycle after writing the setup value to the ACTMD register is completed.

17-1 Overview

17-1-1 Overview

The MN101CF57D is equivalent to MN101C57D except its Mask ROM is substituted with 64 KB of Flash EEPROM.

The MN101CF57D is programmed in one of two modes;
PROM writer mode, which uses a dedicated PROM writer for a microcontroller's stand-alone programming. Onboard programming mode, which the CPU controls programming of a microcontroller on a target board.

■ **User program area (64 KB : #0x'04000' to #0x'13FFF')**
･This area stores an user program. It is overwritten in both programming modes.

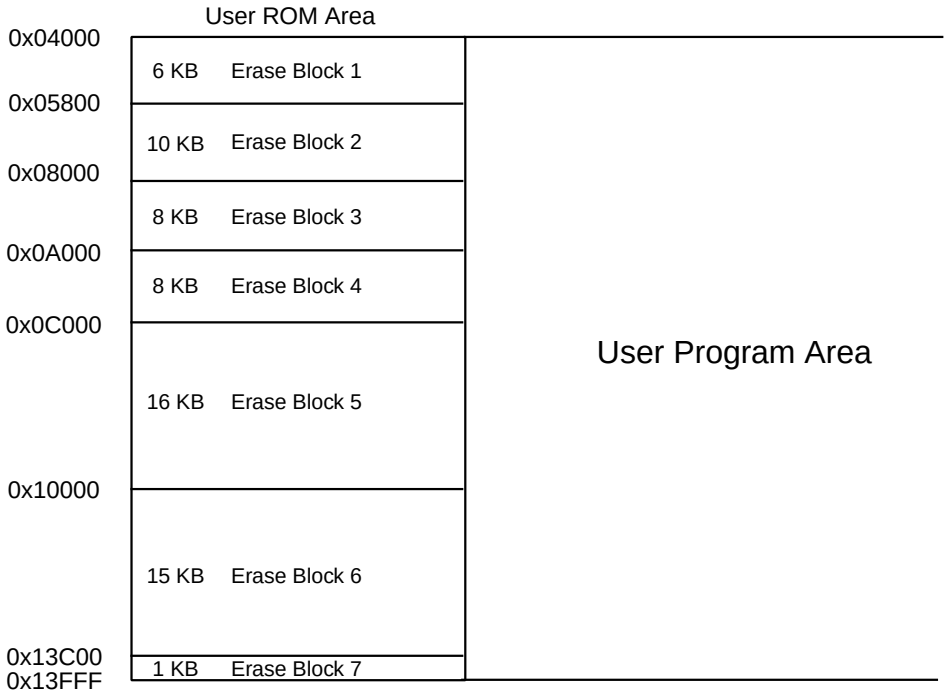


Figure 17-1-1 Memory Map of Internal Flash EEPROM

1 cycle of "erase-write" process is counted as 1 programming in every block.
That is, when several blocks are programmed one-time separately, programming count is added by just the number of programming cycle. (For instance, when block 1 and 2 are programmed separately, 2 program count is added.)
Therefore, program several blocks together to reduce the programming count.

17-1-2 Differences between Mask ROM version and Flash EEPROM version

Table 17-1-1 shows differences between 8-bit microcontroller MN101C57X (Mask ROM version) and MN101CF57D (Flash EEPROM version).

Table 17-1-1 Differences between Mask ROM version and Flash EEPROM version

<table>
<tr><th></th><th>Mask ROM version (MN101C57X)</th><th>Flash EEPROM version (MN101CF57D)</th></tr>
<tr><td>Operation voltage</td><td>2.0 V to 5.5 V (at 1.00 µs/2 MHz)
2.2 V to 5.5 V (at 500 µs/4.19 MHz)
2.0 V to 5.5 V (at 125 µs/32.768 kHz)</td><td>2.5 V to 5.5 V (at 1.00 µs/2 MHz)
2.5 V to 5.5 V (at 500 µs/4.19 MHz)
2.5 V to 5.5 V (at 125 µs/32.768 kHz)</td></tr>
<tr><td>Pin DC characteristics</td><td colspan="2">I/O currents, input judge levels are the same</td></tr>
<tr><td>Oscillation characteristics</td><td colspan="2">Matching evaluation of each oscillator is necessary
when these versions are rotated for mass production</td></tr>
<tr><td>Noise characteristics</td><td colspan="2">Noise evaluation of each version is necessary
when they are rotated for mass production</td></tr>
<tr><td rowspan="2">Power pin condition</td><td rowspan="2">V_{DD} pins are short-circuit
(17 pin, 19 pin and 39 pin)</td><td>In normal operation:
V_{DD} pins are short-circuit
(17 pin, 19 pin and 39 pin)</td></tr>
<tr><td>In on board programming:
V_{DD1}(19 pin), V_{DD2}(17 pin)
V_{PP}(39 pin)</td></tr>
</table>

Refer to [Chapter 17 17-3-2 Circuit Requirements for the Target Board] for the details.

17-2 PROM Writer Programming Mode

In PROM writer mode, the CPU is halted for Internal flash EEPROM to be programed. Use the dedicated adaptor socket, which connects to the dedicated PROM writer. When the mocrocontroller connects to the adaptor socket, it automatically enters PROM writer mode.

Matching information of the dedicated writer is posted on our Website;
http://www.semicon.panasonic.co.jp/micom/index.html

Select the adapter socket depending on your programming writer and the package type.

Programming writer	P/N
Ando model	TE101-CF57D100

■Fixing a device in the adapter socket and the position of the No.1 pin.

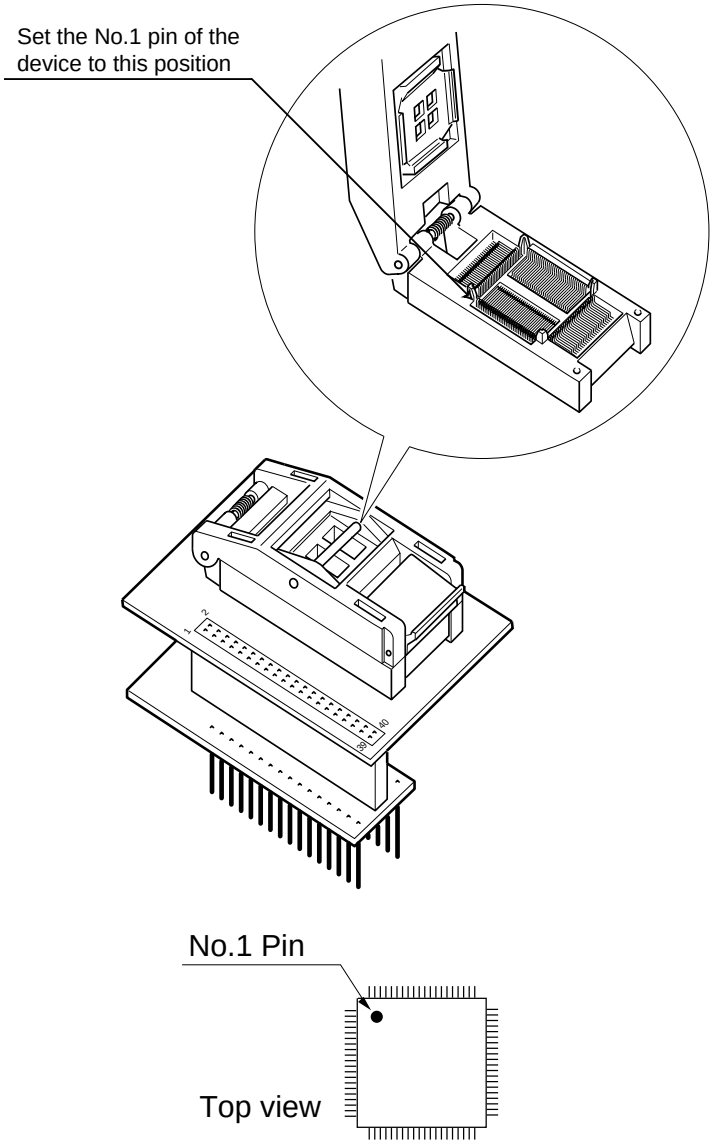


Table 17-2-1 Fixing a Device on the Adapter Socket and the Position of No.1 Pin

17-3 Onboard Serial Programming Mode

17-3-1 Overview

The onboard serial programming mode is primarily used to program the flash EEPROM in devices that are already installed on a PCB board with internal serial interface. Use the dedicated serial writer for programming controlled by the load program. In this mode, load program is write/erase-protected in the hardware.

■Hardware and software requirements
Hardware and software products required for onboard serial programming are as follows.

Hardware requirements
・Onboard serial writer
・Flash programming connectors or pins for target board.

Software requirements
・Load program installed in the internal flash EEPROM
(Loading must be completed with PROM writer before the MN101CF57Ds is installed on a PCB board. Standard onboard serial programming writer comes with load program.)
・Programming algorithm for operating onboard serial writer

■Built-in hardware for onboard serial programming mode
Use this LSI's serial interface 0 as a standard serial writer for programming the flash EEPROM in onboard serial programming mode.
[☞ Chapter 11 Serial Interface 0]

Serial interface I/O pins (SBT0B, SBI0B, SBO0B) used for onboard serial programming should be reserved as dedicated pins to prevent other user circuits from communicating with the device. Altenatively, design your target board to be capable of normal communication with serial writer.

■Onboard serial programming writer
The onboard serial programming writer is compatible with following model. The load program can be downloaded from the following Website.

YDC model: AF220/AF200 flash microcontroller programmer
http://www.ydc.co.jp/micom/product/download_impressE.htm

17-3-2 Circuit Requirements for the Target Board

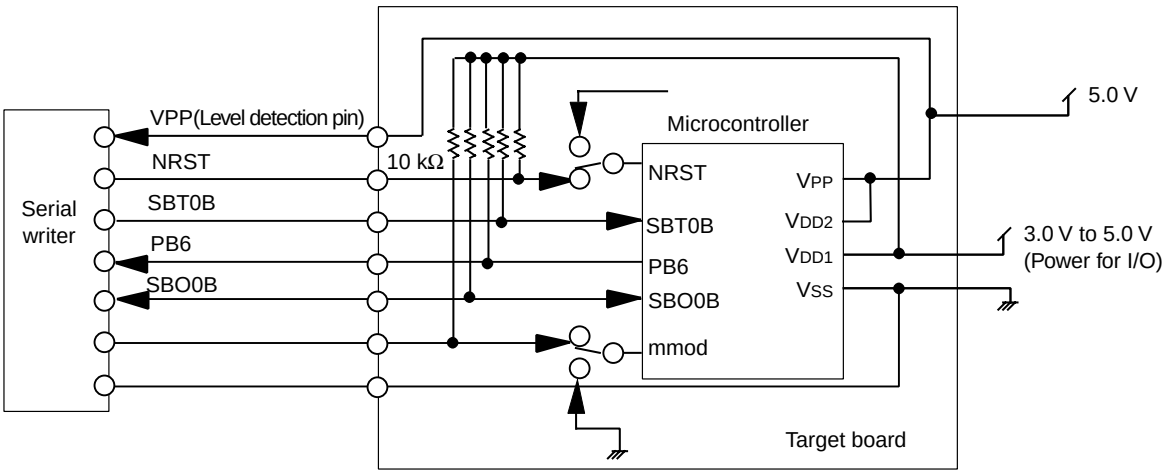


Figure 17-3-1 Circuit Requirements for the Target Board

Pins

- ●V_{DD1}(19 pin) : 3.0 V to 5.0 V power supply (for I/O)
- ●V_{DD2}(17 pin) : 5.0 V Power supply (for flash EEPROM and internal circuits)
- ●V_{PP}(39 pin) : V_{PP} level detection pin for target board
- ●NRST(18 pin) : Reset
- ●SBT0B(57 pin) : Clock supply pin for serial interface
- ●SBO0B(55 pin) : Data input pin for serial interface
- ●GND(11 pin) : Ground
- ●PB6(56 pin) : Busy signal output pin
- ●mmod(14 pin) : mmod pin (in user mode: L, in onboard programming mode: H)

・V_{PP} and V_{DD2} pins must supply 5.0 V from external power supply.
V_{PP} and V_{DD2} should be supplied within the range of 4.5 V ≤ (V_{PP} = V_{DD2}) ≤ 5.5 V.
When V_{DD} level is too low (under 5.0 V), serial writer generates error message.

・Connect pull-up resistors on the target board to NRST, mmod, SBT0B, SB00B and PB6 pins, which are connected to the power supply. The resistance value should be 10 kΩ ± 1 kΩ.

・Install a switch on the target board to toggle between NRST, mmod for serial programming and NRST, mmod for normal opeation. Alternatively, install a wired-OR connection. (For a wired-OR connection, disable NRST, mmod for normal operation during serial programming)

・NRST pin is output from the serial writer through an open connection.

・SBT0B, SB00B and PB6 pins should be reserved as dedicated pin for serial writer to prevent other user circuits on the target board from communicating with the device. Alternatively, design your target board on which the serial writer can program the device correctly.

・It is vital to take your target board design into consideration, such as to increase the signal capacity for serial writer, to prevent noise from interfering with operation of the Mask ROM.

17-3-3 Hardware Requirements for Onboard Programming

(1) Interface

This LSI contains following hardwares for serial interface programming of the flash EEPROM.

●8-bit serial interface : 1 pc
(used with serial interface 0)
· Data transmission/reception through external clock
·Transfer bit LSB first
· Clock speed can be selected from among 500 kbps, 250 kbps, 125 kbps and 62.5 kbps

●I/O pins : 3 pins
· SBT0B, SBI 0B and SBO0B pins for serial interface. These pins also serve as I/O pins.

(1) Interface block diagram

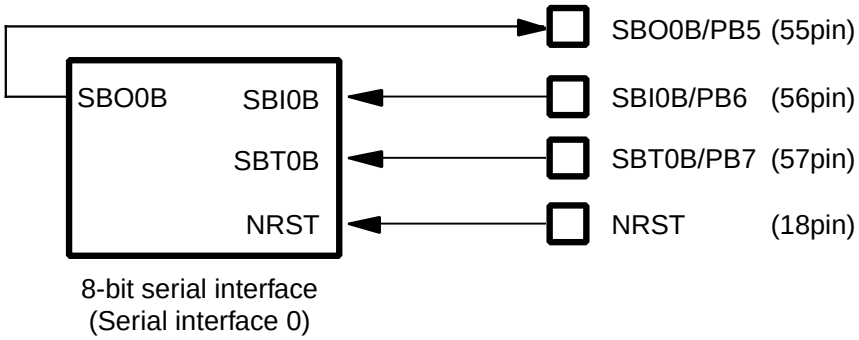


Figure 17-3-2 Interface block diagram

When programming the memory, you need not be aware of these microcontroller hardware connections. However, serial interface I/O pins (SBT0B, SBI0B, SBO0B) used for onboard serial programming [☞ 17-3-3. Target Board Circuits for On-board Serial Interface Programming] should be reserved as dedicated pins to prevent other user circuits from communicating with the device. Altenatively, design your target board to be capable of normal communication with serial writer.

17-3-4 Memory Map of Microcontroller used in Onboard Programming

■User program area

・This area stores an user program.

RAM address space

Address	Size	
0x00000 | 0x006FF	1792 bytes	Serial writer working area
0x00700 | 0x007FF	256 bytes	Reserved area

■Serial writer working area

・This 1792 bytes area starting from address 0x00000 is used as serial writer working area. Download an operation program that drives serial programming from load program to this area for onboard serial programming.

・Users need not be aware of the RAM address space.

17-3-5 Microcontroller clock on the target board

· For the clock supply to the microcontroller on the target board, use the existing target board clock. Therefore, each user uses different oscillator frequency for the microcontroller clock.
· Following table shows maximum / minimum rating of the oscillator frequency for the microcontroller clock.

Clock frequency	Operating voltage	
	$V_{DD}1$	$V_{DD}2$
2 MHz ≤ fosc ≤ 20 MHz	5 V	5 V
2 MHz ≤ fosc ≤ 8.38 MHz	3 V	5 V

17-4 Programming Flow

Figure 17-4-1 shows the flow for reprogramming (erasing and programming) the flash EEPROM.

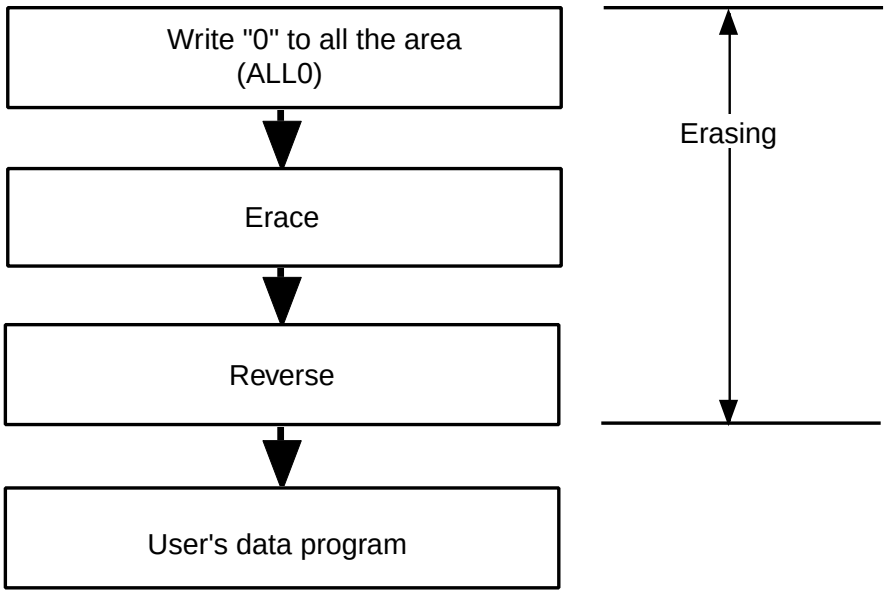


Figure 17-4-1 Reprogramming Flow of Internal Flash EEPROM

Erase the data of flash EEPROM before programming as shown in this flowchart.
The erase routine consists of three steps, first writing all zeros (x'00') to the entire memory space, next erasing the memory, and finally reversing, which is executed when bit is over-erased.

17-5 Probe Switches

17-5-1 PRB-MBB101C57-M

- This probe must be used with the following boards.
  - Connector board : PX-CN101-M
  - MBB board : PRB-MBB101C57M
  - Adapter board : PRB-ADP101-100-M
  - Dummy target : PRB-DMY101C57-M

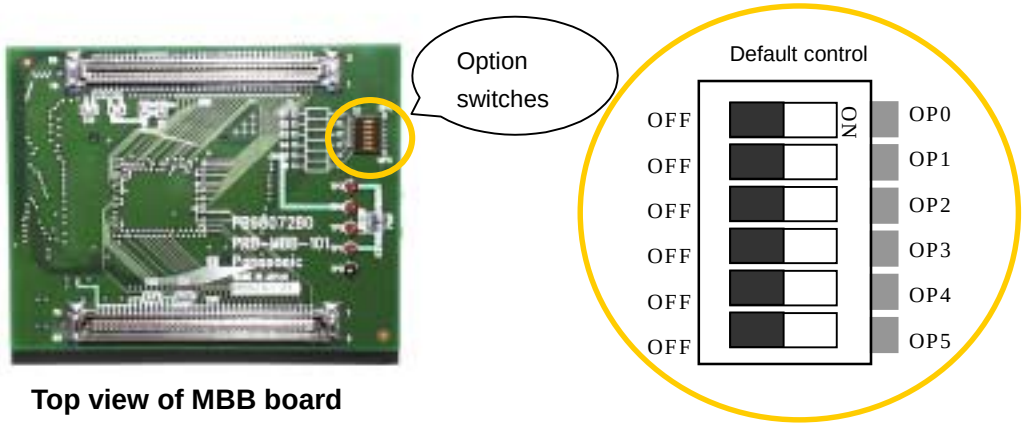
    The dummy target should be connected when ICE is operated independently, the adapter board should be connected at connection to the target.
- This probe is mounted the switches for mask option.

  The setting of the switches shown below.

Table 1.Table of setting option switches.

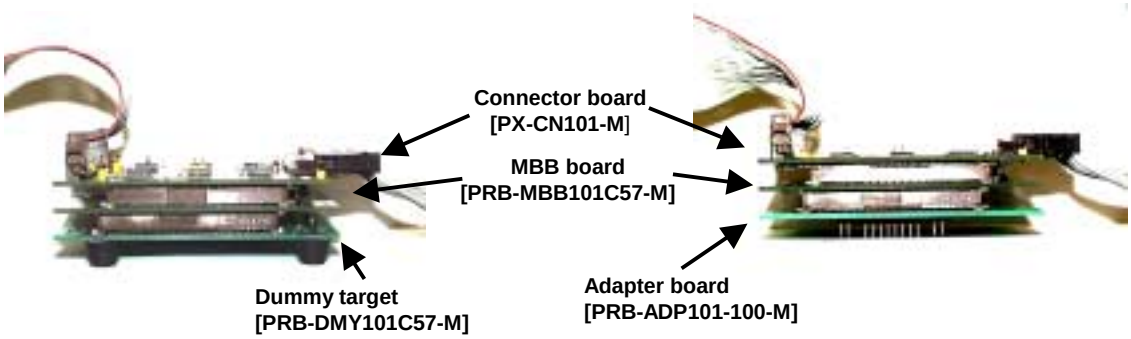
OP Number	ON	OFF
OP0	no operation	
OP1	no operation	
OP2	no operation	
OP3	no operation	
OP4	Reset by the software at watchdog timer generation	Reset by NMI (by the hardware) at watch dogtimer generation
OP5	no operation	

Figure 1. Layout of option switches



Top view of MBB board

Figure 2.Composition with PRB-MBB101C57-M



- When ICE is operated independently.

- At connection to the target

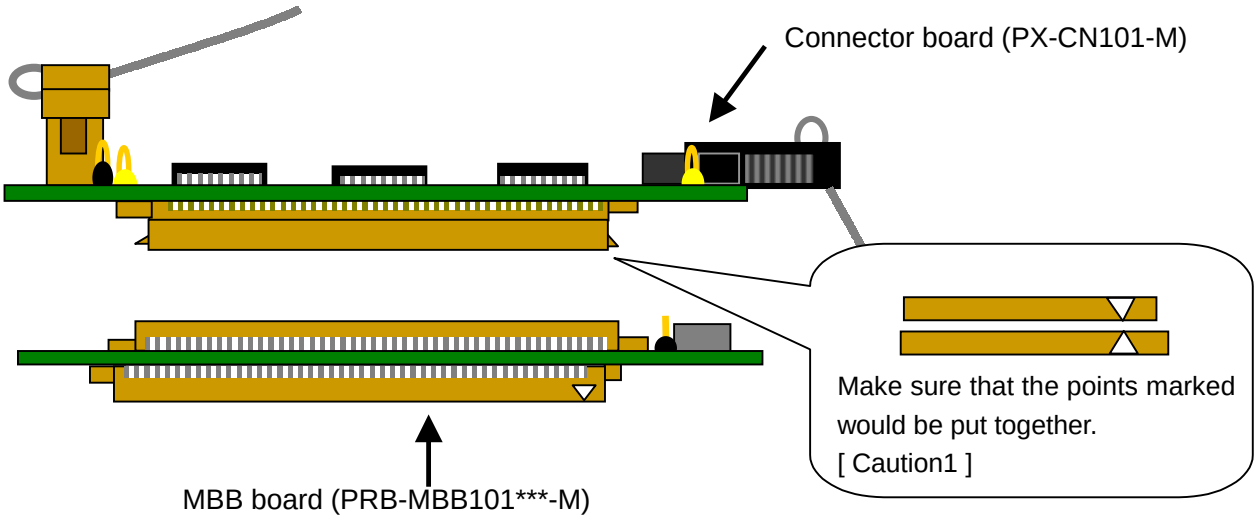
17-5-2 PX-CN101-M

This board can be used for any MBB models(product No.PRB-MBB101***-M) of MN101 series.
(Please visit our website for the latest information on the product.)

Figure1. PX-CN101-M Layout

< How to connect >

Figure2. Connecting a PX-CN101-M to a MBB board



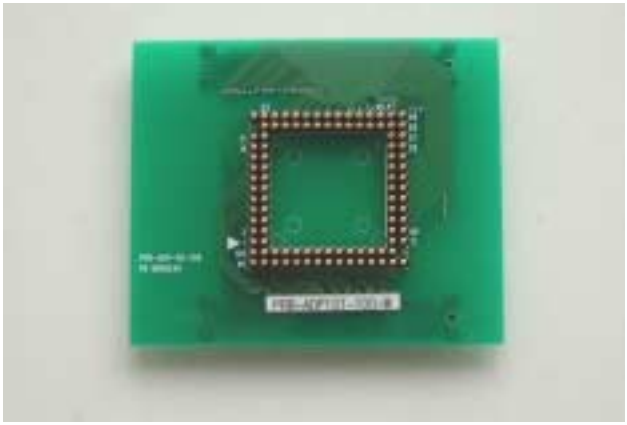
[Caution1]
Connect CNC of PX-CN101-M to CNC of PRB-MBB101***-M, and
CND of PX-CN101-M to CND of PRB-MBB101***-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

17-5-3 PRB-ADP101-100-M

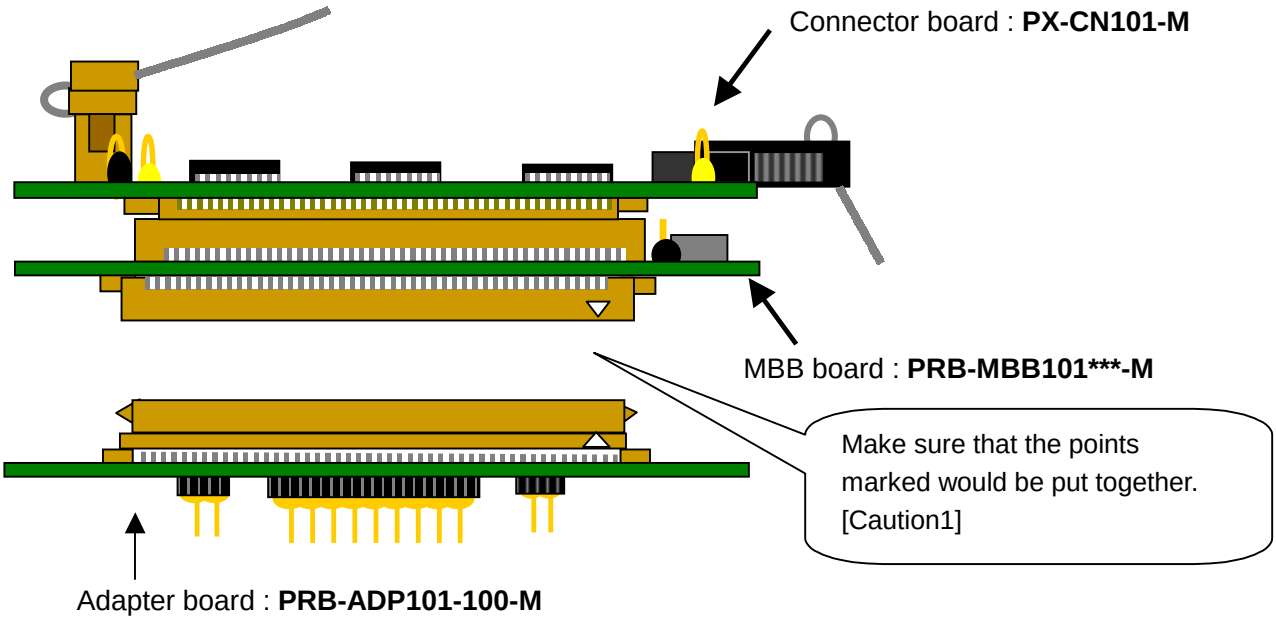
When connected to the target, use this board with MBB board.
This board can be used with the following boards.
(The product type is subject to change without prior notice. The latest information should be confirmed on our web site.)
- PRB-MBB101C57-M

Improper matching may cause any damage to the ICE.

Figure 1. Adapter Board Layout



< How to connect >


Connector board : PX-CN101-M
MBB board : PRB-MBB101***-M
Make sure that the points marked would be put together. [Caution1]
Adapter board : PRB-ADP101-100-M

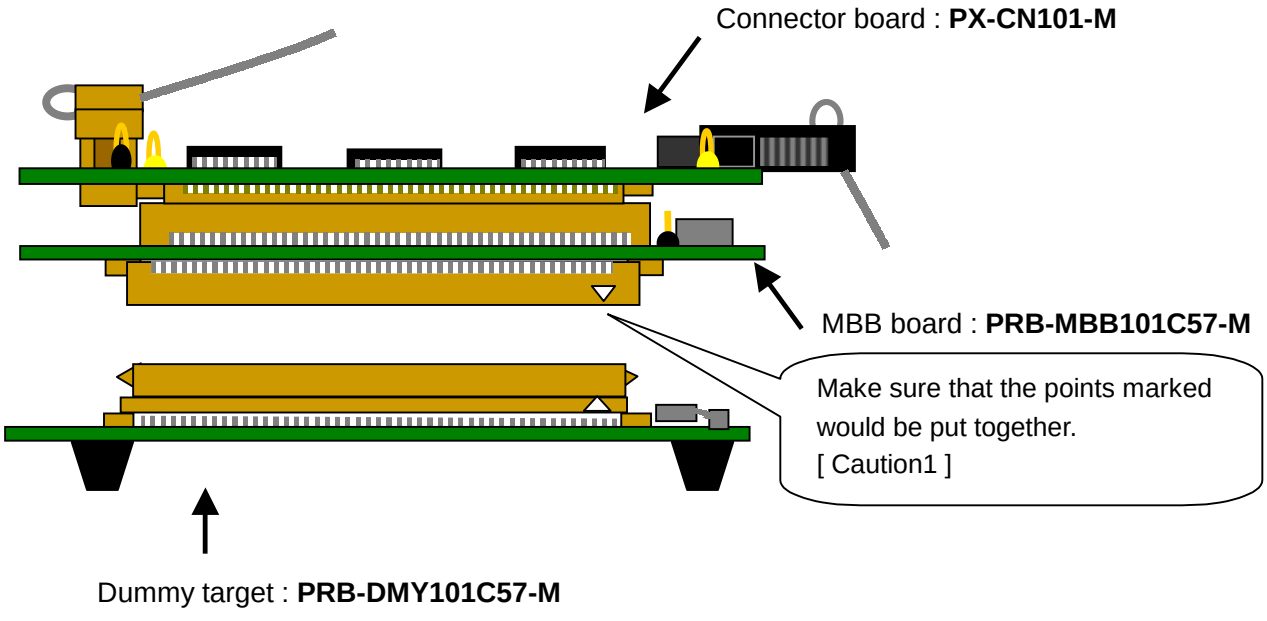
[Caution1]
Connect CNE of PRB-MBB101***-M to CNE of PRB-ADP101-100-M, and
CNF of PRB-MBB101***-M to CNF of PRB-ADP101-100-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

17-5-4 PRB-DMY101C57-M

Dummy target boards differ depending upon the models. This board can be used for only MN101C57 100pin.
When unconnected to the target, use this board with the PRB-MBB101C57-M.
Improper matching may cause any damage to the ICE

Figure 1. PRB-DMY101C57-M Layout

< How to connect >


Connector board : PX-CN101-M
MBB board : PRB-MBB101C57-M
Make sure that the points marked would be put together.
[Caution1]
Dummy target : PRB-DMY101C57-M

[Caution1]
Connect CNE of PRB-MBB101C57-M to CNE of PRB-DMY101C57-M, and
CNF of PRB-MBB101C57-M to CNF of PRB-DMY101C57-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

17-6 Special Function Registers List

Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F00'	CPUM	RESERVED	OSCSEL1	OSCSEL0	OSCDBL	STOP	HALT	OSC1	OSC0	II-24, 28
		0	1	1	0	0	0	0	0	
		Set always to "0"	Division Rate Setup		Internal System Clock Setup	STOP mode Setup	HALT mode Setup	Oscillation Control		
X'3F01'	MEMCTR	IOW1	IOW0	IVBM	EXMEM	EXMEH	IRWE	EXW1	EXW0	II-17
		1	1	0	0	1	0	1	1	
		I/O Wait Setup		Interrupt Vector Address	Memory Switching	Weight Switching	Software Write Setup	Fixed Weight Setup		
X'3F02'	WDCTR	-	-	RESERVED	RESERVED	RESERVED	WDTS1	WDTS0	WDEN	IX-3
		-	-	0	0	0	1	1	0	
				Set always to "0"			Watchdog Time-out Period Setup		WDT Activation	
X'3F03'	DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-	II-33 X-3
		0	0	0	0	0	1	-	-	
		P6 Output Selection	Buzzer Output Frequency Setup			Oscillation Stabilization Wait Cycle Setup				
X'3F06'	ACTMD	WTSUP1	WTSUP0	WTHLD1	WTHLD0	RDSUP1	RDSUP0	RDHLD1	RDHLD0	XVI-2
		0	0	0	0	0	0	0	0	
		Write Setup time Selection		Write Hold time Selection		Read Setup Time Selection		Read Hold Time Selection		
X'3F0E'	EXADV	EXADV3	EXADV2	EXADV1	-	-	-	-	-	II-18 IV-25, 47
		0	0	0	-	-	-	-	-	
		Address Pin Setup at Memory Expansion Mode								
X'3F10'	P0OUT	-	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0	IV-7
		-	X	X	X	X	X	X	X	
			Port 0 Output Data							
X'3F11'	P1OUT	-	-	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	IV-14
		-	-	X	X	X	X	X	X	
				Port 1 Output Data						
X'3F12'	P2OUT	P2OUT7	-	-	-	-	-	-	-	IV-19
		1	-	-	-	-	-	-	-	
		Port 2 Output Data								
X'3F13'	P3OUT	-	P3OUT6	P3OUT5	P3OUT4	P3OUT3	P3OUT2	P3OUT1	P3OUT0	IV-22
		-	X	X	X	X	X	X	X	
			Port 3 Output Data							
X'3F14'	P4OUT	P4OUT7	P4OUT6	P4OUT5	P4OUT4	P4OUT3	P4OUT2	P4OUT1	P4OUT0	IV-30
		X	X	X	X	X	X	X	X	
		Port 4 Output Data								
X'3F15'	P5OUT	-	-	-	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0	IV-35
		-	-	-	X	X	X	X	X	
					Port 5 Output Data					
X'3F16'	P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	IV-41
		X	X	X	X	X	X	X	X	
		Port 6 Output Data								
X'3F17'	P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	IV-45
		X	X	X	X	X	X	X	X	
		Port 7 Output Data								
X'3F18'	P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	IV-50
		X	X	X	X	X	X	X	X	
		Port 8 Output Data								
X'3F19'	P9OUT	-	-	-	-	P9OUT3	P9OUT2	P9OUT1	P9OUT0	IV-54
		-	-	-	-	X	X	X	X	
						Port 9 Output Data				
X'3F1A'	PAOUT	PAOUT7	PAOUT6	PAOUT5	PAOUT4	PAOUT3	PAOUT2	PAOUT1	PAOUT0	IV-58
		X	X	X	X	X	X	X	X	
		Port A Output Data								

Note) x : Initial value is unstable. - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F1B'	PBOUT	PBOUT7	PBOUT6	PBOUT5	PBOUT4	PBOUT3	PBOUT2	PBOUT1	PBOUT0	IV-62
		X	X	X	X	X	X	X	X	
		Port B Output Data								
X'3F1E'	P4SYO	P4SYO7	P4SYO6	P4SYO5	P4SYO4	P4SYO3	P4SYO2	P4SYO1	P4SYO0	IV-31
		0	0	0	0	0	0	0	0	
		Port 4 Synchronous Output Control								
X'3F20'	P0IN	-	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0	IV-7
		-	X	X	X	X	X	X	X	
			Port 0 Input Data							
X'3F21'	P1IN	-	-	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	IV-14
		-	-	X	X	X	X	X	X	
				Port 1 Input Data						
X'3F22'	P2IN	-	-	P2IN5	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0	IV-19
		-	-	X	X	X	X	X	X	
				Port 2 Input Data						
X'3F23'	P3IN	-	P3IN6	P3IN5	P3IN4	P3IN3	P3IN2	P3IN1	P3IN0	IV-22
		-	X	X	X	X	X	X	X	
			Port 3 Input Data							
X'3F24'	P4IN	P4IN7	P4IN6	P4IN5	P4IN4	P4IN3	P4IN2	P4IN1	P4IN0	IV-30
		X	X	X	X	X	X	X	X	
		Port 4 Input Data								
X'3F25'	P5IN	-	-	-	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0	IV-35
		-	-	-	X	X	X	X	X	
					Port 5 Input Data					
X'3F26'	P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	IV-41
		X	X	X	X	X	X	X	X	
		Port 6 Input Data								
X'3F27'	P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	IV-45
		X	X	X	X	X	X	X	X	
		Port 7 Input Data								
X'3F28'	P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	IV-50
		X	X	X	X	X	X	X	X	
		Port 8 Input Data								
X'3F29'	P9IN	-	-	-	-	P9IN3	P9IN2	P9IN1	P9IN0	IV-54
		-	-	-	-	X	X	X	X	
						Port 9 Input Data				
X'3F2A'	PAIN	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	IV-58
		X	X	X	X	X	X	X	X	
		Port A Input Data								
X'3F2B'	PBIN	PBIN7	PBIN6	PBIN5	PBIN4	PBIN3	PBIN2	PBIN1	PBIN0	IV-62
		X	X	X	X	X	X	X	X	
		Port B Input Data								
X'3F2E'	FLOAT	SC0SEL	PARDWN	P1RDWN	P0RDWN	-	-	SYOEVS1	SYOEVS0	IV-8, 16, 31,59 IX-8
		0	0	0	0	-	-	0	0	
		Serial 0 I/O pin selection	PA pull-up/ down resistor selection	P1 pull-up/ down resistor selection	P0 pull-up/ down resistor selection			P4 Synchronous Output Event Selection		
X'3F2F'	P1OMD	-	-	P1OMD5	P1OMD4	P1OMD3	P1OMD2	P1OMD1	P1OMD0	IV-15
		-	-	0	0	0	0	0	0	
				I/O Port, Timer8 Timer7 Output Selection	I/O Port, Timer7 Output Selection	I/O Port, Timer3 Output Selection	I/O Port, Timer2 Output Selection	I/O Port, Timer1 Output Selection	I/O Port, Timer0 Output Selection	
X'3F30'	P0DIR	-	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0	IV-7
		-	0	0	0	0	0	0	0	
			Port0 I/O Direction Control							

Note) x : Initial value is unstable. - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F31'	P1DIR	-	-	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	IV-14
		-	-	0	0	0	0	0	0	
		Port1 I/O Direction Control								
X'3F33'	P3DIR	-	P3DIR6	P3DIR5	P3DIR4	P3DIR3	P3DIR2	P3DIR1	P3DIR0	IV-22
		-	0	0	0	0	0	0	0	
		Port 3 I/O Direction Control								
X'3F34'	P4DIR	P4DIR7	P4DIR6	P4DIR5	P4DIR4	P4DIR3	P4DIR2	P4DIR1	P4DIR0	IV-30
		0	0	0	0	0	0	0	0	
		Port 4 I/O Direction Control								
X'3F35'	P5DIR	-	-	-	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0	IV-35
		-	-	-	0	0	0	0	0	
		Port 5 I/O Direction Control								
X'3F36'	P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	IV-41
		0	0	0	0	0	0	0	0	
		Port 6 I/O Direction Control								
X'3F37'	P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	IV-45
		0	0	0	0	0	0	0	0	
		Port 7 I/O Direction Control								
X'3F38'	P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	IV-50
		0	0	0	0	0	0	0	0	
		Port 8 I/O Direction Control								
X'3F39'	P9DIR	-	-	-	-	P9DIR3	P9DIR2	P9DIR1	P9DIR0	IV-54
		-	-	-	-	0	0	0	0	
		Port 9 I/O Direction Control								
X'3F3A'	PADIR	PADIR7	PADIR6	PADIR5	PADIR4	PADIR3	PADIR2	PADIR1	PADIR0	IV-58
		0	0	0	0	0	0	0	0	
		Port A I/O Direction Control								
X'3F3B'	PBDIR	PBDIR7	PBDIR6	PBDIR5	PBDIR4	PBDIR3	PBDIR2	PBDIR1	PBDIR0	IV-58
		0	0	0	0	0	0	0	0	
		Port B I/O Direction Control								
X'3F3C'	PAIMD	PAIMD7	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0	IV-58
		0	0	0	0	0	0	0	0	
		Port A I/O Port, Analog input pin Selection								
X'3F3D'	PBIMD	PBIMD7	PBIMD6	PBIMD5	PBIMD4	PBIMD3	PBIMD2	PBIMD1	PBIMD0	IV-62
		0	0	0	0	0	0	0	0	
		Port B I/O Port, Analog input pin Selection								
X'3F3E'	P4IMD	IRQ4SEL	-	-	-	P4KYEN3	P4KYEN2	P4KYEN1	P4KYEN0	III-50
		0	-	-	-	0	0	0	0	
		IRQ4 Interrupt Source Selection				P47,46 KEY Interrupt Selection	P45,44 KEY Interrupt Selection	P43,42 KEY Interrupt Selection	P41,40 KEY Interrupt Selection	
X'3F3F'	P5OMD	-	-	-	-	P5OMD3	P5OMD2	P5OMD1	P5OMD0	IV-36
		-	-	-	-	0	0	0	0	
						I/O Port, Timer 8 Output Selection	I/O Port, Timer 2 Output Selection	I/O Port, Timer 7 Output Selection	I/O Port, Timer 0 Output Selection	
X'3F40'	P0PLUD	-	P0PLUD6	P0PLUD5	P0PLUD4	P0PLUD3	P0PLUD2	P0PLUD1	P0PLUD0	IV-7
		-	0	0	0	0	0	0	0	
		Port 0 Pull-up/Pull-down Control								
X'3F41'	P1PLUD	-	-	P1PLUD5	P1PLUD4	P1PLUD3	P1PLUD2	P1PLUD1	P1PLUD0	IV-14
		-	-	0	0	0	1	1	0	
		Port 1 Pull-up/Pull-down Resistors Selection								
X'3F42'	P2PLU	-	-	P2PLU5	P2PLU4	P2PLU3	P2PLU2	P2PLU1	P2PLU0	IV-19
		-	-	0	0	0	0	0	0	
		Port 2 Pull-up Resistors Selection								

Note) x : Initial value is unstable. - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F43'	P3PLU	-	P3PLU6	P3PLU5	P3PLU4	P3PLU3	P3PLU2	P3PLU1	P3PLU0	IV-22
		-	0	0	0	0	0	0	0	
		Port 3 Pull-up Resistors Selection								
X'3F44'	P4PLU	P4PLU7	P4PLU6	P4PLU5	P4PLU4	P4PLU3	P4PLU2	P4PLU1	P4PLU0	IV-30
		0	0	0	0	0	0	0	0	
		Port 4 Pull-up Resistors Selection								
X'3F45'	P5PLU	-	-	-	P5PLU4	P5PLU3	P5PLU2	P5PLU1	P5PLU0	IV-35
		-	-	-	0	0	0	0	0	
		Port 5 Pull-up Resistors Selection								
X'3F46'	P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	IV-41
		0	0	0	0	0	0	0	0	
		Port 6 Pull-up Resistors Selection								
X'3F47'	P7PLU	P7PLU7	P7PLU6	P7PLU5	P7PLU4	P7PLU3	P7PLU2	P7PLU1	P7PLU0	IV-45
		0	0	0	0	0	0	0	0	
		Port 7 Pull-up Resistors Selection								
X'3F48'	P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	IV-50
		0	0	0	0	0	0	0	0	
		Port 8 Pull-up Resistors Selection								
X'3F49'	P9PLU	-	-	-	-	P9PLU3	P9PLU2	P9PLU1	P9PLU0	IV-54
		-	-	-	-	0	0	0	0	
		Port 9 Pull-up Resistors Selection								
X'3F4A'	PAPLUD	PAPLUD7	PAPLUD6	PAPLUD5	PAPLUD4	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	IV-58
		0	0	0	0	0	0	0	0	
		Port A Pull-up/Pull-down Resistors Selection								
X'3F4B'	PBPLU	PBPLU7	PBPLU6	PBPLU5	PBPLU4	PBPLU3	PBPLU2	PBPLU1	PBPLU0	IV-62
		0	0	0	0	0	0	0	0	
		Port B Pull-up Resistors Selection								
X'3F4D'	P0IMD	-	-	P0KYEN5	P0KYEN4	P0KYEN3	P0KYEN2	P0KYEN1	P0KYEN0	III-49
		-	-	0	0	0	0	0	0	
				P05 Key Interrupt Selection	P04 Key Interrupt Selection	P03 Key Interrupt Selection	P02 Key Interrupt Selection	P01 Key Interrupt Selection	P00 Key Interrupt Selection	
X'3F4F'	P5LED	-	-	-	P5LED4	P5LED3	P5LED2	P5LED1	P5LED0	IV-37
		-	-	-	0	0	0	0	0	
		Port 5 Large Current Drive Control								
X'3F50'	TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	IV-9
		X	X	X	X	X	X	X	X	
		Timer 0 Binary Counter								
X'3F51'	TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	IV-9
		X	X	X	X	X	X	X	X	
		Timer 1 Binary Counter								
X'3F52'	TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	IV-8
		X	X	X	X	X	X	X	X	
		Timer 0 Compare Register								
X'3F53'	TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	IV-8
		X	X	X	X	X	X	X	X	
		Timer 1 Compare Register								
X'3F54'	TM0MD	-	-	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0	VI-10
		-	-	0	0	0	0	0	0	
				Pulse Width Measurement	Timer 0 Operation Mode Selection	Timer 0 Count Control	Clock Source Selection			
X'3F55'	TM1MD	-	-	-	TM1CAS	TM1EN	TM1CK2	TM1CK1	TM1CK0	VI-11
		-	-	-	0	0	0	0	0	
					Timer 1 Operation Mode Selection	Timer 1 Count Control	Clock Source Selection			

Note) x : Initial value is unstable. - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F56'	CK0MD	-	-	-	-	-	TM0PSC1	TM0PSC0	TM0BAS	V-7
		-	-	-	-	-	X	X	X	
							Count Clock Setting (Prescaler Output)			
X'3F57'	CK1MD	-	-	-	-	-	TM1PSC1	TM1PSC0	TM1BAS	V-7
		-	-	-	-	-	X	X	X	
							Count Clock Setting (Prescaler Output)			
X'3F58'	TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	VI-9
		X	X	X	X	X	X	X	X	
		Timer 2 Binary Counter								
X'3F59'	TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	VI-9
		X	X	X	X	X	X	X	X	
		Timer 3 Binary Counter								
X'3F5A'	TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	VI-8
		X	X	X	X	X	X	X	X	
		Timer 2 Compare Register								
X'3F5B'	TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	VI-8
		X	X	X	X	X	X	X	X	
		Timer 3 Compare Register								
X'3F5C'	TM2MD	TM2ADD2	TM2ADD1	TM2MOD	TM2PWM	TM2EN	TM2CK2	TM2CK1	TM2CK0	VI-12
		0	0	0	0	0	0	0	0	
		Added Pulse Position		Pulse Width Measurement Control	Timer 2 Operation ModeSelection	Timer 2 Count Control	Clock Source Selection			
X'3F5D'	TM3MD	-	-	-	TM3CAS	TM3EN	TM3CK2	TM3CK1	TM3CK0	VI-13
		-	-	-	0	0	0	0	0	
					Timer 3 Operation ModeSelection	Timer 3 Count Control	Clock Source Selection			
X'3F5E'	CK2MD	-	-	-	-	-	TM2PSC1	TM2PSC0	TM2BAS	V-8
		-	-	-	-	-	X	X	X	
							Count Clock Setting (Prescaler Output)			
X'3F5F'	CK3MD	-	-	-	-	-	TM3PSC1	TM3PSC0	TM3BAS	V-8
		-	-	-	-	-	X	X	X	
							Count Clock Setting (Prescaler Output)			
X'3F68'	TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	VIII-5
		X	X	X	X	X	X	X	X	
		Timer 6 Binary Counter								
X'3F69'	TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	VIII-5
		X	X	X	X	X	X	X	X	
		Timer 6 Compare Register								
X'3F6A'	TM6MD	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0	VIII-6
		0	0	0	0	0	0	0	0	
		Timer 8 Binary Counter ClearSelection	Time Base Timer Interrupt Cycle Control			Timer 6 Clock Source Selection			Time Base Timer Clock SourceSelection	
X'3F6B'	TBCLR	-	-	-	-	-	-	-	-	VIII-5
		-	-	-	-	-	-	-	-	
		Time Base Timer Clear Control Register (For Writing Only)								
X'3F6C'	TM7MD3	TM7CKSMP	TM7CKEDG	RESERVED	TM7EDG	RESERVED	RESERVED	TM7OUT1	TM7OUT0	VII-15
		0	0	0	0	0	0	0	0	
		Input Capture Sampling Selection	TM7IO Count Edge Selection	Set always to "0"	Dead Time Selection	Set always to "0"		Timer Output Waveform Selection		
X'3F6D'	TM8MD3	TM8CKSMP	RESERVED	RESERVED	RESERVED	RESERVED	TM78SEL	TM8PWMF	TM8BCR	VII-18
		0	0	0	0	0	0	0	0	
		Input Capture Sampling Selection	Set always to "0"				Timer Output Waveform Selection	PWM Output at TM8EN=0	Timer 8 Counter Clear Factor Selection	
X'3F6E'	RMCTR	-	-	-	TM0RM	RM0EN	-	RMDTY0	RMBTMS	VI-14
		-	-	-	0	0	-	0	0	
					P10 Special Function Output Selection	Remote Control Carrier Output Enable		RemoteControl Carrier Output DutySelection	Remote Control Carrier Base Timer Selection	

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Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F6F'	PSCMD	-	-	-	-	-	-	-	PSCEN	V-6
		-	-	-	-	-	-	-	0	
									Prescaler Count Control	
X'3F70'	TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 7 Binary Counter Lower 8 Bits								
X'3F71'	TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 7 Binary Counter Upper 8 Bits								
X'3F72'	TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	VII-7
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 1 Lower 8 Bits								
X'3F73'	TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	VII-7
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 1 Upper 8 Bits								
X'3F74'	TM7PR1L	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0	VII-9
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 1 Lower 8 Bits								
X'3F75'	TM7PR1H	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0	VII-9
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 1 Upper 8 Bits								
X'3F76'	TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 7 Input Compare Register Lower 8 Bits								
X'3F77'	TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 7 Input Compare Register Upper 8 Bits								
X'3F78'	TM7MD1	RESERVED	RESERVED	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0	VII-13
		0	0	1	0	0	0	0	0	
		Set always to "0"		Timer Output Reset Control	Timer 7 Count Control	Count Clock Selection		Clock Source Selection		
X'3F79'	TM7MD2	T7ICEDG	T7PWMSL	TM7BCR	RESERVED	T7IRS1	T7ICEN	T7ICT1	T7ICT0	VII-14
		0	0	0	0	0	0	0	0	
		Capture Trigger Edge Selection	IGBT,PWM Mode Selection	Timer7 Counter Clear Factor Selection	Set always to "0"	Timer 7 Interrupt Factor Selection	Capture Operation Enable	IGBT Trigger/ Capture Trigger Selection		
X'3F7A'	TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	VII-7
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 2 Lower 8 Bits								
X'3F7B'	TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	VII-7
		X	X	X	X	X	X	X	X	
		Timer 7 Compare Register 2 Upper 8 Bits								
X'3F7C'	TM7PR2L	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0	VII-9
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 2 Lower 8 Bits								
X'3F7D'	TM7PR2H	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0	VII-9
		X	X	X	X	X	X	X	X	
		Timer 7 Preset Register 2 Upper 8 Bits								
X'3F7E'	TM7DEADPR1	TM7DEADPR17	TM7DEADPR16	TM7DEADPR15	TM7DEADPR14	TM7DEADPR13	TM7DEADPR12	TM7DEADPR11	TM7DEADPR10	VII-12
		0	0	0	0	0	0	0	0	
		Timer 7 Dead Time Preset Register 1								
X'3F7F'	TM7DEADPR2	TM7DEADPR27	TM7DEADPR26	TM7DEADPR25	TM7DEADPR24	TM7DEADPR23	TM7DEADPR22	TM7DEADPR21	TM7DEADPR20	VII-13
		0	0	0	0	0	0	0	0	
		Timer 7 Dead Time Preset Register 2								

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Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F80'	TM8BCL	TM8BCL7	TM8BCL6	TM8BCL5	TM8BCL4	TM8BCL3	TM8BCL2	TM8BCL1	TM8BCL0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 8 Binary Counter Lower 8 Bits								
X'3F81'	TM8BCH	TM8BCH7	TM8BCH6	TM8BCH5	TM8BCH4	TM8BCH3	TM8BCH2	TM8BCH1	TM8BCH0	VII-11
		X	X	X	X	X	X	X	X	
		Timer 8 Binary Counter Upper 8 Bits								
X'3F82'	TM8OC1L	TM8OC1L7	TM8OC1L6	TM8OC1L5	TM8OC1L4	TM8OC1L3	TM8OC1L2	TM8OC1L1	TM8OC1L0	VII-8
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register Lower 8 Bits								
X'3F83'	TM8OC1H	TM8OC1H7	TM8OC1H6	TM8OC1H5	TM8OC1H4	TM8OC1H3	TM8OC1H2	TM8OC1H1	TM8OC1H0	VII-8
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 1 Upper 8 Bits								
X'3F84'	TM8PR1L	TM8PR1L7	TM8PR1L6	TM8PR1L5	TM8PR1L4	TM8PR1L3	TM8PR1L2	TM8PR1L1	TM8PR1L0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 1 Lower 8 Bits								
X'3F85'	TM8PR1H	TM8PR1H7	TM8PR1H6	TM8PR1H5	TM8PR1H4	TM8PR1H3	TM8PR1H2	TM8PR1H1	TM8PR1H0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 1 Upper 8 Bits								
X'3F86'	TM8ICL	TM8ICL7	TM8ICL6	TM8ICL5	TM8ICL4	TM8ICL3	TM8ICL2	TM8ICL1	TM8ICL0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 8 Input Caputure Register Lower 8 Bits								
X'3F87'	TM8ICH	TM8ICH7	TM8ICH6	TM8ICH5	TM8ICH4	TM8ICH3	TM8ICH2	TM8ICH1	TM8ICH0	VII-12
		X	X	X	X	X	X	X	X	
		Timer 8 Input Caputure Register Upper 8 Bits								
X'3F88'	TM8MD1	TM8EN	TM8CAS	TM8CL	TM8PS2	TM8PS1	TM8PS0	TM8CK1	TM8CK0	VII-16
		0	0	1	0	0	0	0	0	
		Timer 8 Count Control	Timer 7,8 Cascade Control	Timer Output Reset Control	Count Clock Selection			Clock Source Selection		
X'3F89'	TM8MD2	T8ICEDG	T8PWMSL	TM8PWM1	TM8PWM0	TM8IRS1	T8ICEN	T8ICT1	T8ICT0	VII-17
		0	0	0	0	0	0	0	0	
		Capture Trigger Edge Selection	PWM Mode Selection	PWM Waveform Selection	Timer Output Waveform Selecrion	Timer8 Interrupt Factor Selection	Input Capture Operation Enable	Capture Trigger Selection		
X'3F8A'	TM8OC2L	TM8OC2L7	TM8OC2L6	TM8OC2L5	TM8OC2L4	TM8OC2L3	TM8OC2L2	TM8OC2L1	TM8OC2L0	VII-8
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 2 Lower 8 Bits								
X'3F8B'	TM8OC2H	TM8OC2H7	TM8OC2H6	TM8OC2H5	TM8OC2H4	TM8OC2H3	TM8OC2H2	TM8OC2H1	TM8OC2H0	VII-8
		X	X	X	X	X	X	X	X	
		Timer 8 Compare Register 2 Upper 8 Bits								
X'3F8C'	TM8PR2L	TM8PR2L7	TM8PR2L6	TM8PR2L5	TM8PR2L4	TM8PR2L3	TM8PR2L2	TM8PR2L1	TM8PR2L0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 2 Lower 8 Bits								
X'3F8D'	TM8PR2H	TM8PR2H7	TM8PR2H6	TM8PR2H5	TM8PR2H4	TM8PR2H3	TM8PR2H2	TM8PR2H1	TM8PR2H0	VII-10
		X	X	X	X	X	X	X	X	
		Timer 8 Preset Register 2 Upper 8 Bits								
X'3F8E'	NFCTR	P21IM	NF1SCK1	NF1SCK0	NF1EN	NF0SCK2	NF0SCK1	NF0SCK0	NF0EN	III-47
		0	0	0	0	0	0	0	0	
		ACZ Input Enable Flag	IRQ1/Noise Filter Sampling Period Selection		IRQ1/Noise Filter Enable	IRQ0 / Noise Filter Sampling Cycle Selection			IRQ0 / Noise Filter Enable	
X'3F8F'	EDGDT	EDGSEL7	EDGSEL6	-	-	EDGSEL3	EDGSEL2	-	-	III-48
		0	0	-	-	0	0	-	-	
		IRQ7 Both Edges Interrupt Selection	IRQ6 Both Edges Interrupt Selection			IRQ3 Both Edges Interrupt Selection	IRQ2 Both Edges Interrupt Selection			
X'3F90'	SCOMD0	SC0CE1	SC0REN	SC0TRN	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0	XI-6
		0	0	0	0	0	1	1	1	
		Transmission Data/ Recived Data Edge Selection	Recieved Data polarity Selection	Transmission Data polarity Selection	First Transfer Bit Selection	Start Condition Selection	Synchronous Serial Transfer Bit Count Selection			

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Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3F91'	SC0MD1	SC0IOM	SC0SBTS	SC0SBIS	SC0SBOS	SC0CKM	SC0MST	-	SC0CMD	XI-7
		0	0	0	0	0	0	-	0	
		Serial Data Input Selection	SBT Pin Function Selection	Serial I/F Input Control	SBO Pin Function Selection	Clock Divided by 8 Selection	Clock Master/Slave Selection		Synchronous/ Duplex UART Selection	
X'3F92'	SC0MD2	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	-	SC0BRKF	SC0BRKE	XI-9
		0	0	0	0	0	-	0	0	
		Specify Flame Mode		Specify Added Bit		Parity Enable		Break Status Receive Monitor	Break Status Transmit Control	
X'3F93'	SC0MD3	SC0TBSY	SC0RBSY	SC0TEMP	SC0REMP	SC0FEF	SC0PEK	SC0ORE	SC0ERE	XI-10
		0	0	0	0	0	0	0	0	
		Serial Bus Status		Transfer Buffer Empty Flag	Receive Buffer Empty Flag	Framing Error Detection	Parity Error Detection	Overrun Error Detection	Error Monitor Flag	
X'3F94'	RXBUF0	RXBUF07	RXBUF06	RXBUF05	RXBUF04	RXBUF03	RXBUF02	RXBUF01	RXBUF00	XI-5
		X	X	X	X	X	X	X	X	
		Serial Interface 0 Receive Buffer								
X'3F95'	TXBUF0	TXBUF07	TXBUF06	TXBUF05	TXBUF04	TXBUF03	TXBUF02	TXBUF01	TXBUF00	XI-5
		X	X	X	X	X	X	X	X	
		Serial Interface 0 Transfer Buffer								
X'3F96'	SC0ODC	-	-	-	-	-	-	SC0ODC1	SC0ODC0	XI-11
		-	-	-	-	-	-	0	0	
								P02/PB7 N ch Open-drain Control	P00/PB5 N ch Open-drain Control	
X'3F97'	SC0CKS	-	-	-	-	SC0TMSEL	SC0PSC2	SC0PSC1	SC0PSC0	V-9 XI-12
		-	-	-	-	X	X	X	X	
						Serial 0 Tranfer Clock Selection (Prescaler Output)				
X'3FA0'	SC2MD0	SC2BSY	SC2CE1	-	SC2DIR	SC2STE	SC2LNG2	SC2LNG1	SC2LNG0	XII-6
		0	0	-	0	0	1	1	1	
		Serial Bus Status	Transmission Data/ Recived Data Edge Selection		Specify First Bit to be Transferred	Start Condition Selection	Synchronous serial transfer bit Selection			
X'3FA1'	SC2MD1	SC2IOM	SC2SBTS	SC2SBIS	SC2SBOS	-	SC2MST	-	-	XII-7
		0	0	0	0	-	0	-	-	
		Serial Data Input Pin Selection	SBT2 Pin Function Selection	Serial Input Control	SBO2 Pin Function Selection		Clock Master/Slave Selection			
X'3FA2'	SC2TRB	SC2TRB7	SC2TRB6	SC2TRB5	SC2TRB4	SC2TRB3	SC2TRB2	SC2TRB1	SC2TRB0	XII-5
		X	X	X	X	X	X	X	X	
		Serial Interface 2 Transmission/Reception Shift Register								
X'3FA6'	SC2ODC	-	-	-	-	-	-	SC2ODC1	SC2ODC0	XII-8
		-	-	-	-	-	-	0	0	
								P05 N ch Open-drain Control	P03 N ch Open-drain Control	
X'3FA7'	SC2CKS	-	-	-	-	RESERVED	SC2PSC2	SC2PSC1	SC2PSC0	V-9 XII-8
		-	-	-	-	X	X	X	X	
						Set to "0" when serial 2 is used	Serial 2 Transfer Clock Selection (Prescaler Output)			
X'3FB0'	ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	-	-	-	XIII-5
		0	0	0	0	0	-	-	-	
		Sample Hold Time Setup		A/D Conversion Clock Selection		A/D Rudder Resistance Control				
X'3FB1'	ANCTR1	-	-	-	-	ANCHS3	ANCHS2	ANCHS1	ANCHS0	XIII-6
		-	-	-	-	0	0	0	0	
						Analog Input Channel Selection				
X'3FB2'	ANCTR2	ANST	Reserved	-	-	-	-	-	-	XIII-6
		0	0	-	-	-	-	-	-	
		A/D Conversion Status	Set always to "0".							
X'3FB3'	ANBUF0	ANBUF07	ANBUF06	-	-	-	-	-	-	XIII-7
		X	X	-	-	-	-	-	-	
		A/D Conversion Data Storage Register (Lower 2 Bits)								
X'3FB4'	ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	XIII-7
		X	X	X	X	X	X	X	X	
		A/D Conversion Data Storage Register (Upper 8 bits)								

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Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3FC5'	RMCTR1	-	-	RMRMD1	RMRMD0	RMNF	RMCLK2	RMCLK1	RMCLK0	XV-5
		0	0	0	0	0	0	-	0	
		Set always to "0"		Edge Recognition Selection		Noise Filter Selection	Remote Control Sample Block Selection			
X'3FC6'	RMCTR2	RM1TSW3	RM1TSW2	RM1TSW1	RM1TSW0	RMEN	RMHDEN	RMHSW1	RMHSW0	XV-6
		0	0	0	0	0	0	0	0	
		1T Count Selection				Reception Start/Stop	Data Detection Switching Selection	Header System Selection		
X'3FC7'	RMCTR3	RMHDL7	RMHDL6	RMHDL5	RMHDL4	RMHDL3	RMHDL2	RMHDL1	RMHDL0	XV-7
		0	0	0	0	0	0	0	0	
		Header L Interval Count Setup								
X'3FC8'	RMCTR4	RMHDH7	RMHDH6	RMHDH5	RMHDH4	RMHDH3	RMHDH2	RMHDH1	RMHDH0	XV-7
		0	0	0	0	0	0	0	0	
		Header H Interval Count Setup								
X'3FC9'	RMCTR5	RMZERO7	RMZERO6	RMZERO5	RMZERO4	RMZERO3	RMZERO2	RMZERO1	RMZERO0	XV-8
		0	0	0	0	0	0	0	0	
		0 Data Count Setup								
X'3FCA'	RMCTR6	RM0NE7	RM0NE6	RM0NE5	RM0NE4	RM0NE3	RM0NE2	RM0NE1	RM0NE0	XV-8
		0	0	0	0	0	0	0	0	
		1 Data Count Setup								
X'3FCB'	RMCTR7	RMHDD7	RMHDD6	RMHDD5	RMHDD4	RMHDD3	RMHDD2	RMHDD1	RMHDD0	XV-8
		0	0	0	0	0	0	0	0	
		Header + 8-bit Detection Count Setup								
X'3FCC'	RMCTR8	RMCNT2	RMCNT1	RMCNT0	RMRECV	HEADER	160TOVF	DATAERR	1TERR	XV-9
		0	0	0	0	0	0	0	0	
		Data Count Value next of Header Setup			8-bit Reception Complete	Header Detection	Counter Overflow Detection	0/1 Error Detection	1T Error Detection	
X'3FCD'	RMDAT1	RMDATS7	RMDATS6	RMDATS5	RMDATS4	RMDATS3	RMDATS2	RMDATS1	RMDATS0	XV-10
		X	X	X	X	X	X	X	X	
		Remote Control Shift Data								
X'3FCE'	RMDAT2	RMDATB7	RMDATB6	RMDATB5	RMDATB4	RMDATB3	RMDATB2	RMDATB1	RMDATB0	XV-10
		X	X	X	X	X	X	X	X	
		Remote Control Buffer Data								
X'3FCF'	RMICTR	-	RMJD2	RMJD1	RMJD0	DATERREN	OVFEN	HEADEN	SBEN	XV-11
		0	0	0	0	0	0	0	0	
		Set always to "0"	Data Judgement Margin Setup			Data Error Interrupt	Counter Overflow Interrupt	Header Interrupt	Shift Buffer Interrupt	
X'3FD9'	LCDMD1	LCDEN	SGDEN	LCDTY1	LCDTY0	LCDCK3	LCDCK2	LCDCK1	LCDCK0	XIV-7
		0	0	0	0	0	0	0	0	
		LCD Driver Circuit ON	LCD Display Enable	LCD Display Duty Selection		LCD Clock Source Selection				
X'3FDA'	LCDMD2	-	-	LCRHL	LCREN	-	-	-	-	XIV-8
		0	0	0	0	0	0	0	0	
		Set always to "0"		Internal Voltage Divider Resistor Type Selection	Internal Voltage Divider Resistor Connection	Set always to "0"				
X'3FDB'	LCCTR1	-	-	COMSL3	COMSL2	COMSL1	COMSL0	LCISL1	LCISL0	IV-23,51,55 XIV-9
		-	-	0	0	0	0	0	0	
				COM3/Port93 Selection	COM2/Port92 Selection	COM1/Port91 Selection	COM0/Port90 Selection	SEG0-7 /Port080-87 Selection	SEG8-9 /Port36-35 Selection	
X'3FDC'	LCCTR2	LC2SL7	LC2SL6	LC2SL5	LC2SL4	LC2SL3	LC2SL2	LC2SL1	LC2SL0	IV-42,46 XIV-10
		0	0	0	0	0	0	0	0	
		SEG10 to 11/ P77-76 Selection	SEG12-13/ P75-74 Selection	SEG14-15/ P73-72 Selection	SEG16-17/ P71-70 Selection	SEG18-19/ P67-66 Selection	SEG20-21/ P65-64 Selection	SEG22-23/ P63-62 Selection	SEG24-25/ P61-60 Selection	
X'3FDD'	LCCTR3	-	LC3SL6	LC3SL5	LC3SL4	LC3SL3	LC3SL2	LC3SL1	LC3SL0	IV-24,32 XIV-11
		-	0	0	0	0	0	0	0	
			SEG34/ P34 Selection	SEG35-36/ P33-32 Selection	SEG37-38/ P31-30 Selection	SEG26-27/ P47-46 Selection	SEG28-29/ P45-44 Selection	SEG30-31/ P43-42 Selection	SEG32-33/ P41-40 Selection	
X'3FDE'	LCCTR4	LC4SL7	LC4SL6	LC4SL5	LC4SL4	LC4SL3	LC4SL2	LC4SL1	LC4SL0	IV-63 XIV-12
		0	0	0	0	0	0	0	0	
		SEG39/ PB7 Selection	SEG40/ PB6 Selection	SEG41/ PB5 Selection	SEG42/ PB4 Selection	SEG43/ PB3 Selection	SEG44/ PB2 Selection	SEG45/ PB1 Selection	SEG46/ PB0 Selection	

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Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3FE1'	NMICR	-	-	-	-	-	PIR	WDIR	RESERVED	III-16
		-	-	-	-	-	0	0	0	
							Program Interrupt Request	Watchdog Timer Interrupt Request	Set always to "0"	
X'3FE2'	IRQ0ICR	IRQ0LV1	IRQ0LV0	REDG0	-	-	-	IRQ0IE	IRQ0IR	III-17
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE3'	IRQ1ICR	IRQ1LV1	IRQ1LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR	III-18
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE4'	IRQ2ICR	IRQ2LV1	IRQ2LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR	III-19
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE5'	IRQ3ICR	IRQ3LV1	IRQ3LV0	REDG3	-	-	-	IRQ3IE	IRQ3IR	III-20
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE6'	IRQ4ICR	IRQ4LV1	IRQ4LV0	REDG4	-	-	-	IRQ4IE	IRQ4IR	III-21
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE7'	IRQ5ICR	IRQ5LV1	IRQ5LV0	REDG5	-	-	-	IRQ5IE	IRQ5IR	III-22
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE8'	IRQ6ICR	IRQ6LV1	IRQ6LV0	REDG6	-	-	-	IRQ6IE	IRQ6IR	III-23
		0	0	0	-	-	-	0	0	
		External Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable External Interrupt	External Interrupt Requesst	
X'3FE9'	TM0ICR	TM0LV1	TM0LV0	-	-	-	-	TM0IE	TM0IR	III-24
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FEA'	TM1ICR	TM1LV1	TM1LV0	-	-	-	-	TM1IE	TM1IR	III-25
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FEB'	TM2ICR	TM2LV1	TM2LV0	-	-	-	-	TM2IE	TM2IR	III-26
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FEC'	TM3ICR	TM3LV1	TM3LV0	-	-	-	-	TM3IE	TM3IR	III-27
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FED'	IRQ7ICR	IRQ7LV1	IRQ7LV0	REDG7	-	-	-	IRQ7IE	IRQ7IR	III-28
		0	0	0	-	-	-	0	0	
		Interrupt Level Selection		External Interrupt Valid Edge Setup				Enable Interrupt	Interrupt Requesst	
X'3FEE'	RMICR	RMLV1	RMLV0	-	-	-	-	RMIE	RMIR	III-29
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FEF'	TM6ICR	TM6LV1	TM6LV0	-	-	-	-	TM6IE	TM6IR	III-30
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF0'	TBICR	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR	III-31
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF1'	TM7ICR	TM7LV1	TM7LV0	-	-	-	-	TM7IE	TM7IR	III-32
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	

Note) x : Initial value is unstable. - : No data

Address	Register	Bit Symbol / Initial Value / Description								Page
		bit 7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
X'3FF2'	T7OC2ICR	T7OC2LV1	T7OC2LV0	-	-	-	-	T7OC2IE	T7OC2IR	III-33
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF3'	TM8ICR	TM8LV1	TM8LV0	-	-	-	-	TM8IE	TM8IR	III-34
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF4'	T8OC2ICR	T8OC2LV1	T8OC2LV0	-	-	-	-	T8OC2IE	T8OC2IR	III-35
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF5'	SCORICR	SCORLV1	SCORLV0	-	-	-	-	SCORIE	SCORIR	III-36
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF6'	SCOTICR	SCOTLV1	SCOTLV0	-	-	-	-	SCOTIE	SCOTIR	III-37
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FF8'	SC2ICR	SC2LV1	SC2LV0	-	-	-	-	SC2IE	SC2IR	III-38
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	
X'3FFA'	ADICR	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR	III-39
		0	0	-	-	-	-	0	0	
		Interrupt Level Selection						Enable Interrupt	Interrupt Requesst	

Note) x : Initial value is unstable. - : No data

17-7 Instruction Set

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Machine Code Ext.	1	2	3	4	5	6	7	8	9	10	11	Notes
Data Move Instructions																						
MOV	MOV Dn,Dm	Dn→Dm	--	--	--	--	2	1			1010	DnDm										
	MOV imm8,Dm	imm8→Dm	--	--	--	--	4	2			1010	DmDm	<#8.	...>								
	MOV Dn,PSW	Dn→PSW	●	●	●	●	3	3		0010	1001	01Dn										
	MOV PSW,Dm	PSW→Dm	--	--	--	--	3	2		0010	0001	01Dm										
	MOV (An),Dm	mem8(An)→Dm	--	--	--	--	2	2			0100	1ADm										
	MOV (d8,An),Dm	mem8(d8+An)→Dm	--	--	--	--	4	2			0110	1ADm	<d8.	...>								*1
	MOV (d16,An),Dm	mem8(d16+An)→Dm	--	--	--	--	7	4		0010	0110	1ADm	<d16	....	....	...>						
	MOV (d4,SP),Dm	mem8(d4+SP)→Dm	--	--	--	--	3	2			0110	01Dm	<d4>									*2
	MOV (d8,SP),Dm	mem8(d8+SP)→Dm	--	--	--	--	5	3		0010	0110	01Dm	<d8.	...>								*3
	MOV (d16,SP),Dm	mem8(d16+SP)→Dm	--	--	--	--	7	4		0010	0110	00Dm	<d16	....	....	...>						
	MOV (io8),Dm	mem8(IOTOP+io8)→Dm	--	--	--	--	4	2			0110	00Dm	<io8	...>								
	MOV (abs8),Dm	mem8(abs8)→Dm	--	--	--	--	4	2			0100	01Dm	<abs	8..>								
	MOV (abs12),Dm	mem8(abs12)→Dm	--	--	--	--	5	2			0100	00Dm	<abs	12..	...>							
	MOV (abs16),Dm	mem8(abs16)→Dm	--	--	--	--	7	4		0010	1100	00Dm	<abs	16..	....	...>						
	MOV Dn,(Am)	Dn→mem8(Am)	--	--	--	--	2	2			0101	1aDn										
	MOV Dn,(d8,Am)	Dn→mem8(d8+Am)	--	--	--	--	4	2			0111	1aDn	<d8.	...>								*1
	MOV Dn,(d16,Am)	Dn→mem8(d16+Am)	--	--	--	--	7	4		0010	0111	1aDn	<d16	....	....	...>						
	MOV Dn,(d4,SP)	Dn→mem8(d4+SP)	--	--	--	--	3	2			0111	01Dn	<d4>									*2
	MOV Dn,(d8,SP)	Dn→mem8(d8+SP)	--	--	--	--	5	3		0010	0111	01Dn	<d8.	...>								*3
	MOV Dn,(d16,SP)	Dn→mem8(d16+SP)	--	--	--	--	7	4		0010	0111	00Dn	<d16	....	....	...>						
	MOV Dn,(io8)	Dn→mem8(IOTOP+io8)	--	--	--	--	4	2			0111	00Dn	<io8	...>								
	MOV Dn,(abs8)	Dn→mem8(abs8)	--	--	--	--	4	2			0101	01Dn	<abs	8..>								
	MOV Dn,(abs12)	Dn→mem8(abs12)	--	--	--	--	5	2			0101	00Dn	<abs	12..	...>							
	MOV Dn,(abs16)	Dn→mem8(abs16)	--	--	--	--	7	4		0010	1101	00Dn	<abs	16..	....	...>						
	MOV imm8,(io8)	imm8→mem8(IOTOP+io8)	--	--	--	--	6	3			0000	0010	<io8	...>	<#8.	...>						
	MOV imm8,(abs8)	imm8→mem8(abs8)	--	--	--	--	6	3			0001	0100	<abs	8..>	<#8.	...>						
	MOV imm8,(abs12)	imm8→mem8(abs12)	--	--	--	--	7	3			0001	0101	<abs	12..	...>	<#8.	...>					
	MOV imm8,(abs16)	imm8→mem8(abs16)	--	--	--	--	9	5		0011	1101	1001	<abs	16..	....	...>	<#8.	...>				
	MOV Dn,(HA)	Dn→mem8(HA)	--	--	--	--	2	2			1101	00Dn										
MOVW	MOVW (An),DWm	mem16(An)→DWm	--	--	--	--	2	3			1110	00Ad										
	MOVW (An),Am	mem16(An)→Am	--	--	--	--	3	4		0010	1110	10Aa										*4
	MOVW (d4,SP),DWm	mem16(d4+SP)→DWm	--	--	--	--	3	3			1110	011d	<d4>									*2
	MOVW (d4,SP),Am	mem16(d4+SP)→Am	--	--	--	--	3	3			1110	010a	<d4>									*2
	MOVW (d8,SP),DWm	mem16(d8+SP)→DWm	--	--	--	--	5	4		0010	1110	011d	<d8.	...>								*3
	MOVW (d8,SP),Am	mem16(d8+SP)→Am	--	--	--	--	5	4		0010	1110	010a	<d8.	...>								*3
	MOVW (d16,SP),DWm	mem16(d16+SP)→DWm	--	--	--	--	7	5		0010	1110	001d	<d16	....	....	...>						
	MOVW (d16,SP),Am	mem16(d16+SP)→Am	--	--	--	--	7	5		0010	1110	000a	<d16	....	....	...>						
	MOVW (abs8),DWm	mem16(abs8)→DWm	--	--	--	--	4	3			1100	011d	<abs	8..>								
	MOVW (abs8),Am	mem16(abs8)→Am	--	--	--	--	4	3			1100	010a	<abs	8..>								
	MOVW (abs16),DWm	mem16(abs16)→DWm	--	--	--	--	7	5		0010	1100	011d	<abs	16..	....	...>						
	MOVW (abs16),Am	mem16(abs16)→Am	--	--	--	--	7	5		0010	1100	010a	<abs	16..	....	...>						
	MOVW DWn,(Am)	DWn→mem16(Am)	--	--	--	--	2	3			1111	00aD										
	MOVW An,(Am)	An→mem16(Am)	--	--	--	--	3	4		0010	1111	10aA										*4
	MOVW DWn,(d4,SP)	DWn→mem16(d4+SP)	--	--	--	--	3	3			1111	011D	<d4>									*2
	MOVW An,(d4,SP)	An→mem16(d4+SP)	--	--	--	--	3	3			1111	010A	<d4>									*2
	MOVW DWn,(d8,SP)	DWn→mem16(d8+SP)	--	--	--	--	5	4		0010	1111	011D	<d8.	...>								*3
	MOVW An,(d8,SP)	An→mem16(d8+SP)	--	--	--	--	5	4		0010	1111	010A	<d8.	...>								*3
	MOVW DWn,(d16,SP)	DWn→mem16(d16+SP)	--	--	--	--	7	5		0010	1111	001D	<d16	....	....	...>						
	MOVW An,(d16,SP)	An→mem16(d16+SP)	--	--	--	--	7	5		0010	1111	000A	<d16	....	....	...>						
	MOVW DWn,(abs8)	DWn→mem16(abs8)	--	--	--	--	4	3			1101	011D	<abs	8..>								
	MOVW An,(abs8)	An→mem16(abs8)	--	--	--	--	4	3			1101	010A	<abs	8..>								
	MOVW DWn,(abs16)	DWn→mem16(abs16)	--	--	--	--	7	5		0010	1101	011D	<abs	16..	....	...>						
	MOVW An,(abs16)	An→mem16(abs16)	--	--	--	--	7	5		0010	1101	010A	<abs	16..	....	...>						
	MOVW DWn,(HA)	DWn→mem16(HA)	--	--	--	--	2	3			1001	010D										
	MOVW An,(HA)	An→mem16(HA)	--	--	--	--	2	3			1001	011A										
	MOVW imm8,DWm	sign(imm8)→DWm	--	--	--	--	4	2			0000	110d	<#8.	...>								*5
	MOVW imm8,Am	zero(imm8)→Am	--	--	--	--	4	2			0000	111a	<#8.	...>								*6
	MOVW imm16,DWm	imm16→DWm	--	--	--	--	6	3			1100	111d	<#16	....	....	...>						

*1 d8 sign-extension *4 A=An, a=Am
*2 d4 zero-extension *5 #8 sign-extension
*3 d8 zero-extension *6 #8 zero-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
	MOVW imm16,Am	imm16→Am	--	--	--	--	6	3			1101	111a	<#16	....	....	...>						
	MOVW SP,Am	SP→Am	--	--	--	--	3	3			0010	0000	100a									
	MOVW An,SP	An→SP	--	--	--	--	3	3			0010	0000	101A									
	MOVW DWn,DWm	DWn→DWm	--	--	--	--	3	3			0010	1000	00Dd									*1
	MOVW DWn,Am	DWn→Am	--	--	--	--	3	3			0010	0100	11Da									
	MOVW An,DWm	An→DWm	--	--	--	--	3	3			0010	1100	11Ad									
	MOVW An,Am	An→Am	--	--	--	--	3	3			0010	0000	00Aa									*2
PUSH	PUSH Dn	SP-1→SP,Dn→mem8(SP)	--	--	--	--	2	3			1111	10Dn										
	PUSH An	SP-2→SP,An→mem16(SP)	--	--	--	--	2	5			0001	011A										
POP	POP Dn	mem8(SP)→Dn,SP+1→SP	--	--	--	--	2	3			1110	10Dn										
	POP An	mem16(SP)→An,SP+2→SP	--	--	--	--	2	4			0000	011A										
EXT	EXT Dn,DWm	sign(Dn)→DWm	--	--	--	--	3	3			0010	1001	000d									*3

Arithmetic manupulation instructions

ADD	ADD Dn,Dm	Dm+Dn→Dm	●	●	●	●	3	2			0011	0011	DnDm									
	ADD imm4,Dm	Dm+sign(imm4)→Dm	●	●	●	●	3	2			1000	00Dm	<#4>									*6
	ADD imm8,Dm	Dm+imm8→Dm	●	●	●	●	4	2			0000	10Dm	<#8.	...>								
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	●	●	●	●	3	2	○		0011	1011	DnDm									
ADDW	ADDW DWn,DWm	DWm+DWn→DWm	●	●	●	●	3	3	○		0010	0101	00Dd									*1
	ADDW DWn,Am	Am+DWn→Am	●	●	●	●	3	3	○		0010	0101	10Da									
	ADDW imm4,Am	Am+sign(imm4)→Am	●	●	●	●	3	2			1110	110a	<#4>									*6
	ADDW imm8,Am	Am+sign(imm8)→Am	●	●	●	●	5	3			0010	1110	110a	<#8.	...>							*7
	ADDW imm16,Am	Am+imm16→Am	●	●	●	●	7	4			0010	0101	011a	<#16	....	....	...>					
	ADDW imm4,SP	SP+sign(imm4)→SP	--	--	--	--	3	2			1111	1101	<#4>									*6
	ADDW imm8,SP	SP+sign(imm8)→SP	--	--	--	--	4	2			1111	1100	<#8.	...>								*7
	ADDW imm16,SP	SP+imm16→SP	--	--	--	--	7	4			0010	1111	1100	<#16	....	....	...>					
	ADDW imm16,DWm	DWm+imm16→DWm	●	●	●	●	7	4			0010	0101	010d	<#16	....	....	...>					
ADDUW	ADDUW Dn,Am	Am+zero(Dn)→Am	●	●	●	●	3	3	○		0010	1000	1aDn									*8
ADDSW	ADDSW Dn,Am	Am+sign(Dn)→Am	●	●	●	●	3	3	○		0010	1001	1aDn									
SUB	SUB Dn,Dm(when Dn≠Dm)	Dm-Dn→Dm	●	●	●	●	3	2	○		0010	1010	DnDm									
	SUB Dn,Dn	Dn-Dn→Dn	0	0	0	1	2	1			1000	01Dn										
	SUB imm8,Dm	Dm-imm8→Dm	●	●	●	●	5	3			0010	1010	DmDm	<#8.	...>							
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	●	●	●	●	3	2	○		0010	1011	DnDm									
SUBW	SUBW DWn,DWm	DWm-DWn→DWm	●	●	●	●	3	3			0010	0100	00Dd									*1
	SUBW DWn,Am	Am-DWn→Am	●	●	●	●	3	3			0010	0100	10Da									
	SUBW imm16,DWm	DWm-imm16→DWm	●	●	●	●	7	4			0010	0100	010d	<#16	....	....	...>					
	SUBW imm16,Am	Am-imm16→Am	●	●	●	●	7	4			0010	0100	011a	<#16	....	....	...>					
MULU	MULU Dn,Dm	Dm*Dn→DWk	0	●	●	●	3	8			0010	1111	111D									*4
DIVU	DIVU Dn,DWm	DWm/Dn→DWm-l...DWm-h	●	●	●	●	3	9			0010	1110	111d									*5
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2			0011	0010	DnDm									
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2			1100	00Dm	<#8.	...>								
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3			0000	0100	<abs	8..>	<#8.	...>						
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3			0000	0101	<abs	12..	...>	<#8.	...>					
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5			0011	1101	1000	<abs	16..	....	...>	<#8.	...>			
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3			0010	1000	01Dd									*1
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3			0010	0101	11Da									
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3			0010	0000	01Aa									*2
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3			1100	110d	<#16	....	....	...>						
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3			1101	110a	<#16	....	....	...>						

Logical manipulation instructions

AND	AND Dn,Dm	Dm&Dn→Dm	0	●	0	●	3	2			0011	0111	DnDm									
	AND imm8,Dm	Dm&imm8→Dm	0	●	0	●	4	2			0001	11Dm	<#8.	...>								
	AND imm8,PSW	PSW&imm8→PSW	●	●	●	●	5	3			0010	1001	0010	<#8.	...>							
OR	OR Dn,Dm	DmIDn→Dm	0	●	0	●	3	2			0011	0110	DnDm									
	OR imm8,Dm	Dmlimm8→Dm	0	●	0	●	4	2			0001	10Dm	<#8.	...>								
	OR imm8,PSW	PSWlimm8→PSW	●	●	●	●	5	3			0010	1001	0011	<#8.	...>							
XOR	XOR Dn,Dm	Dm^Dn→Dm	0	●	0	●	3	2			0011	1010	DnDm									*9
	XOR imm8,Dm	Dm^imm8→Dm	0	●	0	●	5	3			0011	1010	DmDm	<#8.	...>							

*1 D=DWn, d=DWm
*2 A=An, a=Am
*3 d=DWm
*4 D=DWk
*5 D=DWm
*6 #4 sign-extension
*7 #8 sign-extension
*8 Dn zero extension
*9 m≠n

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
NOT	NOT Dn	¯Dn→Dn=	0	●	0	●	3	2			0010	0010	10Dn									
ASR	ASR Dn	Dn.msb→temp,Dn.lsb→CF Dn>>1→Dn,temp→Dn.msb	0	--	●	●	3	2	○		0010	0011	10Dn									
LSR	LSR Dn	Dn.lsb→CF,Dn>>1→Dn 0→Dn.msb	0	0	●	●	3	2	○		0010	0011	11Dn									
ROR	ROR Dn	Dn.lsb→temp,Dn>>1→Dn CF→Dn.msb,temp→CF	0	●	●	●	3	2	○		0010	0010	11Dn									
Bit manipulation instructions																						
BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1→mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011	1000	0bp.	<io8	...>							
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1→mem8(abs8)bp	0	●	0	●	4	4				1011	0bp.	<abs	8..>							
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1→mem8(abs16)bp	0	●	0	●	7	6			0011	1100	0bp.	<abs	16..	....	...>					
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0→mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011	1000	1bp.	<io8	...>							
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0→mem8(abs8)bp	0	●	0	●	4	4				1011	1bp.	<abs	8..>							
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0→mem8(abs16)bp	0	●	0	●	7	6			0011	1100	1bp.	<abs	16..	....	...>					
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	●	0	●	5	3			0010	0000	11Dm	<#8.	...>							
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	●	0	●	7	5			0011	1101	0bp.	<abs	16..	....	...>					
Branch instructions																						
Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H→PC if(ZF=0), PC+3→PC	--	--	--	--	3	2/3				1001	000H	<d4>								*1
	BEQ label	if(ZF=1), PC+4+d7(label)+H→PC if(ZF=0), PC+4→PC	--	--	--	--	4	2/3				1000	1010	<d7.	...H							*2
	BEQ label	if(ZF=1), PC+5+d11(label)+H→PC if(ZF=0), PC+5→PC	--	--	--	--	5	2/3				1001	1010	<d11	....	...H						*3
	BNE label	if(ZF=0), PC+3+d4(label)+H→PC if(ZF=1), PC+3→PC	--	--	--	--	3	2/3				1001	001H	<d4>								1
	BNE label	if(ZF=0), PC+4+d7(label)+H→PC if(ZF=1), PC+4→PC	--	--	--	--	4	2/3				1000	1011	<d7.	...H							*2
	BNE label	if(ZF=0), PC+5+d11(label)+H→PC if(ZF=1), PC+5→PC	--	--	--	--	5	2/3				1001	1011	<d11	....	...H						*3
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H→PC if((VF^NF)=1),PC+4→PC	--	--	--	--	4	2/3				1000	1000	<d7.	...H							*2
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H→PC if((VF^NF)=1),PC+5→PC	--	--	--	--	5	2/3				1001	1000	<d11	....	...H						*3
	BCC label	if(CF=0),PC+4+d7(label)+H→PC if(CF=1), PC+4→PC	--	--	--	--	4	2/3				1000	1100	<d7.	...H							*2
	BCC label	if(CF=0), PC+5+d11(label)+H→PC if(CF=1), PC+5→PC	--	--	--	--	5	2/3				1001	1100	<d11	....	...H						*3
	BCS label	if(CF=1),PC+4+d7(label)+H→PC if(CF=0), PC+4→PC	--	--	--	--	4	2/3				1000	1101	<d7.	...H							*2
	BCS label	if(CF=1), PC+5+d11(label)+H→PC if(CF=0), PC+5→PC	--	--	--	--	5	2/3				1001	1101	<d11	....	...H						*3
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H→PC if((VF^NF)=0),PC+4→PC	--	--	--	--	4	2/3				1000	1110	<d7.	...H							*2
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H→PC if((VF^NF)=0),PC+5→PC	--	--	--	--	5	2/3				1001	1110	<d11	....	...H						*3
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H→PC if((VF^NF)|ZF=0),PC+4→PC	--	--	--	--	4	2/3				1000	1111	<d7.	...H							*2
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H→PC if((VF^NF)|ZF=0),PC+5→PC	--	--	--	--	5	2/3				1001	1111	<d11	....	...H						*3
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H→PC if((VF^NF)|ZF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0001	<d7.	...H							*2

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H→PC if((VF^NF)|ZF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0001	<d11	....	...H						*3
	BHI label	if(CFIZF=0),PC+5+d7(label)+H→PC if(CFIZF=1), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0010	<d7.	...H							*2
	BHI label	if(CFIZF=0),PC+6+d11(label)+H→PC if(CFIZF=1), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0010	<d11	....	...H						*3
	BLS label	if(CFIZF=1),PC+5+d7(label)+H→PC if(CFIZF=0), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0011	<d7.	...H							*2
	BLS label	if(CFIZF=1),PC+6+d11(label)+H→PC if(CFIZF=0), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0011	<d11	....	...H						*3
	BNC label	if(NF=0),PC+5+d7(label)+H→PC if(NF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0100	<d7.	...H							*2
	BNC label	if(NF=0),PC+6+d11(label)+H→PC if(NF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0100	<d11	....	...H						*3
	BNS label	if(NF=1),PC+5+d7(label)+H→PC if(NF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0101	<d7.	...H							*2
	BNS label	if(NF=1),PC+6+d11(label)+H→PC if(NF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0101	<d11	....	...H						*3
	BVC label	if(VF=0),PC+5+d7(label)+H→PC if(VF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0110	<d7.	...H							*2
	BVC label	if(VF=0),PC+6+d11(label)+H→PC if(VF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0110	<d11	....	...H						*3
	BVS label	if(VF=1),PC+5+d7(label)+H→PC if(VF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0111	<d7.	...H							*2
	BVS label	if(VF=1),PC+6+d11(label)+H→PC if(VF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0111	<d11	....	...H						*3
	BRA label	PC+3+d4(label)+H→PC	--	--	--	--	3	3				1110	111H	<d4>								*1
	BRA label	PC+4+d7(label)+H→PC	--	--	--	--	4	3				1000	1001	<d7.	...H							*2
	BRA label	PC+5+d11(label)+H→PC	--	--	--	--	5	3				1001	1001	<d11	....	...H						*3
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H→PC if(Dm≠imm8),PC+6→PC	●	●	●	●	6	3/4				1100	10Dm	<#8.	...>	<d7.	...H					*2
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H→PC if(Dm≠imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1100	10Dm	<#8.	...>	<d11	....	...H				*3
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H→PC if(mem8(abs8)≠imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1100	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H→PC if(mem8(abs8)≠imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1101	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H→PC if(mem8(abs16)≠imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1100	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H→PC if(mem8(abs16)≠imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1101	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H→PC if(Dm=imm8),PC+6→PC	●	●	●	●	6	3/4				1101	10Dm	<#8.	...>	<d7.	..H>					*2
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H→PC if(Dm=imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1101	10Dm	<#8.	...>	<d11	....	...H				*3
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H→PC if(mem8(abs8)=imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1110	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H→PC if(mem8(abs8)=imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1111	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H→PC if(mem8(abs16)=imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1110	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H→PC if(mem8(abs16)=imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1111	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H→PC if(mem8(abs8)bp=1),PC+7→PC	0	●	0	●	7	6/7			0011	0000	0bp.	<abs	8..>	<d7.	...H					*2
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H→PC if(mem8(abs8)bp=1),PC+8→PC	0	●	0	●	8	6/7			0011	0000	1bp.	<abs	8..>	<d11	....	...H				*3

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+7→PC	0	●	0	●	7	6/7			0011	0100	0bp.	<io8	...>	<d7.	...H					*1
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+8→PC	0	●	0	●	8	6/7			0011	0100	1bp.	<io8	...>	<d11	....	...H				*2
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H→PC if(mem8(abs16)bp=1),PC+9→PC	0	●	0	●	9	7/8			0011	1110	0bp.	<abs	16..	....	...>	<d7.	...H			*1
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC if(mem8(abs16)bp=1),PC+10→PC	0	●	0	●	10	7/8			0011	1110	1bp.	<abs	16..	....	...>	<d11	....	...H		*2
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H→PC if(mem8(abs8)bp=0),PC+7→PC	0	●	0	●	7	6/7			0011	0001	0bp.	<abs	8..>	<d7.	...H					*1
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H→PC if(mem8(abs8)bp=0),PC+8→PC	0	●	0	●	8	6/7			0011	0001	1bp.	<abs	8..>	<d11	....	...H				*2
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H→PC if(mem8(io)bp=0),PC+7→PC	0	●	0	●	7	6/7			0011	0101	0bp.	<io8	...>	<d7.	...H					*1
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H→PC if(mem8(io)bp=0),PC+8→PC	0	●	0	●	8	6/7			0011	0101	1bp.	<io8	...>	<d11	....	...H				*2
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H→PC if(mem8(abs16)bp=0),PC+9→PC	0	●	0	●	9	7/8			0011	1111	0bp.	<abs	16..	....	...>	<d7.	...H			*1
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC if(mem8(abs16)bp=0),PC+10→PC	0	●	0	●	10	7/8			0011	1111	1bp.	<abs	16..	....	...>	<d11	....	...H		*2
JMP	JMP (An)	0→PC.17-16,An→PC.15-0,0→PC.H	---	---	---	---	3	4			0010	0001	00A0									
	JMP label	abs18(label)+H→PC	---	---	---	---	7	5			0011	1001	0aaH	<abs	18.b	p15~	0..>					*5
JSR	JSR (An)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+3).bp17-16→mem8(SP+2).bp1-0 0→PC.bp17-16 An→PC.bp15-0,0→PC.H	---	---	---	---	3	7			0010	0001	00A1									
	JSR label	SP-3→SP,(PC+5).bp7-0→mem8(SP) (PC+5).bp15-8→mem8(SP+1) (PC+5).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+5).bp17-16→mem8(SP+2).bp1-0 PC+5+d12(label)+H→PC	---	---	---	---	5	6			0001	000H	<d12	....	...>							*3
	JSR label	SP-3→SP,(PC+6).bp7-0→mem8(SP) (PC+6).bp15-8→mem8(SP+1) (PC+6).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+6).bp17-16→mem8(SP+2).bp1-0 PC+6+d16(label)+H→PC	---	---	---	---	6	7			0001	001H	<d16	....	....	...>						*4
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-2, (PC+7).bp17-16→mem8(SP+2).bp1-0 abs18(label)+H→PC	---	---	---	---	7	8			0011	1001	1aaH	<abs	18.b	p15~	0..>					*5
	JSRV (tbl4)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7 0→mem8(SP+2).bp6-2, (PC+3).bp17-16→mem8(SP+2).bp1-0 mem8(x'004080+tbl4<<2)→PC.bp7-0 mem8(x'004080+tbl4<<2+1)→PC.bp15-8 mem8(x'004080+tbl4<<2+2).bp7→PC.H mem8(x'004080+tbl4<<2+2).bp1-0→ PC.bp17-16	---	---	---	---	3	9			1111	1110	<t4>									
NOP	NOP	PC+2→PC	---	---	---	---	2	1	○		0000	0000										

*1 d7 sign-extension
*2 d11 sign-extension
*3 d12 sign-extension
*4 d16 sign-extension
*5 aa=abs18.17 - 16

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
RTS	RTS	mem8(SP)→(PC).bp7-0 mem8(SP+1)→(PC).bp15-8 mem8(SP+2).bp7→(PC).H mem8(SP+2).bp1-0→(PC).bp17-16 SP+3→SP	---	---	---	---	2	7			0000 0001											
RTI	RTI	mem8(SP)→PSW mem8(SP+1)→(PC).bp7-0 mem8(SP+2)→(PC).bp15-8 mem8(SP+3).bp7→(PC).H mem8(SP+3).bp1-0→(PC).bp17-16 mem8(SP+4)→HA-l mem8(SP+5)→HA-h SP+6→SP	●	●	●	●	2	11			0000 0011											
Contorl instructions																						
REP	REP imm3	imm3-1→RPC	---	---	---	---	3	2			0010 0001 1rep											*1

*1 no repeat whn imm3=0, (rep: imm3-1)

Other than the instruction of MN101C Series,the assembler of this Series has the following instructions as macro instructions.
The assembler will interpret the macro instructions below as the assembler instructions.

macro instructions		replaced instructions		remarks
INC	Dn	ADD	1,Dn	
DEC	Dn	ADD	-1,Dn	
INC	An	ADDW	1,An	
DEC	An	ADDW	-1,An	
INC2	An	ADDW	2,An	
DEC2	An	ADDW	-2,An	
CLR	Dn	SUB	Dn,Dm	n=m
ASL	Dn	ADD	Dn,Dm	n=m
LSL	Dn	ADD	Dn,Dm	n=m
ROL	Dn	ADDC	Dn,Dm	n=m
NEG	Dn	NOT ADD	Dn 1,Dn	
NOPL		MOVW	DWn,DWm	n=m
MOV	(SP),Dn	MOV	(0,SP),Dn	
MOV	Dn,(SP)	MOV	Dn,(0,SP)	
MOVW	(SP),DWn	MOVW	(0,SP),DWn	
MOVW	DWn,(SP)	MOVW	DWn,(0,SP)	
MOVW	(SP),An	MOVW	(0,SP),An	
MOVW	An,(SP)	MOVW	An,(0,SP)	

Ver3.2(2002.01.31)

17-8 Instruction Map

MN101C SERIES INSTRUCTION MAP

1st nibble\2nd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the exension code is b'oo10'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nible\ 3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2		BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3		BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

Extension code: b'0011'

2nd nibble\ 3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TBZ (abs8)bp,d7								TBZ (abs8)bp,d11							
1	TBNZ (abs8)bp,d7								TBNZ (abs8)bp,d11							
2	CMP Dn,Dm															
3	ADD Dn,Dm															
4	TBZ (io8)bp,d7								TBZ (io8)bp,d11							
5	TBNZ (io8)bp,d7								TBNZ (io8)bp,d11							
6	OR Dn,Dm															
7	AND Dn,Dm															
8	BSET (io8)bp								BCLR (io8)bp							
9	JMP abs18(label)								JSR abs18(label)							
A	XOR Dn,Dm / XOR #8,Dm															
B	ADDC Dn,Dm															
C	BSET (abs16)bp								BCLR (abs16)bp							
D	BTST (abs16)bp								cmp #8,(abs16)	mov #8,(abs16)			CBEQ #8,(abs16),d7/11		CBNE #8,(abs16),d7/11	
E	TBZ (abs16)bp,d7								TBZ (abs16)bp,d11							
F	TBNZ (abs16)bp,d7								TBNZ (abs16)bp,d11							

Ver2.1(2001.03.26)

Record of Changes

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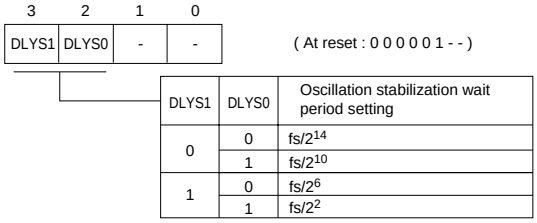
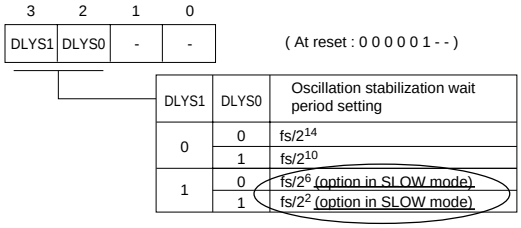
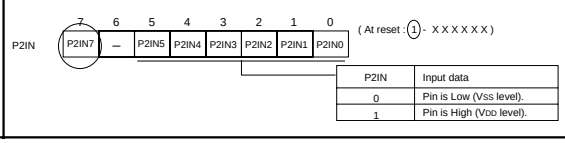
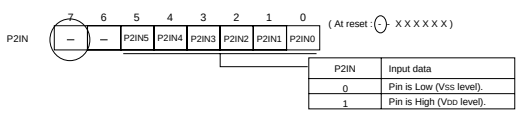
<table>
<tr><th rowspan="2">Page</th><th rowspan="2">Section</th><th rowspan="2"></th><th colspan="2">Definition of Changes</th></tr>
<tr><th>Previous Edition (Version 1.5)</th><th>New Edition (Version 1.6)</th></tr>
<tr><td>XVII-5</td><td>-</td><td>Change</td><td>YDC model: AF220/AF200 flash microcontroller programmer
http://www.ydc.co.jp/micom/product/download_impress.htm</td><td>YDC model: AF220/AF200 flash microcontroller programmer
http://www.ydc.co.jp/micom/product/download_impressE.htm</td></tr>
<tr><td>XVII-8</td><td>Table</td><td>Change</td><td>17-3-5 Microcontroller clock on the target board
<table><tr><th>Clock frequency Maximum / Operating voltage (VDD1)</th><th>Clock frequency Minimum / Operating voltage (VDD1)</th></tr><tr><td>2.0 MHz / 5.0 V</td><td>2.0 MHz / 2.5 V *1</td></tr></table></td><td>17-3-5 Microcontroller clock on the target board
<table><tr><th rowspan="2">Clock frequency</th><th colspan="2">Operating voltage</th></tr><tr><th>VDD1</th><th>VDD2</th></tr><tr><td>2 MHz ≤ fosc ≤ 20 MHz</td><td>5 V</td><td>5 V</td></tr><tr><td>2 MHz ≤ fosc ≤ 8.38 MHz</td><td>3 V</td><td>5 V</td></tr></table></td></tr>
</table>

Record of Changes

MN101C57 LSI User's Manual Record of Changes (Ver.1.3 to Ver.1.5) (1/2)

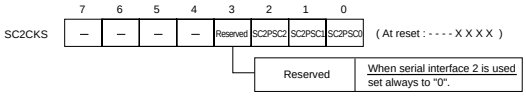
Page	Section		Definition of Changes	
			Previous Edition (Version 1.3)	New Edition (Version 1.5)
1-3, 1-20	Line7	Change	Machine cycle (at 2-devide of crystal oscillation) High speed mode: 0.5 µs / 4 MHz (2.3 V to 5.5 V)*1	Machine cycle (at 2-devide of crystal oscillation) High speed mode: 0.5 µs / 4 MHz (2.2 V to 5.5 V)*1
1-17	Note	Deletion	*1 When the reference voltage is input to VLCIN2 pin, 3/2 times voltage of the reference voltage is output to VLC1 pin, 1/2 times voltage of the reference voltage is output to VLC3 pin. When the reference voltage is input to VLCIN3 pin, 3 times voltage of the reference voltage is output to VLC1 pin, twice voltage of the reference voltage is output to VLC2 pin.	-
1-30	1-5-5 Table	Change	A/D Converter Characteristics: Rating MIN TYP MAX 4. Zero transition voltage 30 100 5. Full-scale transition voltage 4900 4970	A/D Converter Characteristics: Rating MIN TYP MAX 4. Zero transition voltage 10 30 5. Full-scale transition voltage 4970 4990
1-36 | 1-37	-	Addition	-	1-6-5 Oscillator
2-33	Figure 2-6-4	Change	Osillation stabilization wait time control register (DLYCTR : x'03F03', R/W) 	Osillation stabilization wait time control register (DLYCTR : x'03F03', R/W) 
10-3	Figure 10-2-1			
3-3	Table 3-1-1	Change	Maskable interrupt Vector number : 2 to 28 Table address : x'04008' to x'04070	Maskable interrupt Vector number : 2 to 26 Table address : x'04008' to x'04068
3-16	Note	Addition	-	On this LSI, when undefined instruction is decoded, the program interrupt request flag (PIR) is set to "1", and the non-maskable interrupt is generated. When the PIR flag is confirmed to be set using the non-maskable interrupt service routine, the reset via the software, which the reset pin (P27) outputs "0", is recommended.
	Caution	Addition	-	Once the WDIR becomes "1" by generation of non-maskable interrupt, only the program can clear it to "0".
4-3	Note	Addition	-	How to determine pull-up resistor value How to determine pull-down resistor value
4-19	Figure 4-4-1	Change	Port 2 input register(P2IN : x'03F22', R) 	Port 2 input register(P2IN : x'03F22', R) 

Note) Title, figure and table are not counted as lines.

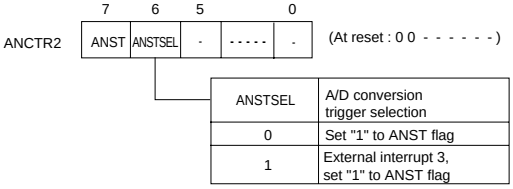
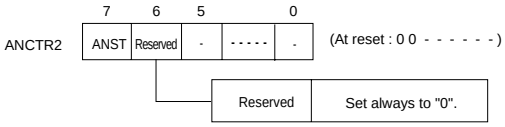
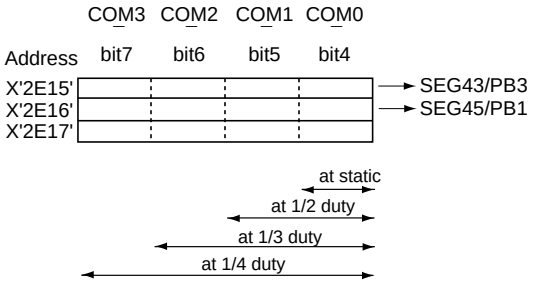
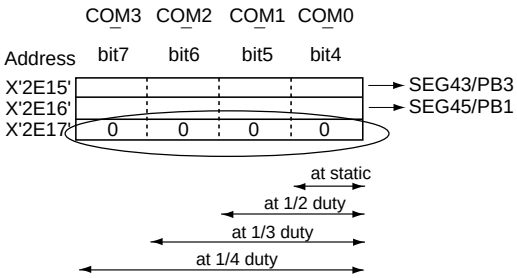
MN101C57 LSI User's Manual Record of Changes (Ver.1.3 to Ver.1.5) (2/2)

<table>
<tr><th rowspan="2">Page</th><th rowspan="2">Section</th><th rowspan="2"></th><th colspan="2">Definition of Changes</th></tr>
<tr><th>Previous Edition (Version 1.3)</th><th>New Edition (Version 1.5)</th></tr>
<tr><td>5-9

12-8</td><td>Figure 5-2-7

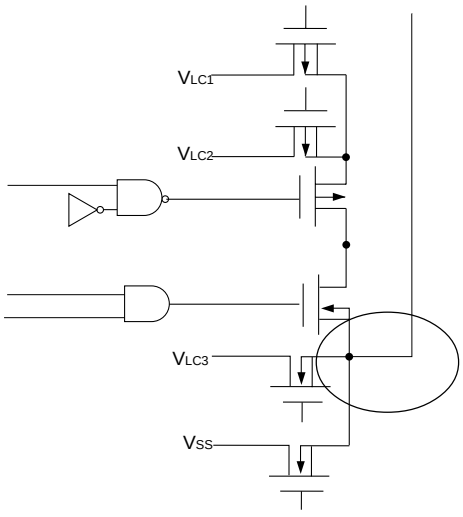
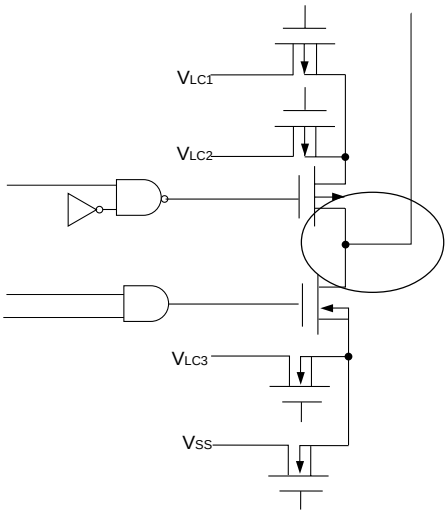
Figure 12-2-6</td><td>Change</td><td>Serial Interface 2 Transfer Clock Selection Register
(SC2CKS : x'03FA7', R/W)
</td><td>Serial Interface 2 Transfer Clock Selection Register
(SC2CKS : x'03FA7', R/W)
 
</td></tr>
<tr><td>13-6

17-14</td><td>Figure 13-2-3

address x'3FB2'</td><td>Change</td><td>AD converter control register 2 (ANCTR2)
 
</td><td>AD converter control register 2 (ANCTR2)
 
</td></tr>
<tr><td>14-8</td><td>Figure 14-2-2</td><td>Change</td><td>Mode Control Register 2 (LCDMD2: X3FDA, R/W)
(At reset: - 0 0 0 0 0 0 0 0)</td><td>Mode Control Register 2 (LCDMD2: X3FDA, R/W)
(At reset: 0 0 0 0 0 0 0 0 0)</td></tr>
<tr><td rowspan="2">14-13</td><td>Figure 14-2-7</td><td>Change</td><td>Matching of the Segment Output Latch and the Segment/ Common Pins:
 
</td><td>Matching of the Segment Output Latch and the Segment/ Common Pins:
 
</td></tr>
<tr><td>Caution</td><td>Addition</td><td>-</td><td>Upper 4 bits of x2E17 allocated to the segment output latch is unpopulated area. When data is read, 0 is read out from this area.</td></tr>
<tr><td>17-2
|
17-9</td><td>-</td><td>Addition</td><td>-</td><td>Description about Flash EEPROM</td></tr>
<tr><td>17-7</td><td>Table</td><td>Change</td><td>Address Register bit 7
X'3F22' P2IN P2IN7</td><td>Address Register bit 7
X'3F22' P2IN -</td></tr>
<tr><td>17-15</td><td>Table</td><td>Change</td><td>Address Register
X'3FCF' RMICR</td><td>Address Register
X'3FCF' RMTICR</td></tr>
<tr><td>17-18
|
17-23</td><td>Table</td><td>Change</td><td>17-4 Instruction Set ver.3.1</td><td>17-7 Instruction Set ver.3.2</td></tr>
<tr><td>17-24
|
17-25</td><td>Table</td><td>Change</td><td>17-5 Instruction Map ver.3.1</td><td>17-8 Instruction Map ver.3.2</td></tr>
</table>

Record of Changes

MN101C57 LSI User's Manual Record of Changes (Ver.1.1 to Ver.1.3)

Page	Section		Definition of Changes	
			Previous Edition (Version 1.1)	New Edition (Version 1.3)
1-5		Change	Timer 8; - Square wave output and PWM output can be output to large current driver port P51 (TM70).	Timer 8; - Square wave output and PWM output can be output to large current driver port P53 (TM80).
1-5	Line 1-2	Change	♦Unused Pins (only for output pin) Set unused pins (only for output pin)open.	♦Unused Pins (output pins and LCD output pins) Set unused pins (output pins and LCD output pins) open.
3-3	Table 3-1-1	Change	Interrupt factor of reset : External RST pin input	Interrupt factor of reset : NRST pin input
4-65 to 4-67	Figure 4-13-3 4-13-4 4-13-5	Change		
11-40	11-3-3	Addition	-	♦Transfer bit Count and Transfer First bit in UART communitation ♦Receive bit Count and Transfer First bit in UART communitation
11-41	Line 8-11	Delition	♦Transfer bit Count and Transfer First bit Refer to : XI-15 ♦Receive bit Count and Transfer First bit Refer to : XI-15	-
13-12		Change	(2) Select the analog input pin. ANCTR1 (x'3FB1') bp2-0 : ANCHS2-0 = 000 Select the analog input pin from AN7-0 (PA7-0) by the ANCHS2-0 flag of the A/D converter control register 1 (ANCTR1).	(2) Select the analog input pin. ANCTR1 (x'3FB1') bp3-0 : ANCHS3-0 = 000 Select the analog input pin from AN15-0 (PB7-0, PA7-0) by the ANCHS3-0 flag of the A/D converter control register 1 (ANCTR1).
14-2 to 14-5	14-1	Change	-	Organization of the section is changed.
14-6		Change	* Address x'02E00' to x'02E0F' are assigned to the segment output latch.	* Address x'02E00' to x'02E17' are assigned to the segment output latch.
14-13	Line 5	Change	The assigned address are X2E00' to X2E0F', and segment output latch value is indefined at reset.	The assigned address are X2E00' to X2E017', and segment output latch value is indefined at reset.

Note) Title, figure and table are not counted as lines.

MN101C57C/57D LSI User's Manual Description Record of Changes (Ver.1.1 to 1.2)

page	Line	definition	Description of Changes	
			Former version	New version
Cover	Pub number	C	21457-011E	21457-012E
Colophon		C	September, 2001 1st Edition 1st Printing	October, 2001 1st Edition 2nd Printing
Sales office		C		Latest version

<Definition>
A: add
D: delete
C: modify, change

MN101C57C/57D/F57D
LSI User's Manual

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